SRAM DATA BOOK

MICRON
TECHNOLOGY, INC.

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SRAM DATA BOOK

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ABOUT THE COVER:

Front — Clockwise from left, 1) Micron's Cache Data SRAM wafer; 2) Micron team members build quality into every Micron wafer at our Boise, Idaho, facilities; 3) a SEM photograph of the SRAM lithography process; and 4) Micron's packaged SRAMs in SOJ, PQFP and SOIC packages.

Back — Micron's Boise, Idaho, headquarters.

IMPORTANT NOTICE

Micron Technology, Inc., reserves the right to change products or specifications without notice. Customers are advised to obtain the latest versions of product specifications, which should be considered in evaluating a product's appropriateness for a particular use. There is no assurance that Micron's semiconductors are appropriate for any application by a customer.

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A. LIFE SUPPORT DEVICES OR SYSTEMS ARE DEVICES OR SYSTEMS WHICH (1) ARE INTENDED FOR SURGICAL IMPLANT INTO THE BODY, OR (2) SUPPORT OR SUSTAIN LIFE AND WHOSE FAILURE TO PERFORM WHEN PROPERLY USED IN ACCORDANCE WITH INSTRUCTIONS FOR USE PROVIDED IN THE LABELING CAN BE REASONABLY EXPECTED TO RESULT IN A SIGNIFICANT INJURY TO THE USER.

B. CRITICAL COMPONENT IS ANY COMPONENT OF A LIFE SUPPORT DEVICE OR SYSTEM WHOSE FAILURE TO PERFORM CAN BE REASONABLY EXPECTED TO CAUSE THE FAILURE OF THE LIFE SUPPORT DEVICE OR SYSTEM OR TO AFFECT ITS SAFETY OR EFFECTIVENESS.

ADVANTAGES

Quality, productivity and innovation unite at Micron. Because of our emphasis on quality, we have created hundreds of reliable, high-performance memory products. Our products feature some of the industry's fastest speeds and smallest die sizes, delivered when you need them, and reliable beyond your expectations. And, because we produce our products in a centralized location, we can offer unparalleled flexibility and project control.

COMPONENT INTEGRATED CIRCUITS

Micron Technology entered the memory market 14 years ago to manufacture dynamic random access memory (DRAM). From there, we developed high-performance fast static RAM (SRAM), multiport DRAM (VRAM and Triple Port DRAM), and a variety other memory products.

As we bring progressive memory solutions to our customers, we enjoy recognition for our achievements. Micron's Triple Port DRAM was the first IC ever to incorporate a second, independent serial access port, allowing unparalleled flexibility in data manipulation. In 1990, Micron's Triple Port received the 1990 "Product of the Year" award from *Electronic Products* magazine.

SPECIALTY MEMORY PRODUCTS

Beyond our standard component memory, Micron is introducing many revolutionary products that we expect will follow the Triple Port's tradition. From FIFOs to processors, Micron continues to forge ahead into new and exciting frontiers.

We are pleased to be first to market with our compact, easy-to-install IC DRAM Card. Ideal for laptop, notebook and other portable systems, Micron's IC DRAM Card offers both high density and low power within JEDEC and JEIDA specifications.

MILITARY CERTIFIED PRODUCTS

As one of the few manufacturers of military-grade memory in North America, Micron is proud to provide a documented source inspection from wafer start to finished product. We've earned recognition from U.S. and European space agencies as well as Joint Army/Navy certification for both our NMOS and CMOS process technologies.

DIE SALES

In addition to our durable ceramic packaging, Micron also provides memory devices in bare die form. These are increasingly in demand for commercial and military use in highly specialized applications. Micron's bare dice are available in 6" wafers and wafflepacks.

OEM SYSTEM-LEVEL PRODUCTS

For total project management, Micron offers added value services. These include both standard contract manufacturing of system-level products from any single phase — design, assembly, customer kitted assembly, comprehensive quality testing or shipping — and complete turnkey services covering all phases of production. Our component and system-level manufacturing facilities are centrally located in Boise, Idaho, so any reliable component products you may need for your board are readily available.

QUALITY

Without a doubt, the most important thing we provide goes out to every Micron customer with every Micron product — quality. That's because we believe that quality must be internalized at every level of our company. We're committed to our employees as well as our customers. We provide every Micron team member with the tools, confidence and motivation they need to make Micron's quality philosophy a reality.

One way we have measurably improved both productivity and product quality is through our quality improvement teams. These groups of Micron team members get together to address a wide range of issues within their areas. We've also implemented statistical process controls to evaluate every facet of the memory design, fabrication, assembly and shipping process. And our AMBYX™ intelligent burn-in and test system* gives Micron the ultimate edge in product reliability.

*For more information on Micron's AMBYX™, see Section 7.

Micron Technology, Inc., is dedicated to the design, manufacture and marketing of high quality, highly reliable memory integrated circuits. Our corporate mission is:

"To be a world class team
developing advantages for our customers"

At Micron, we are investing time, talent and resources to bring you the finest DRAMs, SRAMs, VRAMs and other specialty memory products. We have developed a unique intelligent burn-in system, the AMBYX™, that evaluates and reports the quality level of each and every component we produce.

We are dedicated to continuous improvement of all our products and services. This means continual reduction of electrical and mechanical defect levels. It also means the addition of new services such as "just-in-time" delivery and electronic data interchange programs. And, when you have a design or application question, you can get the answers you need from the source — one of Micron's applications engineers.

We're proud of our products, our progress and our performance. And we're pleased that you're choosing Micron as your memory supplier.

The Micron Team

ABOUT THIS BOOK

CONTENT

The 1992 ***SRAM Data Book*** from Micron Technology provides complete specifications on all standard SRAMs and SRAM modules as well as specialty and derivative products based on our SRAM production process.

The SRAM Data Book is one of three product data books Micron publishes. Its two companion volumes include our ***DRAM Data Book*** (to be released in February/March 1992) and ***Military Data Book*** (currently available).*

SECTION ORGANIZATION

Micron's 1992 ***SRAM Data Book*** contains a detailed Table of Contents with sequential and numerical indexes of products as well as a complete product selection guide. The Data Book is organized into nine sections:

- **Sections 1–5:** Individual product families. Contains a product selection guide followed by data sheets.
- **Section 6:** Application information.
- **Section 7:** Summary of Micron's unique quality and reliability programs and testing operation, including our AMBYX™ intelligent burn-in and test system.**
- **Section 8:** Packaging information.
- **Section 9:** Product ordering information, including a list of sales representatives and distributors worldwide.

DATA SHEET SEQUENCE

Data sheets in this book are ordered by width first and depth second. For example, the SRAM section begins with the 16K x 1 SRAM followed by 64K x 1 and all other x1 configurations in order of ascending depth. Next come the x4 products, followed by x8, etc., as applicable to the specific product family.

DATA SHEET DESIGNATIONS

As detailed below, each Micron product data sheet is classified as either **Advance, Preliminary** or **Final**. In addition, new product data sheets that are new additions to this data book are designated with a "New" in the tab area of the front page.

SURVEY

We have included a removable, postage-paid survey form in the front of this book. Your time in completing and returning this survey will enhance our efforts to continually improve our product literature.

For more information on Micron product literature, or to order additional copies of this publication, contact:

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DATA SHEET DESIGNATORS

DATA SHEET MARKING	DEFINITION
"Advance"	This data sheet contains initial descriptions of products still under development.
"Preliminary"	This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.
No Marking (Final)	This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.
"New"	This data sheet (which may be either Advance, Preliminary or Final) is a new addition to the Data Book.

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* For complete information on Micron's Military Products, send for our ***Military Data Book*** by calling Micron Technology, Inc.

** Micron's ***Quality/Reliability Handbook*** is available by calling the number listed above.

COMPONENT PRODUCT NUMBERING SYSTEM

Format = AA BB CC DDDD EE FFF-GG HH HH*

PRODUCT FAMILY

DRAM = 4
DPDRAM = 42
TPDRAM = 43
DRAM FIFO = 46
SRAM = 5
FIFO = 52
CACHE/LATCHED SRAM = 56
SYNCHRONOUS SRAM = 58

DEVICE NUMBER
(NUMBER CAN BE MODIFIED TO INDICATE VARIATIONS)

DRAM = Width, Density
DPDRAM = Width, Density
TPDRAM = Width, Density
DRAM FIFO = Width, Density
SRAM = Total Bits, Width
LATCHED SRAM = Total Bits, Width
CACHE SRAM = Density, Width
FIFO = Width, Density
SYNCH. SRAM = Density, Width

OPTIONS
(LISTED IN HIERARCHY IN CASE OF MULTIPLE OPTIONS)

Interim (Errata) Version = I
Low Power, Extended Refresh DRAM and Low Power SRAM = L
JEDEC Test Mode (4 Meg DRAM) = J
3.3V = V
3.3V, Low Power, Extended Refresh = H
2K Refresh (16 Meg DRAM) = R
Self & Extended Refresh, Low Power = S

| AA | BB | CC | DDDD | EE | FFF | GG | HH HH* |

PRODUCT LINE IDENTIFIER

Micron Technology Component Product = MT

PROCESS TECHNOLOGY

CMOS = C
BICMOS = B

PACKAGE CODE

PLASTIC
- DIP = Blank
- DIP (Wide Body) = W
- ZIP = Z
- LCC = EJ
- SOIC = SG
- QFP = LG
- TSOP (Type II) = TG
- TSOP (Reversed) = RG
- TSOP (Longer) = TL
- SOJ = DJ
- SOJ (Reversed) = DR
- SOJ (Longer) = DL

DIE
- Die = XDC
- Wafer = XWC
- Military Die = XD
- Military Wafer = XW

CERAMIC
- DIP = C
- DIP (Wide Body) = CW
- LCC (Narrow Body) = ECN
- LCC = EC
- LCC (Wide Body) = ECW
- SOIC = CG
- SOJ = DCJ
- PGA = CA
- FLAT PACK = F

ACCESS TIME

-8 = 8ns or 80ns
-10 = 10ns or 100ns
-12 = 12ns or 120ns
-15 = 15ns or 150ns
-17 = 17ns
-20 = 20ns
-25 = 25ns
-35 = 35ns
-45 = 45ns
-50 = 50ns
-53 = 53ns
-55 = 55ns
-60 = 60ns
-70 = 70ns
-85 = 85ns

PROCESSING* LEVEL/TEMP/SPECIAL

Commercial Process
- 0°C to +70°C = Blank
- -40°C to +85°C = IT
- -40°C to +125°C = AT
- -55°C to +125°C = XT

MIL-STD-883C
- -55°C to +125°C = 883C
- -55°C to +110°C (DRAMs) = 883C
- 0°C to +70°C = M070
- Low Volt Data Retention = L
- Tape and Reel = TR
- Bar Code = BC
- EPI Wafer = E

* Multiple processing codes are separated by a space. Listed in hierarchy in case of multiple options.

MODULE PRODUCT NUMBERING SYSTEM

Format = AA BB C DDD EE-FF GG*

PACKAGE CODE

DIP = D
GOLD PLATE = G
ZIP = Z
SIP = N
SIMM = M

NUMBER OF PARTS

DEPTH

| AA | BB | C | DDD | EE | F | GG* |

PRODUCT LINE IDENTIFIER

Micron Technology Component Product = MT

RAM FAMILY

SRAM = S
DRAM = D

ORGANIZATION

Width

SPECIAL DESIGNATOR*

Partial = P
Low Power = L

* Multiple processing codes are separated by a space. Listed in hierarchy in case of multiple options.

STATIC RAMS PAGE

CE .... CHIP ENABLE
OE .... OUTPUT ENABLE
OT .... OUTPUTS TRACK INPUTS DURING WRITE
SI/O .... SEPARATE DATA INPUTS AND OUTPUTS
HZ .... HIGH IMPEDANCE OUTPUTS DURING WRITE

SYNCHRONOUS SRAMS

SR	SYNCHRONOUS READS
DSCE	DUAL SYNCHRONOUS CHIP ENABLE
BW	BYTE WRITE
STW	SELF-TIMED WRITES
SWE	SYNCHRONOUS WRITE ENABLE

SRAM MODULES

CE	CHIP ENABLE
OE	OUTPUT ENABLE

CACHE DATA/LATCHED SRAMS

CE	CHIP ENABLE
OE	OUTPUT ENABLE
BW	BYTE WRITE
LA/Data	LATCHED ADDRESS AND DATA
DCE	DUAL CHIP ENABLE
SWE	SYNCHRONOUS WRITE ENABLE
BS	BYTE SELECT

FIFO (FIRST-IN FIRST-OUT) MEMORIES

PAGE

E .... EXPANDABLE DEPTH AND WIDTH PF .... PROGRAMMABLE FLAG

APPLICATION/TECHNICAL INFORMATION

PRODUCT RELIABILITY

PACKAGE INFORMATION

SALES INFORMATION

NUMERICAL INDEX

Part # **PAGE**

NUMERICAL INDEX (Continued)

PAGE

Part #

SRAM PRODUCT SELECTION GUIDE*

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and Number of Pins				Process	Page
				PDIP	SOJ	ZIP	SOIC		
16K x 1	$\overline{CE}$ only	MT5C1601	8 to 35	20	24	-	-	CMOS	1-1
64K x 1	$\overline{CE}$ only	MT5C6401	8 to 35	22	24	-	-	CMOS	1-9
256K x 1	$\overline{CE}$ only	MT5C2561	15 to 45	24	24	-	-	CMOS	1-17
1 Meg x 1	$\overline{CE}$ only	MT5C1001	20 to 45	28	28	-	-	CMOS	1-25
4K x 4	$\overline{CE}$ only	MT5C1604	8 to 35	20	24	-	-	CMOS	1-33
4K x 4	$\overline{CE}$ & $\overline{OE}$	MT5C1605	8 to 35	22	24	-	-	CMOS	1-41
4K x 4	Separate I/O	MT5C1606	8 to 35	24	24	-	-	CMOS	1-49
4K x 4	Separate I/O, High-Z	MT5C1607	8 to 35	24	24	-	-	CMOS	1-49
16K x 4	$\overline{CE}$ only	MT5C6404	8 to 35	22	24	-	-	CMOS	1-57
16K x 4	$\overline{CE}$ & $\overline{OE}$	MT5C6405	8 to 35	24	24	-	-	CMOS	1-65
16K x 4	Separate I/O, $\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$	MT5C6406	8 to 35	28	28	-	-	CMOS	1-73
16K x 4	Separate I/O, High-Z	MT5C6407	8 to 35	28	28	-	-	CMOS	1-73
64K x 4	$\overline{CE}$ only	MT5C2564	15 to 45	24	24	-	24	CMOS	1-81
64K x 4	$\overline{CE}$ & $\overline{OE}$	MT5C2565	15 to 45	28	28	-	-	CMOS	1-89
256K x 4	$\overline{CE}$ & $\overline{OE}$	MT5C1005	20 to 45	28	28	-	-	CMOS	1-97
1 Meg x 4	$\overline{CE}$ & $\overline{OE}$	MT5C4005	20 to 55	-	32	-	-	CMOS	1-105
1 Meg x 4	$\overline{CE}$ & $\overline{OE}$	MT5C4105	12 to 17	-	32	-	-	CMOS	1-107
2K x 8	$\overline{CE}$ & $\overline{OE}$	MT5C1608	8 to 35	24	24	-	-	CMOS	1-109
8K x 8	$\overline{CE1}$, CE2 & $\overline{OE}$	MT5C6408	8 to 35	28	28	-	-	CMOS	1-117
32K x 8	$\overline{CE}$ & $\overline{OE}$	MT5C2568	15 to 45	28	28	28	-	CMOS	1-125
128K x 8	$\overline{CE1}$, CE2 & $\overline{OE}$	MT5C1008	20 to 45	32	32	-	-	CMOS	1-133
128K x 8	$\overline{CE}$ & $\overline{OE}$	MT5C1009	20 to 45	32	32	-	-	CMOS	1-141
512K x 8	$\overline{CE}$ & $\overline{OE}$	MT5C4008	20 to 55	-	32	-	-	CMOS	1-149
512K x 8	$\overline{CE}$ & $\overline{OE}$	MT5C4108	12 to 17	-	36	-	-	CMOS	1-151
32K x 9	$\overline{CE1}$, CE2 & $\overline{OE}$	MT5C2889	15 to 25	-	32	-	-	CMOS	1-153
128K x 9	$\overline{CE}$ & $\overline{OE}$	MT5C1189	17 to 35	-	32	-	-	CMOS	1-161
256K x 16	$\overline{CE}$ & $\overline{OE}$	MT5C4116	12 to 17	-	44	-	-	CMOS	1-169

*Automotive, industrial and extended temperature specifications begin on page 1-171.

SYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package			Process	Page
				PLCC	PQFP	SOJ		
128K x 9	Synchronous SPARC™ Cache SRAM	MT58C1289	16, 20	-	-	32	CMOS	2-1
16K x 16	Registered Address, Write Control, Dual Chip Enable; Data Input Latch	MT58C1616	15, 17, 20, 25	52	52	-	CMOS	2-11
16K x 18	Registered Address, Write Control, Dual Chip Enable; Data Input Latch	MT58C1618	15, 17, 20, 25	52	52	-	CMOS	2-21

SRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Package and No. of Pins			Process	Page
				DIP	ZIP	SIMM		
128K x 8	$\overline{CE}$ & $\overline{OE}$	MT4S1288	30, 35, 45	32	-	-	CMOS	3-1
32K x 16	$\overline{CE}$ & $\overline{OE}$	MT2S3216	30, 35, 45	40	-	-	CMOS	3-9
64K x 16	$\overline{CE}$ & $\overline{OE}$	MT4S6416	30, 35, 45	40	-	-	CMOS	3-17
16K x 32	$\overline{CE}$ & $\overline{OE}$	MT8S1632	15, 20, 25, 30, 35, 45	-	64	64	CMOS	3-25
64K x 32	$\overline{CE}$ & $\overline{OE}$	MT8S6432	20, 25, 30, 35, 45	-	64	64	CMOS	3-33
128K x 32	$\overline{CE}$ & $\overline{OE}$	MT4S12832	20, 25, 35, 45	-	64	64	CMOS	3-41
256K x 32	$\overline{CE}$ & $\overline{OE}$	MT8S25632	20, 25, 35, 45	-	64	64	CMOS	3-49

CACHE DATA/LATCHED SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package		Process	Page
				PLCC	PQFP		
Dual 4K x 16 or Single 8K x 16	Mode, Byte Select, CE, OE Address Latch (A0-A11)	MT56C0816	20, 25, 35	52	52	CMOS	4-1
Dual 4K x 16 or Single 8K x 16	Mode, Byte Select, CE, OE Address Latch (A0-A12)	MT56C3816	20, 25, 35	52	52	CMOS	4-13
16K x 16	Latched Address and Data, Dual Chip Enables, Byte Write Controls	MT5C2516	15, 17, 20, 25	52	52	CMOS	4-25
Dual 4K x 18 or Single 8K x 18	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Address Latch (A0-A11)	MT56C0818	20, 25, 35	52	52	CMOS	4-39
Dual 4K x 18 or Single 8K x 18	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Synchronous Write Enable	MT56C2818	24, 28	52	52	CMOS	4-51
Dual 4K x 18 or Single 8K x 18	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Address Latch (A0-A12)	MT56C3818	20, 25, 35	52	52	CMOS	4-61
16K x 18	Latched Address and Data, Dual Chip Enables, Byte Write Controls	MT5C2818	15, 17, 20, 25	52	52	CMOS	4-73

FIFO MEMORIES PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Cycle Time (ns)	Package and Number of Pins			Process	Page
				PDIP	PLCC	SOJ		
512 x 9	Expandable Depth and Width	MT52C9005	15, 20, 25, 35	28	32	28	CMOS	5-1
512 x 9	Programmable Flag Expandable Depth and Width	MT52C9007	15, 20, 25, 35	28	32	28	CMOS	5-13
1K x 9	Expandable Depth and Width	MT52C9010	15, 20, 25, 35	28	32	28	CMOS	5-29
1K x 9	Programmable Flag Expandable Depth and Width	MT52C9012	15, 20, 25, 35	28	32	28	CMOS	5-41
2K x 9	Expandable Depth and Width	MT52C9020	15, 20, 25, 35	28	32	28	CMOS	5-57
2K x 9	Programmable Flag Expandable Depth and Width	MT52C9022	15, 20, 25, 35	28	32	28	CMOS	5-69

APPLICATION/TECHNICAL NOTE SELECTION GUIDE

SRAM PRODUCT SELECTION GUIDE*

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and Number of Pins				Process	Page
				PDIP	SOJ	ZIP	SOIC		
16K x 1	$\overline{\text{CE}}$ only	MT5C1601	8 to 35	20	24	-	-	CMOS	1-1
64K x 1	$\overline{\text{CE}}$ only	MT5C6401	8 to 35	22	24	-	-	CMOS	1-9
256K x 1	$\overline{\text{CE}}$ only	MT5C2561	15 to 45	24	24	-	-	CMOS	1-17
1 Meg x 1	$\overline{\text{CE}}$ only	MT5C1001	20 to 45	28	28	-	-	CMOS	1-25
4K x 4	$\overline{\text{CE}}$ only	MT5C1604	8 to 35	20	24	-	-	CMOS	1-33
4K x 4	$\overline{\text{CE}}$ & $\overline{\text{OE}}$	MT5C1605	8 to 35	22	24	-	-	CMOS	1-41
4K x 4	Separate I/O	MT5C1606	8 to 35	24	24	-	-	CMOS	1-49
4K x 4	Separate I/O, High-Z	MT5C1607	8 to 35	24	24	-	-	CMOS	1-49
16K x 4	$\overline{\text{CE}}$ only	MT5C6404	8 to 35	22	24	-	-	CMOS	1-57
16K x 4	$\overline{\text{CE}}$ & $\overline{\text{OE}}$	MT5C6405	8 to 35	24	24	-	-	CMOS	1-65
16K x 4	Separate I/O, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, $\overline{\text{OE}}$	MT5C6406	8 to 35	28	28	-	-	CMOS	1-73
16K x 4	Separate I/O, High-Z	MT5C6407	8 to 35	28	28	-	-	CMOS	1-73
64K x 4	$\overline{\text{CE}}$ only	MT5C2564	15 to 45	24	24	-	24	CMOS	1-81
64K x 4	$\overline{\text{CE}}$ & $\overline{\text{OE}}$	MT5C2565	15 to 45	28	28	-	-	CMOS	1-89
256K x 4	$\overline{\text{CE}}$ & $\overline{\text{OE}}$	MT5C1005	20 to 45	28	28	-	-	CMOS	1-97
1 Meg x 4	$\overline{\text{CE}}$ & $\overline{\text{OE}}$	MT5C4005	20 to 55	-	32	-	-	CMOS	1-105
1 Meg x 4	$\overline{\text{CE}}$ & $\overline{\text{OE}}$	MT5C4105	12 to 17	-	32	-	-	CMOS	1-107
2K x 8	$\overline{\text{CE}}$ & $\overline{\text{OE}}$	MT5C1608	8 to 35	24	24	-	-	CMOS	1-109
8K x 8	$\overline{\text{CE1}}$, CE2 & $\overline{\text{OE}}$	MT5C6408	8 to 35	28	28	-	-	CMOS	1-117
32K x 8	$\overline{\text{CE}}$ & $\overline{\text{OE}}$	MT5C2568	15 to 45	28	28	28	-	CMOS	1-125
128K x 8	$\overline{\text{CE1}}$, CE2 & $\overline{\text{OE}}$	MT5C1008	20 to 45	32	32	-	-	CMOS	1-133
128K x 8	$\overline{\text{CE}}$ & $\overline{\text{OE}}$	MT5C1009	20 to 45	32	32	-	-	CMOS	1-141
512K x 8	$\overline{\text{CE}}$ & $\overline{\text{OE}}$	MT5C4008	20 to 55	-	32	-	-	CMOS	1-149
512K x 8	$\overline{\text{CE}}$ & $\overline{\text{OE}}$	MT5C4108	12 to 17	-	36	-	-	CMOS	1-151
32K x 9	$\overline{\text{CE1}}$, CE2 & $\overline{\text{OE}}$	MT5C2889	15 to 25	-	32	-	-	CMOS	1-153
128K x 9	$\overline{\text{CE}}$ & $\overline{\text{OE}}$	MT5C1189	17 to 35	-	32	-	-	CMOS	1-161
256K x 16	$\overline{\text{CE}}$ & $\overline{\text{OE}}$	MT5C4116	12 to 17	-	44	-	-	CMOS	1-169

*Automotive, industrial and extended temperature specifications begin on page 1-171.

NOTE: Many Micron components are available in bare die form. Contact Micron Technology, Inc., for more information.

SRAM

16K x 1 SRAM

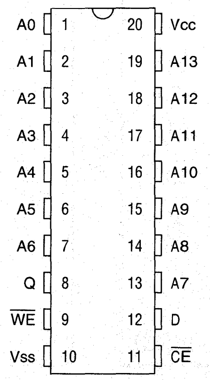
FEATURES

- High speed: 8, 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{\text{CE}}$ option
- All inputs and outputs are TTL compatible

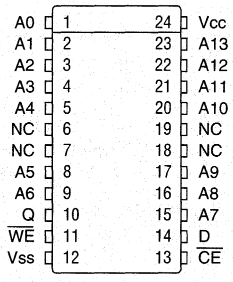
OPTIONS	MARKING
• Timing	
8ns access (preliminary)	- 8
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

20-Pin DIP
(A-4)



24-Pin SOJ
(E-4)



GENERAL DESCRIPTION

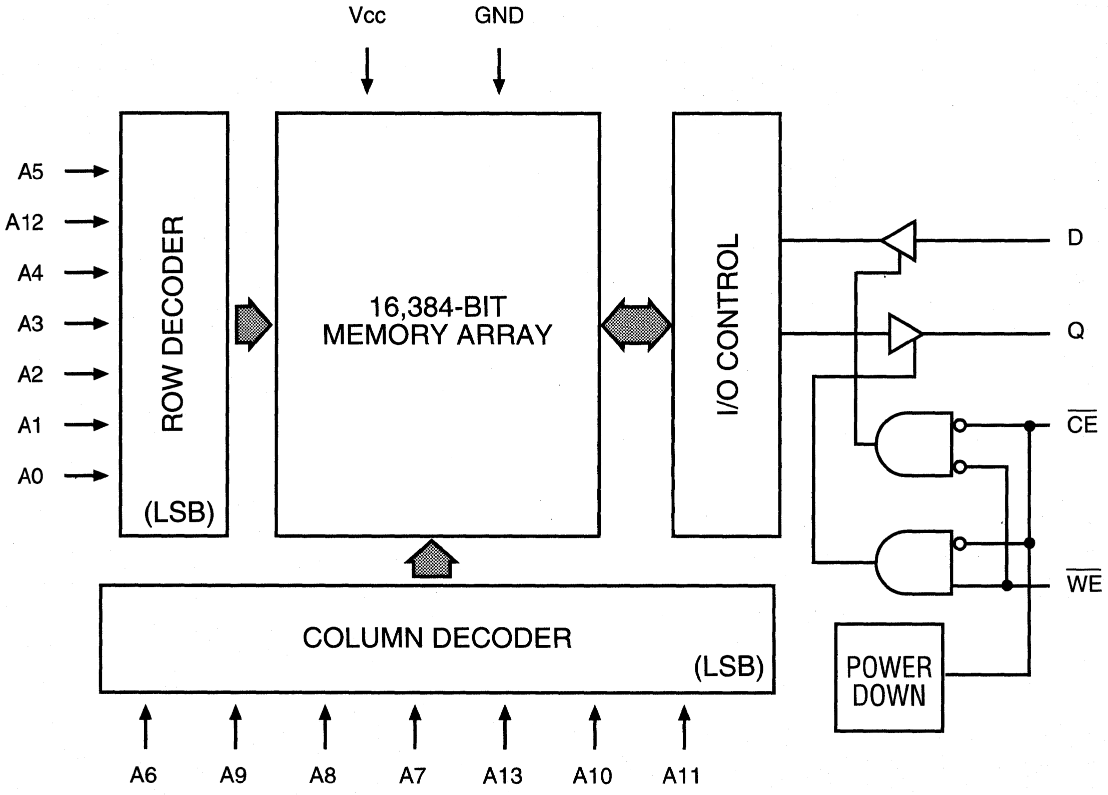
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{\text{CE}}$) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{\text{WE}}$) and $\overline{\text{CE}}$ inputs are both LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH and $\overline{\text{CE}}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \leq V_{OUT} \leq V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX								
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-8**	**-10**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}$; Vcc = MAX f = MAX = 1/ ${}^tRC$ Outputs Open	I_{CC}	65	160	150	140	120	110	100	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}$; Vcc = MAX f = MAX = 1/ ${}^tRC$ Outputs Open	I_{SB1}	20	55	50	45	40	35	30	25	mA	14
	$\overline{CE} \geq$ Vcc -0.2V; Vcc = MAX $V_{IL} \leq$ Vss +0.2V $V_{IH} \geq$ Vcc -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	3	3	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz	C_I	7	pF	4
Output Capacitance	Vcc = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	^{t}RC	8		10		12		15		20		25		35		ns	
Address access time	^{t}AA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^{t}ACE		7		9		10		12		15		20		30	ns	
Output hold from address change	^{t}OH	3		3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^{t}LZCE	2		2		2		3		5		5		5		ns	
Chip disable to output in High-Z	^{t}HZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		8		10		12		15		20		25		35	ns	
WRITE Cycle																	
WRITE cycle time	^{t}WC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^{t}CW	8		9		10		12		15		20		25		ns	
Address valid to end of write	^{t}AW	8		9		11		12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		0		0		ns	
WRITE pulse width	^{t}WP	7		8		9		12		15		18		20		ns	
Data setup time	^{t}DS	5		6		7		8		10		10		12		ns	
Data hold time	^{t}DH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	2		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^{t}HZWE		4		5		5		6		8		8		8	ns	6

*These specifications are preliminary.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

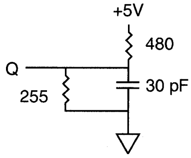


Fig. 1 OUTPUT LOAD EQUIVALENT

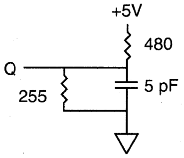


Fig. 2 OUTPUT LOAD EQUIVALENT

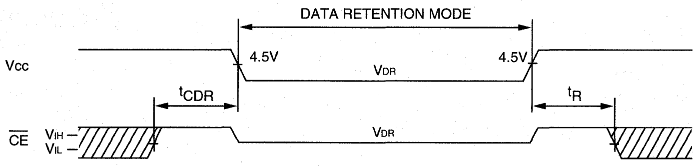
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-171.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{\text{CE}}$ ≥ (Vcc -0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

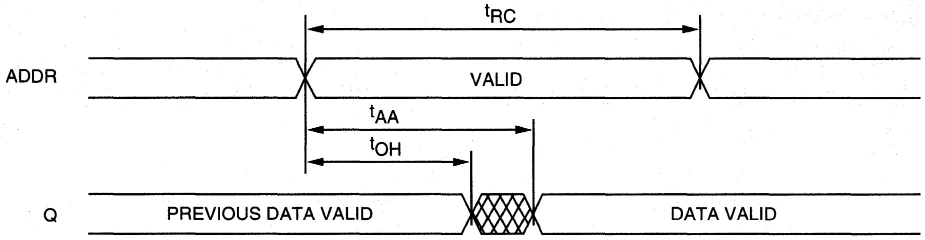
LOW Vcc DATA RETENTION WAVEFORM



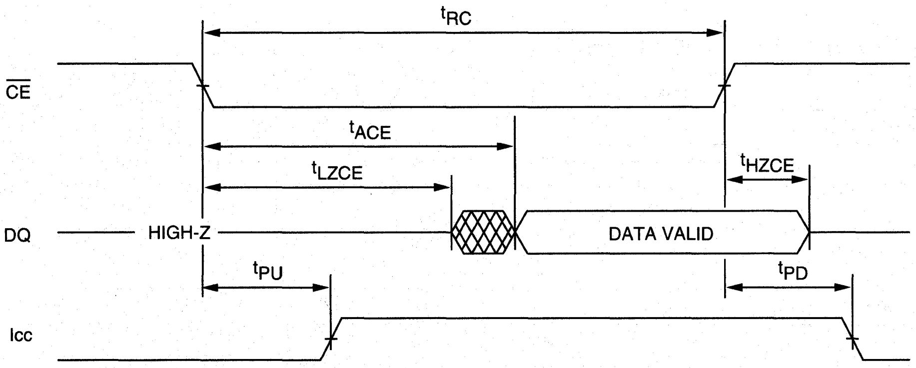
▨ DON'T CARE

▩ UNDEFINED

READ CYCLE NO. 1 [8, 9]



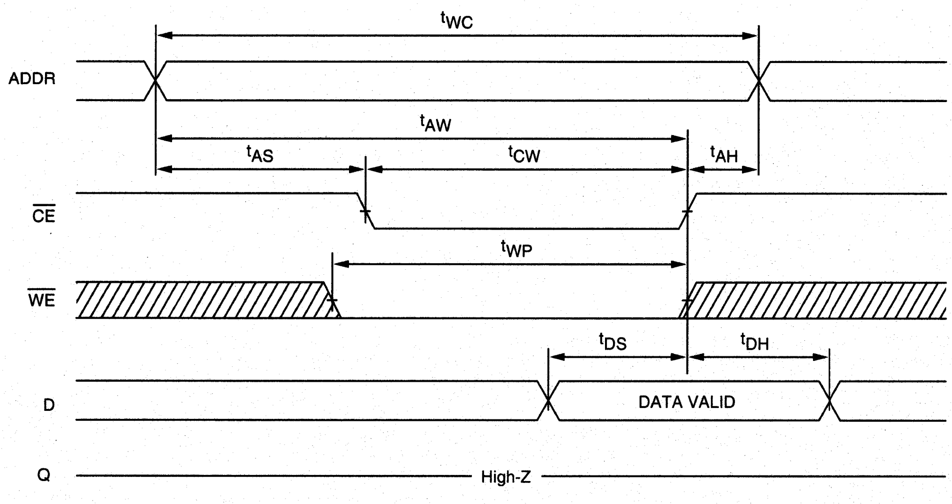
READ CYCLE NO. 2 [7, 8, 10]



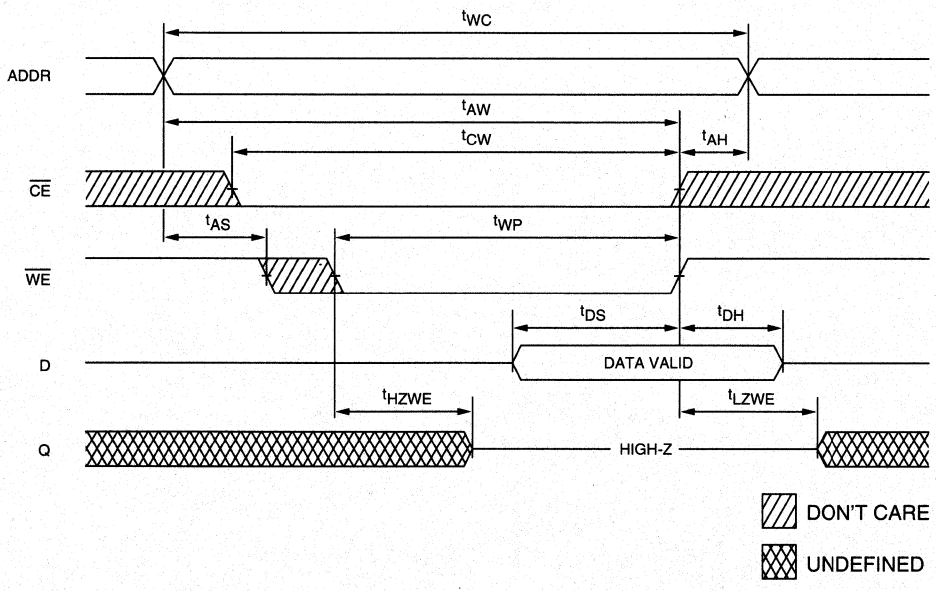
▨ DON'T CARE

▦ UNDEFINED

WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2
(Write Enable Controlled) 7, 12



SRAM

64K x 1 SRAM

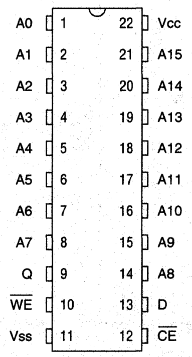
FEATURES

- High speed: 8, 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{\text{CE}}$ option
- All inputs and outputs are TTL compatible

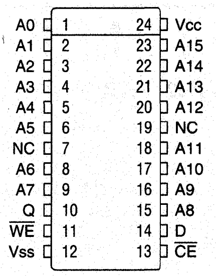
OPTIONS	MARKING
• Timing	
8ns access (preliminary)	- 8
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

22-Pin DIP
(A-6)



24-Pin SOJ
(E-4)



GENERAL DESCRIPTION

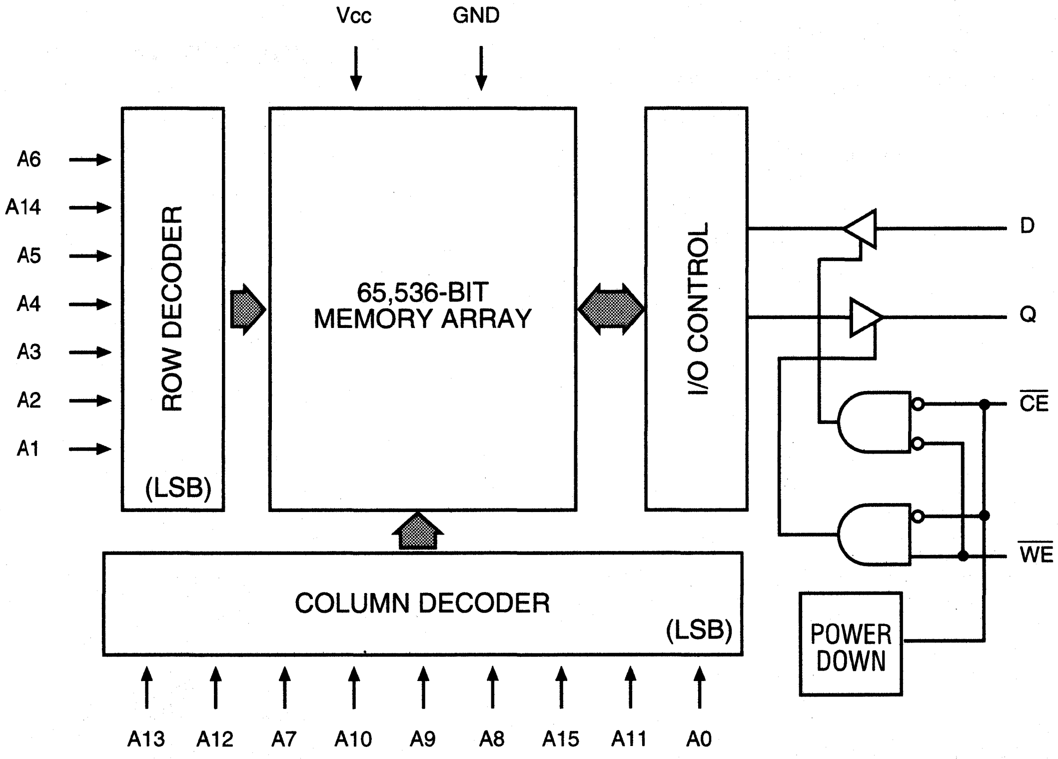
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{\text{CE}}$) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{\text{WE}}$) and $\overline{\text{CE}}$ inputs are both LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH and $\overline{\text{CE}}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ....-1V to +7V
Storage Temperature (Plastic) ....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX								
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-8**	**-10**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	160	150	140	120	110	100	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	55	50	45	40	35	30	25	mA	14
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IL} ≤ Vss +0.2V V_{IH} ≥ Vcc -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	3	3	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz	C_I	7	pF	4
Output Capacitance	Vcc = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle																	
READ cycle time	^tRC	8		10		12		15		20		25		35		ns	
Address access time	^tAA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^tACE		7		9		10		12		15		20		30	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		3		5		5		5		ns	
Chip disable to output in High-Z	^tHZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		8		10		12		15		20		25		35	ns	
WRITE Cycle																	
WRITE cycle time	^tWC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		9		10		12		15		20		25		ns	
Address valid to end of write	^tAW	8		9		11		12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		0		ns	
WRITE pulse width	^tWP	7		8		9		12		15		18		20		ns	
Data setup time	^tDS	5		6		7		8		10		10		12		ns	
Data hold time	^tDH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8		8	ns	6

*These specifications are preliminary.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

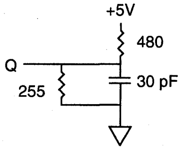


Fig. 1 OUTPUT LOAD EQUIVALENT

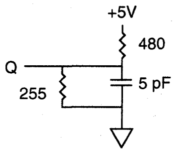


Fig. 2 OUTPUT LOAD EQUIVALENT

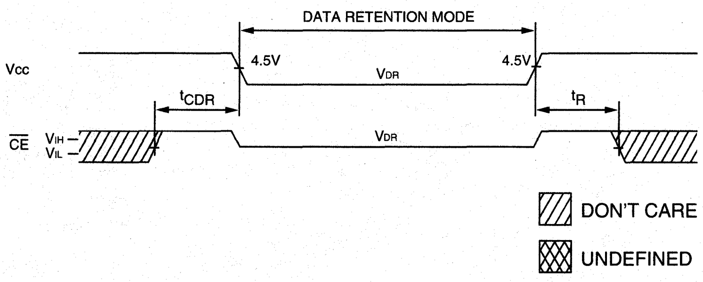
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-173.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

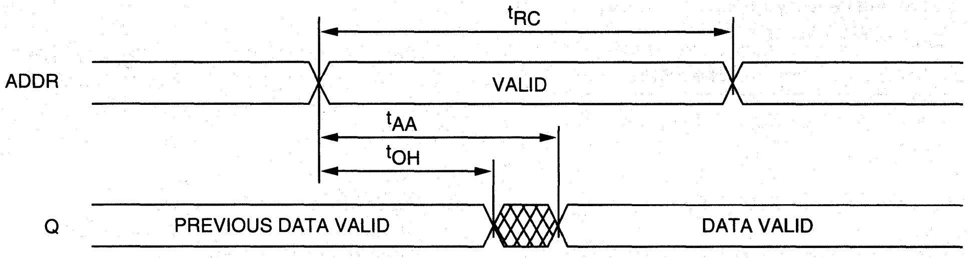
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{\text{CE}}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

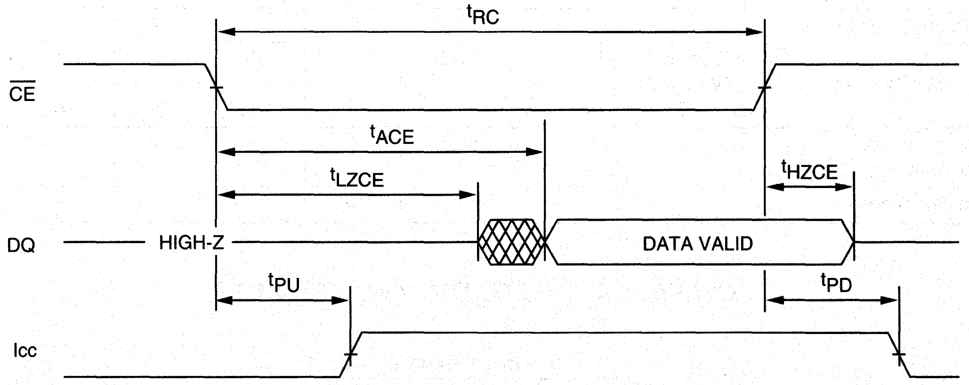
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1[8, 9]



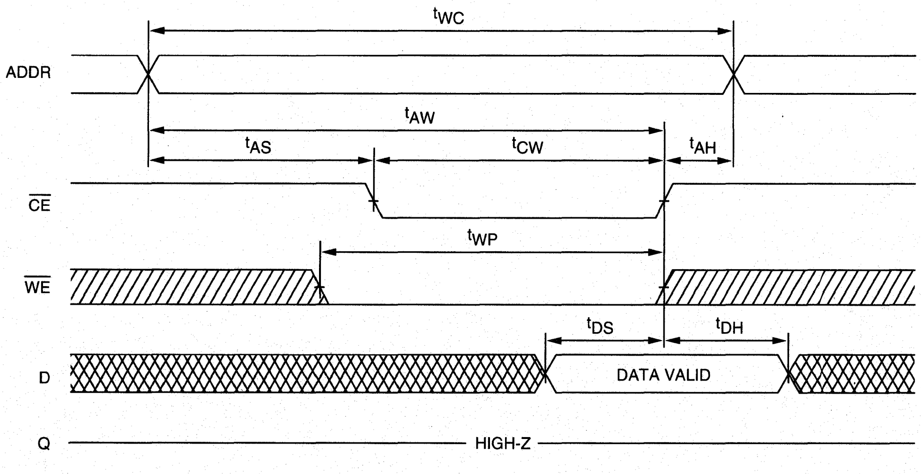
READ CYCLE NO. 2[7, 8, 10]



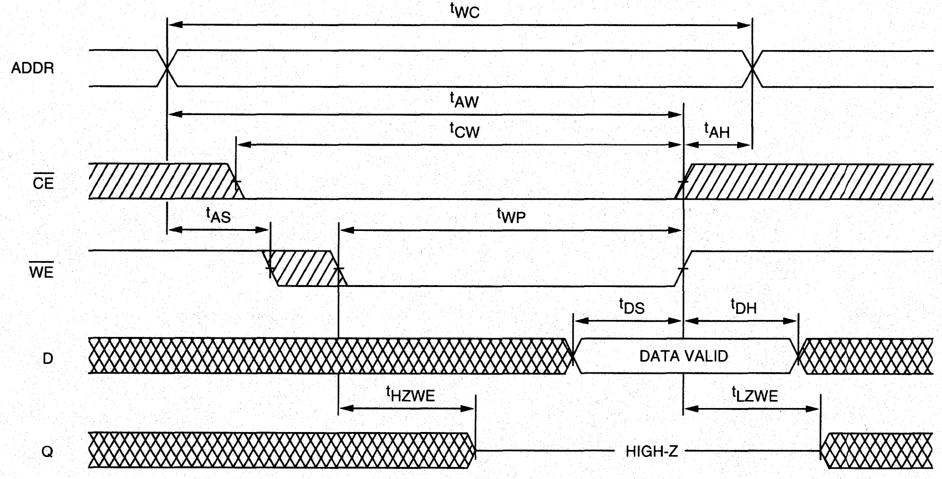
▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2
(Write Enable Controlled) 7, 12



▨ DON'T CARE

▩ UNDEFINED

SRAM

256K x 1 SRAM

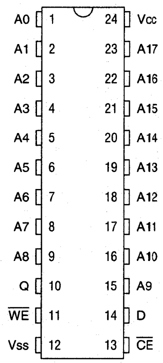
FEATURES

- High speed: 15, 20, 25, 30, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

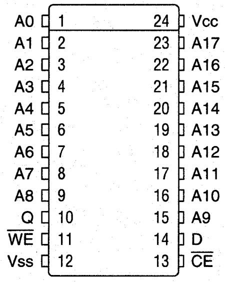
OPTIONS	MARKING
• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

24-Pin DIP
(A-7)



24-Pin SOJ
(E-4)



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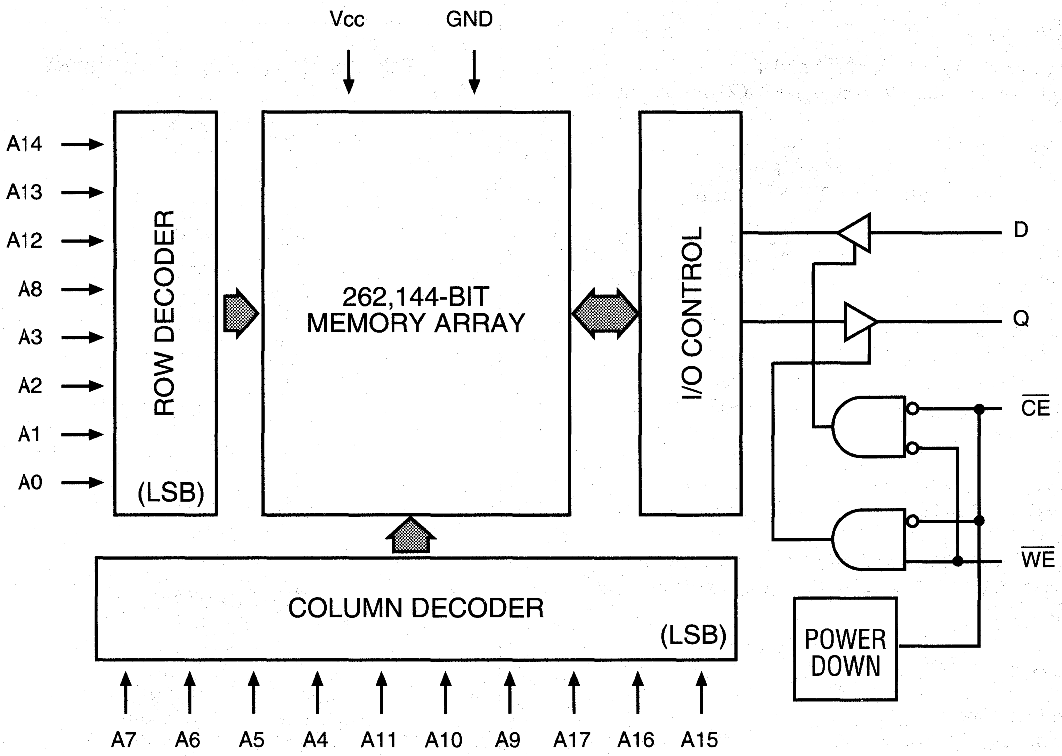
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	IL_I	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	IL_O	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX							
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-15**	**-20**	**-25**	**-30**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^{t}RC Outputs Open	Icc	75	140	120	110	95	90	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^{t}RC Outputs Open	I_{SB1}	11	30	30	25	25	25	25	mA	14
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IL} ≤ Vss +0.2V V_{IH} ≥ Vcc -0.2V; f = 0	I_{SB2}	.04	5	5	5	5	7	7	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	C_I	6	pF	4
Output Capacitance		C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \leq T_A \leq 70°C$; Vcc = 5V ±10%)

DESCRIPTION		-15		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^{t}RC	15		20		25		30		35		45		ns	
Address access time	^{t}AA		15		20		25		30		35		45	ns	
Chip Enable access time	^{t}ACE		15		20		25		30		35		45	ns	
Output hold from address change	^{t}OH	3		3		5		5		5		5		ns	
Chip Enable to output in Low-Z	^{t}LZCE	4		6		6		6		6		6		ns	
Chip disable to output in High-Z	^{t}HZCE		8		9		9		12		15		18	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		15		20		25		30		35		45	ns	
WRITE Cycle															
WRITE cycle time	^{t}WC	15		20		20		25		30		35		ns	
Chip Enable to end of write	^{t}CW	10		15		15		18		20		25		ns	
Address valid to end of write	^{t}AW	10		15		15		18		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		0		ns	
WRITE pulse width	^{t}WP	10		15		15		18		20		25		ns	
Data setup time	^{t}DS	7		10		10		12		15		20		ns	
Data hold time	^{t}DH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	4		5		5		5		5		5		ns	
Write Enable to output in High-Z	^{t}HZWE		7		10		10		12		15		18	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

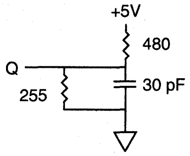


Fig. 1 OUTPUT LOAD EQUIVALENT

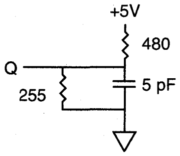


Fig. 2 OUTPUT LOAD EQUIVALENT

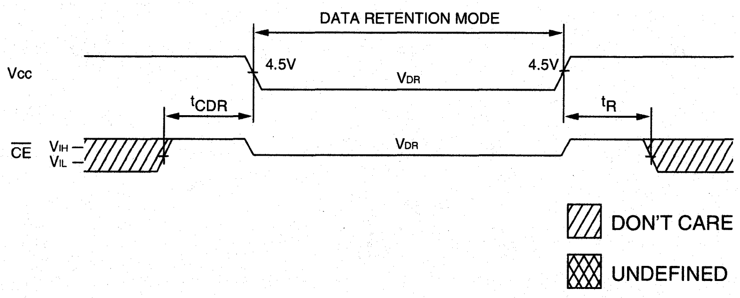
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-175.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

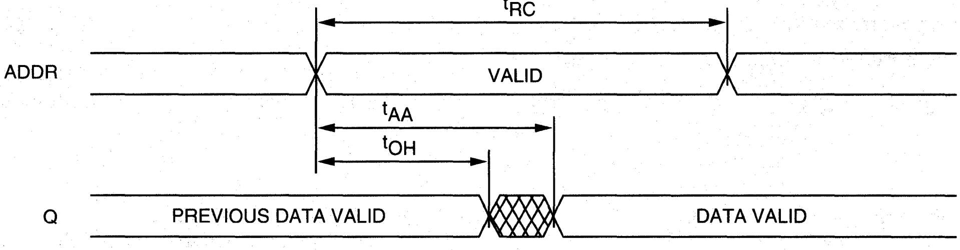
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		95	300	µA	
		Vcc = 3V			350	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

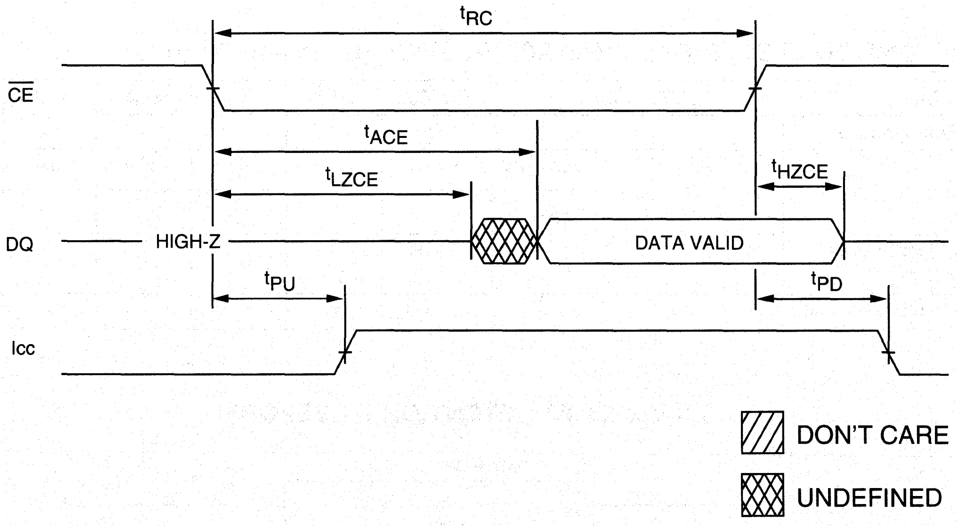
LOW Vcc DATA RETENTION WAVEFORM



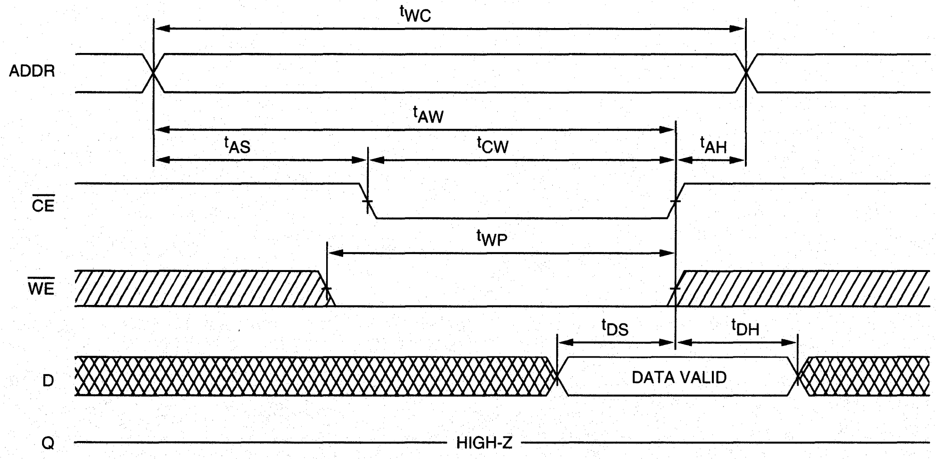
READ CYCLE NO. 1[8, 9]



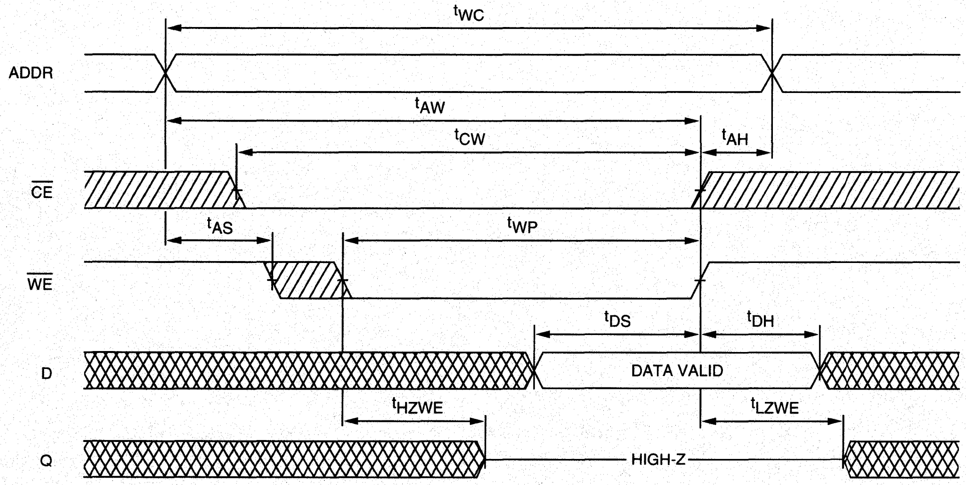
READ CYCLE NO. 2[7, 8, 10]



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2
(Write Enable Controlled)[7, 12]



▨ DON'T CARE

▦ UNDEFINED

SRAM

1 MEG x 1 SRAM

FEATURES

- High speed: 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

OPTIONS	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

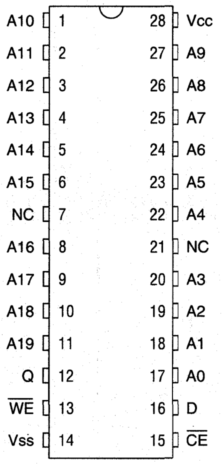
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

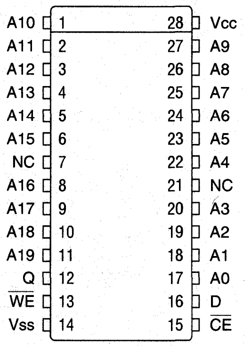
All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

PIN ASSIGNMENT (Top View)

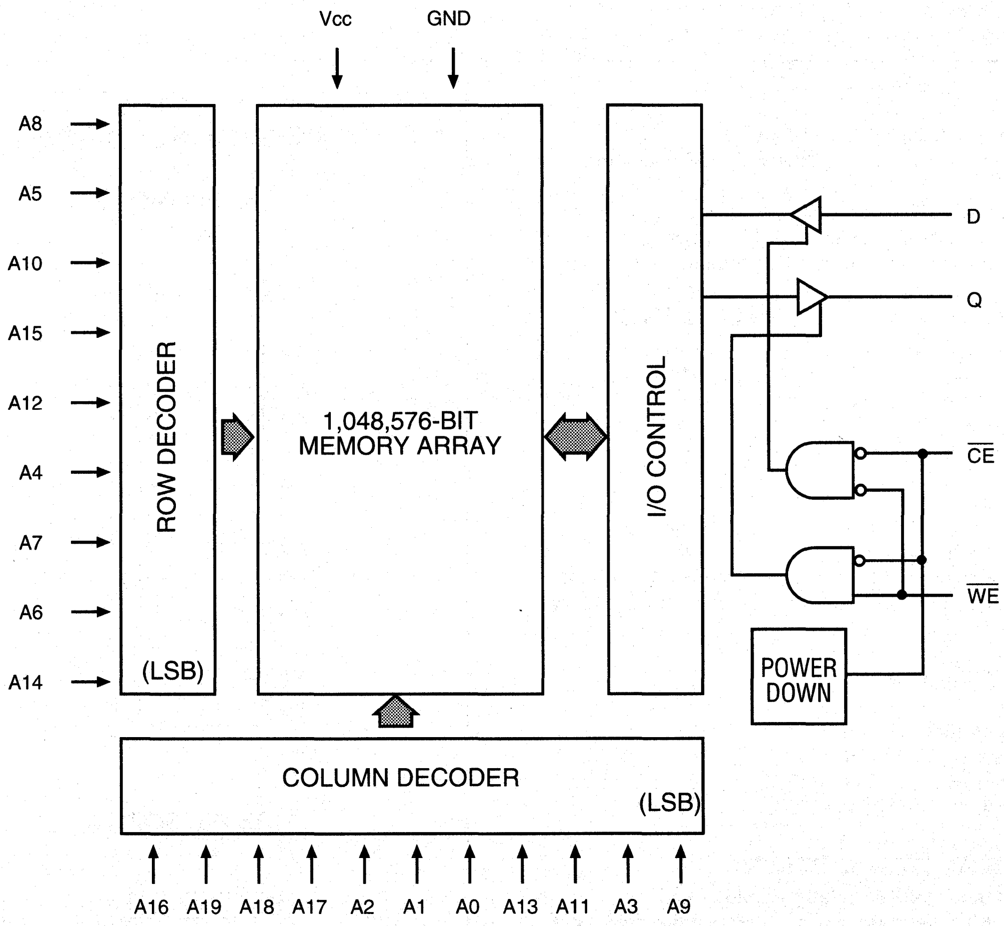
28-Pin DIP
(A-10)



28-Pin SOJ
(E-9)



FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A6 and A14) are encoded using a gray code.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS}	-1V to +7V
Storage Temperature (Plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = $1/{}^{t}RC$ Outputs Open	I_{CC}	95	140	125	115	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = $1/{}^{t}RC$ Outputs Open	I_{SB1}	17	35	30	25	25	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	14
"L" version only	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.3	1.5	1.5	1.5	1.5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	20		25		35		45		ns	
Address access time	^tAA		20		25		35		45	ns	
Chip Enable access time	^tACE		20		25		35		45	ns	
Output hold from address change	^tOH	5		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		5		ns	
Chip disable to output in High-Z	^tHZCE		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		20		25		35		45	ns	
WRITE Cycle											
WRITE cycle time	^tWC	20		25		35		45		ns	
Chip Enable to end of write	^tCW	12		15		20		25		ns	
Address valid to end of write	^tAW	12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	^tWP	12		15		20		25		ns	
Data setup time	^tDS	8		10		15		20		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	5		5		5		5		ns	
Write Enable to output in High-Z	^tHZWE	0	8	0	10	0	15	0	18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

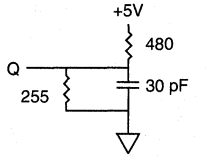


Fig. 1 OUTPUT LOAD EQUIVALENT

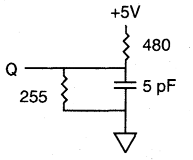


Fig. 2 OUTPUT LOAD EQUIVALENT

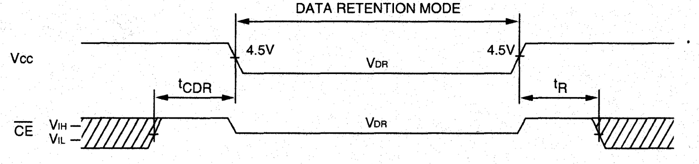
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-177.
14. Typical values are measured at 5V, 25°C and 25ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{\text{CE}}$ ≥ (Vcc -0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		35	200	µA	
		Vcc = 3V			70	400	µA	
		Vcc = 5V			250	1,300	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

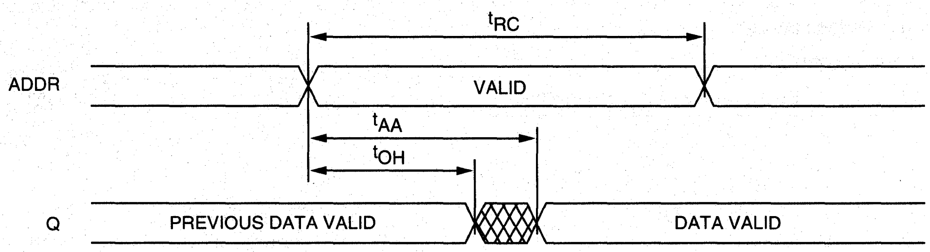
LOW Vcc DATA RETENTION WAVEFORM



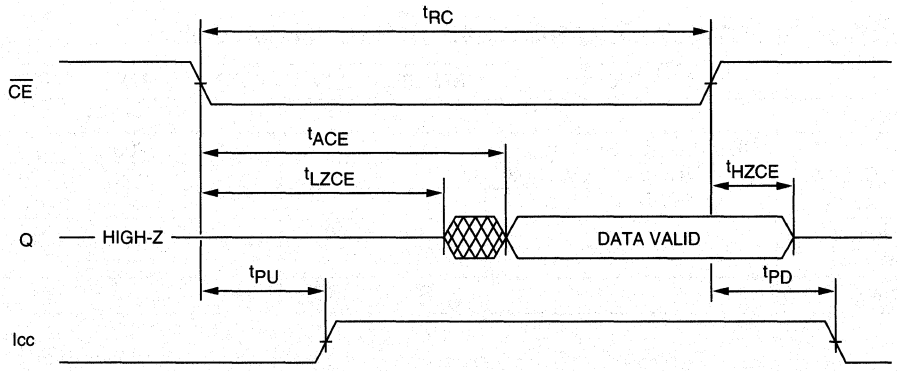
▨ DON'T CARE

▩ UNDEFINED

READ CYCLE NO. 1 [8, 9]



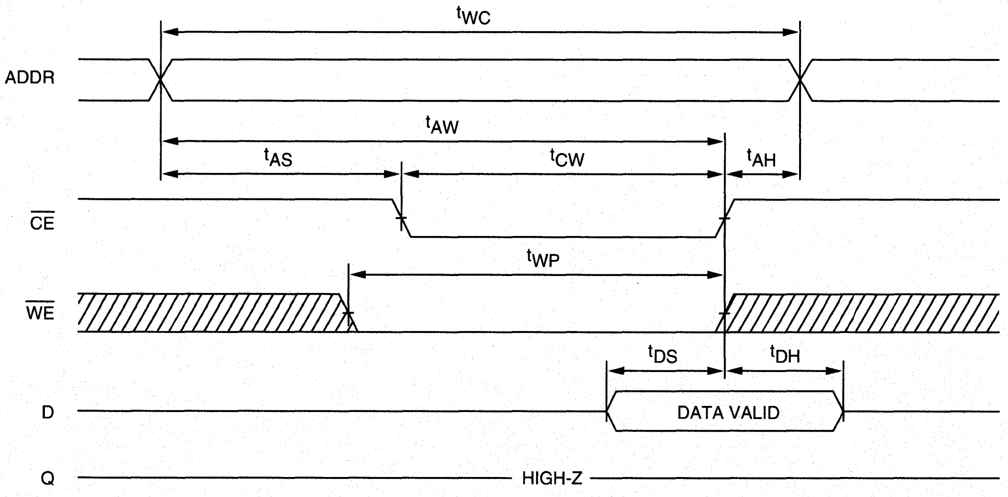
READ CYCLE NO. 2 [7, 8, 10]



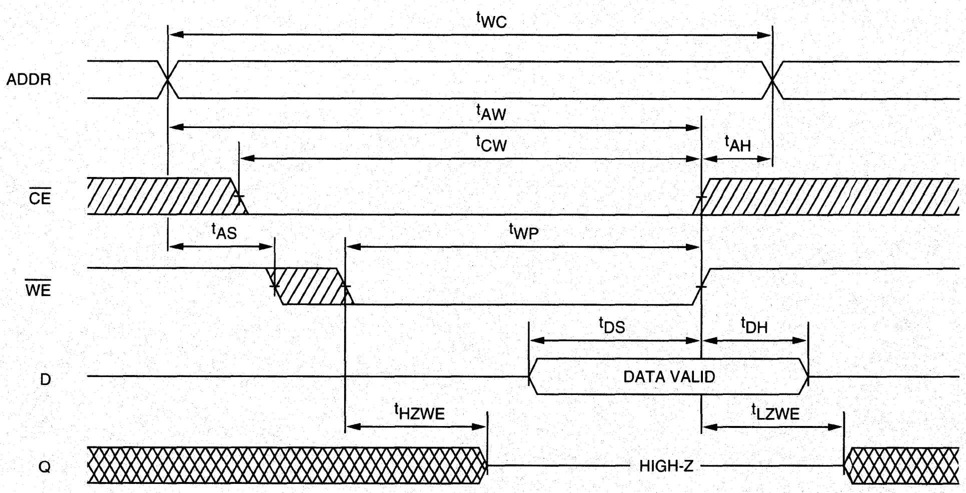
▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 1
(Chip Enable Controlled) 12



WRITE CYCLE NO. 2
(Write Enable Controlled) 7, 12



▨ DON'T CARE

▩ UNDEFINED

MICRON TECHNOLOGY, INC. **MT5C1604**

SRAM

4K x 4 SRAM

FEATURES

- High speed: 8, 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{\text{CE}}$ option
- All inputs and outputs are TTL compatible

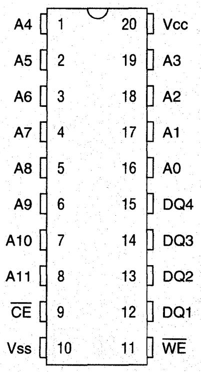
OPTIONS

OPTIONS	MARKING
• Timing	
8ns access (preliminary)	- 8
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

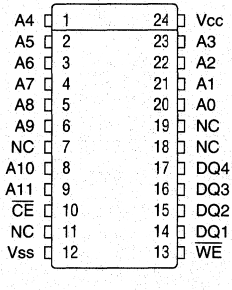
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***

PIN ASSIGNMENT (Top View)

20-Pin DIP
(A-4)



24-Pin SOJ
(E-4)



GENERAL DESCRIPTION

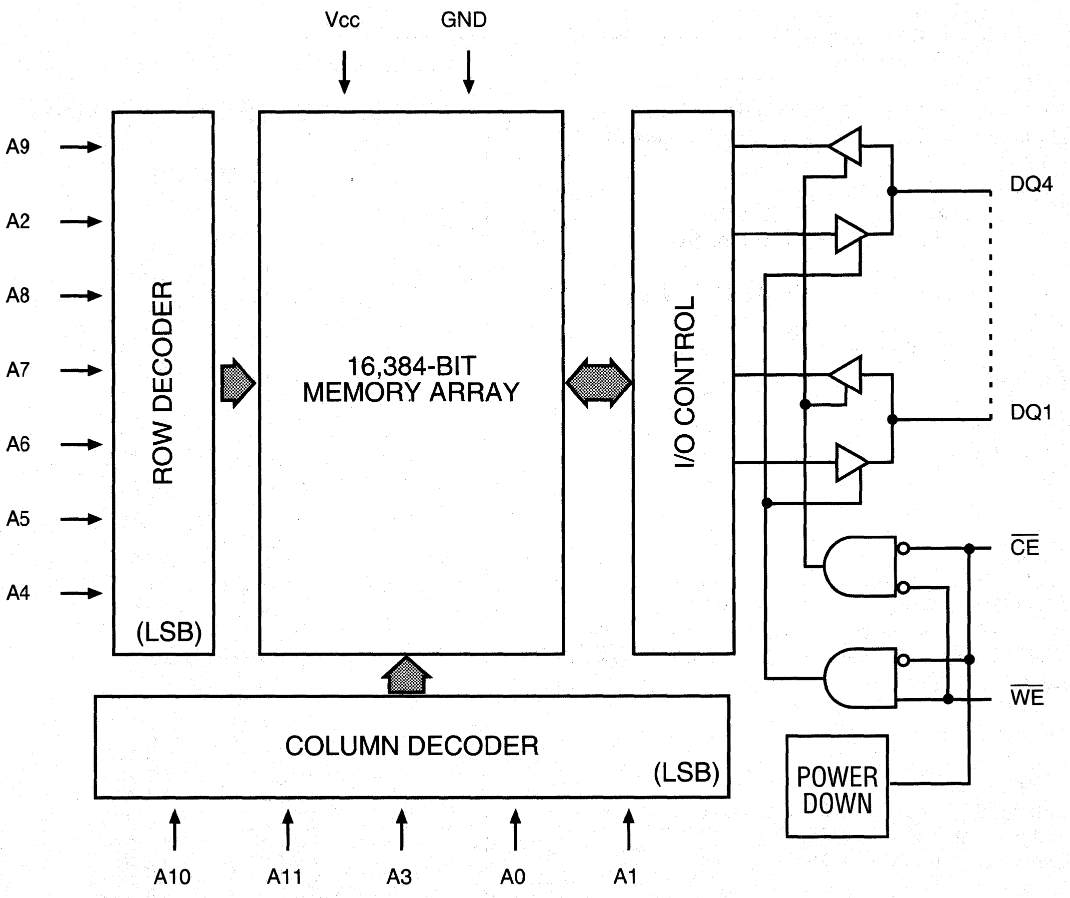
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{\text{CE}}$) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{\text{WE}}$) and $\overline{\text{CE}}$ inputs are both LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH and $\overline{\text{CE}}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	CE	WE	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX								
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-8**	**-10**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	160	150	140	120	110	100	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	55	50	45	40	35	30	25	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	3	3	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Output Capacitance		C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle																	
READ cycle time	^{t}RC	8		10		12		15		20		25		35		ns	
Address access time	^{t}AA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^{t}ACE		7		9		10		12		15		20		30	ns	
Output hold from address change	^{t}OH	3		3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^{t}LZCE	2		2		2		3		5		5		5		ns	
Chip disable to output in High-Z	^{t}HZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		8		10		12		15		20		25		35	ns	
WRITE Cycle																	
WRITE cycle time	^{t}WC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^{t}CW	8		9		10		12		15		20		25		ns	
Address valid to end of write	^{t}AW	8		9		11		12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		0		0		ns	
WRITE pulse width	^{t}WP1	7		8		9		12		15		18		20		ns	
WRITE pulse width	^{t}WP2	8		9		10		14		18		20		25		ns	
Data setup time	^{t}DS	5		6		7		8		10		10		12		ns	
Data hold time	^{t}DH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	2		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^{t}HZWE		4		5		5		6		8		8		8	ns	6

*These specifications are preliminary.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

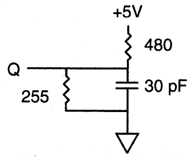


Fig. 1 OUTPUT LOAD EQUIVALENT

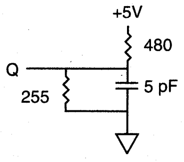


Fig. 2 OUTPUT LOAD EQUIVALENT

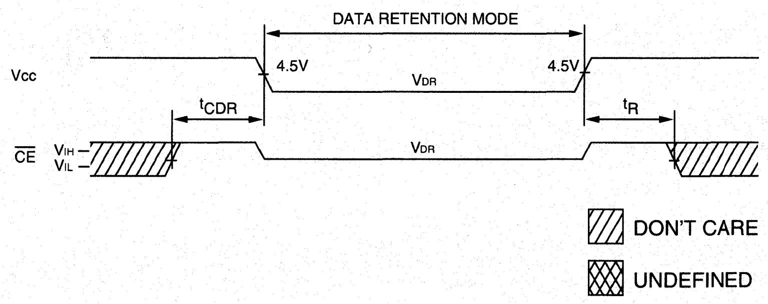
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-171.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

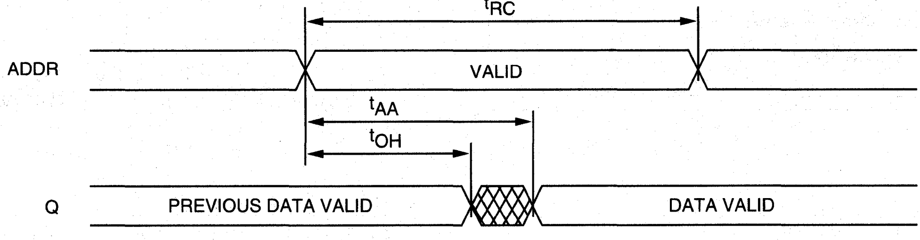
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

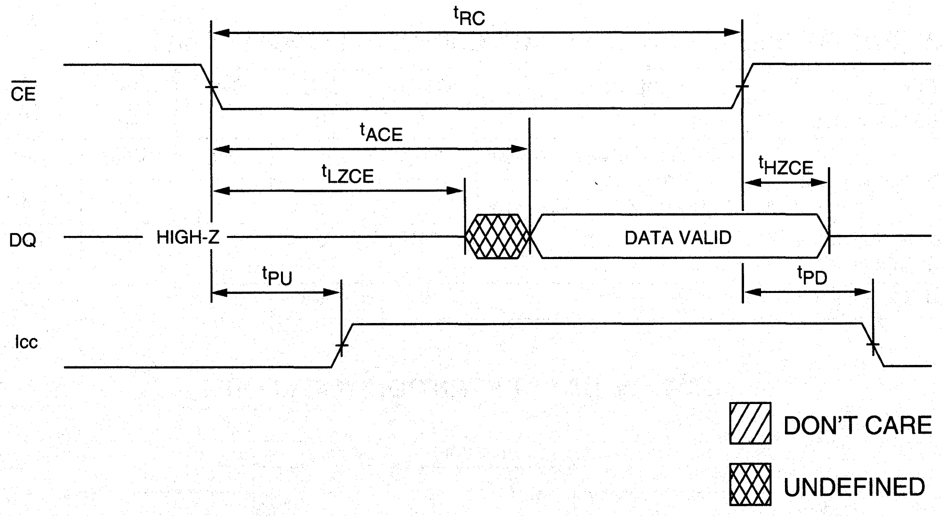
LOW Vcc DATA RETENTION WAVEFORM



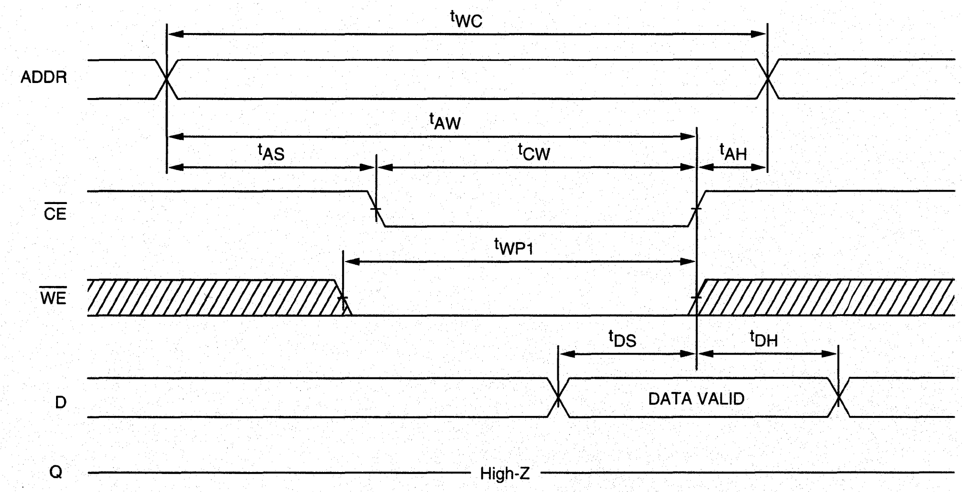
READ CYCLE NO. 1 [8, 9]



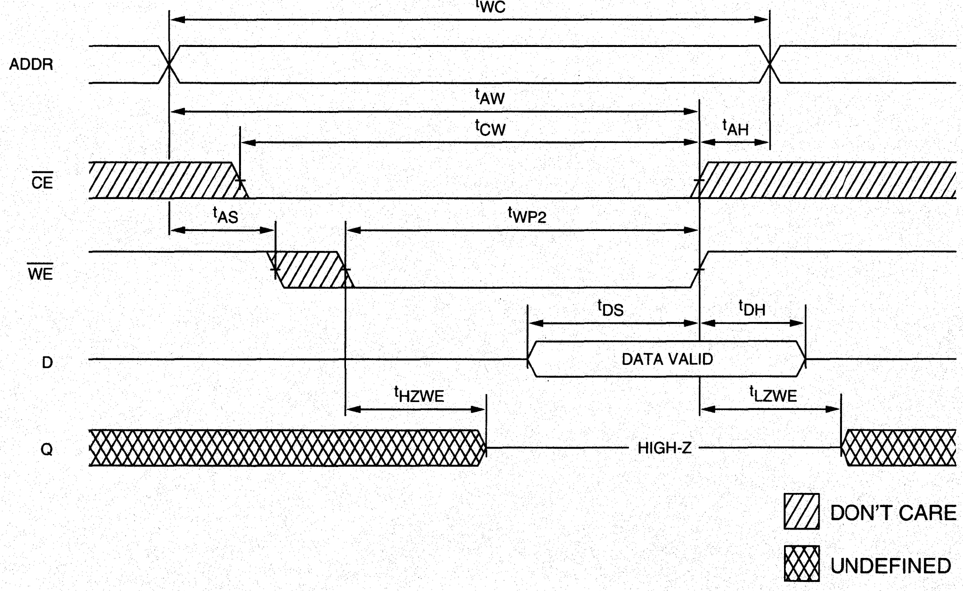
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2
(Write Enable Controlled) [7, 12]



MICRON
TECHNOLOGY, INC.

MT5C1605

SRAM

4K x 4 SRAM

WITH OUTPUT ENABLE

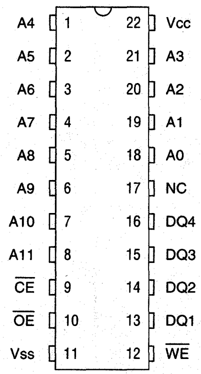
FEATURES

- High speed: 8, 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

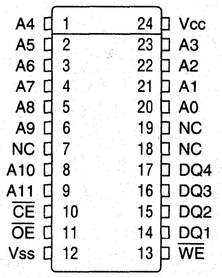
OPTIONS	MARKING
• Timing	
8ns access (preliminary)	- 8
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

22-Pin DIP
(A-6)



24-Pin SOJ
(E-4)



GENERAL DESCRIPTION

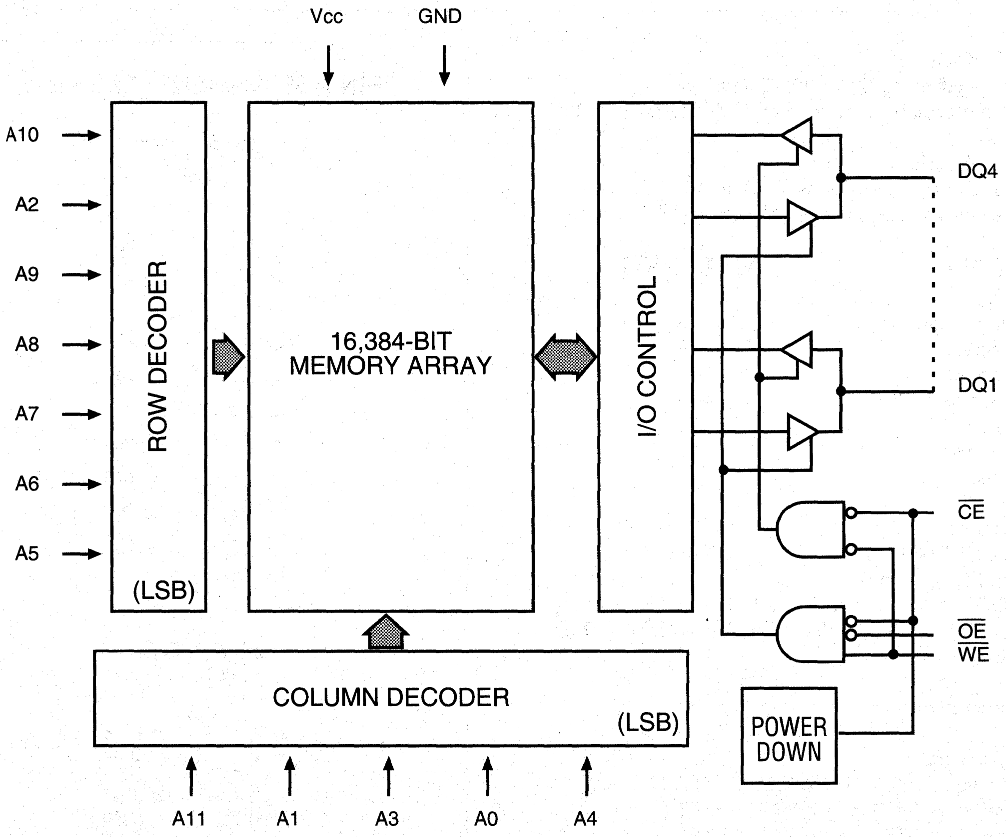
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ....-1V to +7V
Storage Temperature (Plastic) ....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ Vcc	ILI	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ VOUT ≤ Vcc	ILO	-5	5	µA	
Output High Voltage	IOH = -4.0mA	VOH	2.4		V	1
Output Low Voltage	IOL = 8.0mA	VOL		0.4	V	1

				MAX								
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-8**	**-10**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ VIL; Vcc = MAX f = MAX = 1/ ^{t}RC Outputs Open	Icc	65	160	150	140	120	110	100	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ VIH; Vcc = MAX f = MAX = 1/ ^{t}RC Outputs Open	ISB1	20	55	50	45	40	35	30	25	mA	14
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX VIL ≤ Vss +0.2V VIH ≥ Vcc -0.2V; f = 0	ISB2	0.4	3	3	3	3	3	3	3	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	CI	5	pF	4
Output Capacitance		Co	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C $\leq T_A \leq$ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle																	
READ cycle time	^tRC	8		10		12		15		20		25		35		ns	
Address access time	^tAA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^tACE		7		9		10		12		15		20		30	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		3		5		5		5		ns	
Chip disable to output in High-Z	^tHZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		8		10		12		15		20		25		35	ns	
Output Enable access time	^tAOE		3		4		5		6		7		8		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4		4		5		6		7		8		8	ns	6
WRITE Cycle																	
WRITE cycle time	^tWC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		9		10		12		15		20		25		ns	
Address valid to end of write	^tAW	8		9		11		12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	7		8		9		12		15		18		20		ns	
WRITE pulse width	$^tWP2$	8		9		10		14		18		20		25		ns	
Data setup time	^tDS	5		6		7		8		10		10		12		ns	
Data hold time	^tDH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8		8	ns	6

*These specifications are preliminary.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

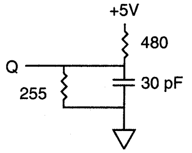


Fig. 1 OUTPUT LOAD EQUIVALENT

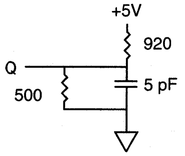


Fig. 2 OUTPUT LOAD EQUIVALENT

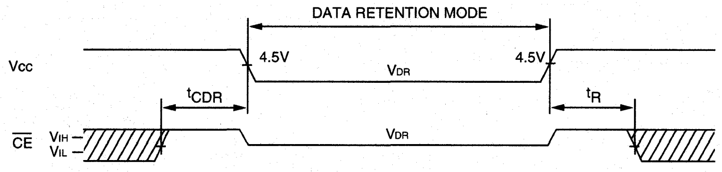
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-171.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{\text{CE}}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

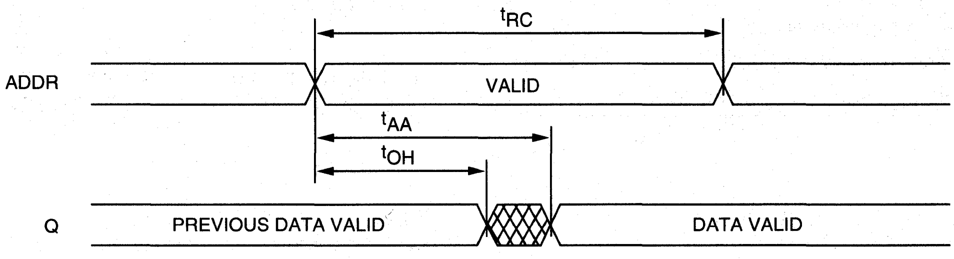
LOW Vcc DATA RETENTION WAVEFORM



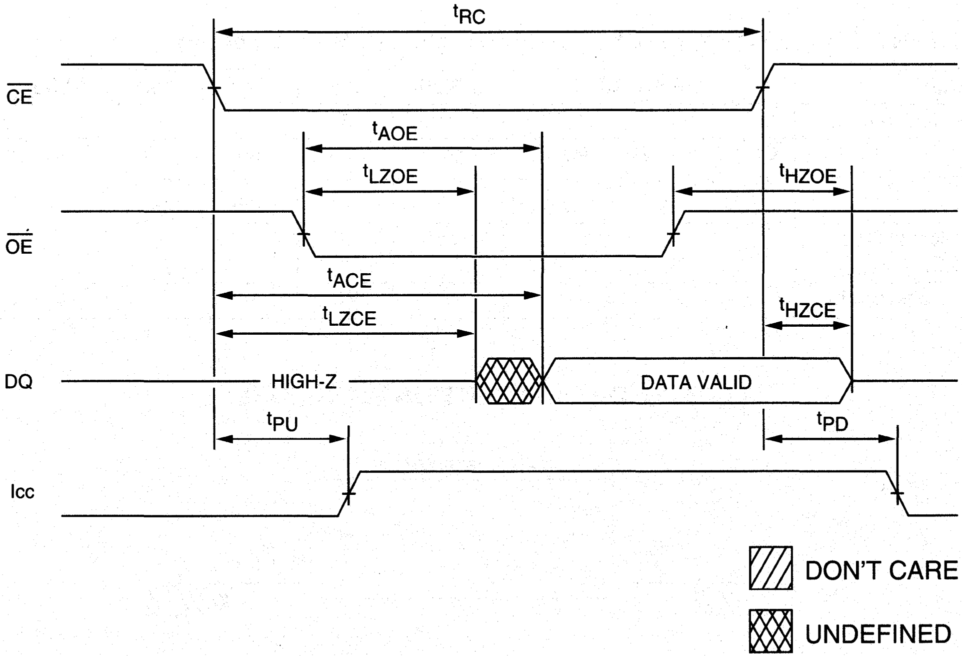
▨ DON'T CARE

▩ UNDEFINED

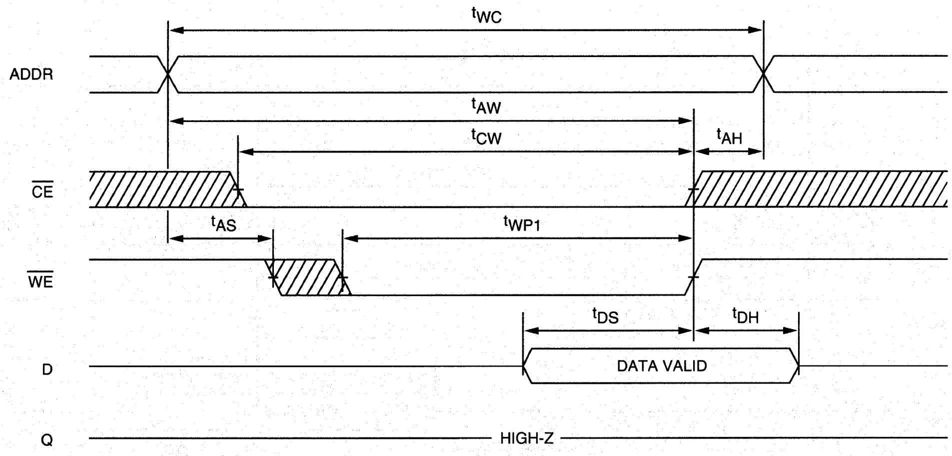
READ CYCLE NO. 1[8,9]



READ CYCLE NO. 2[7,8,10]

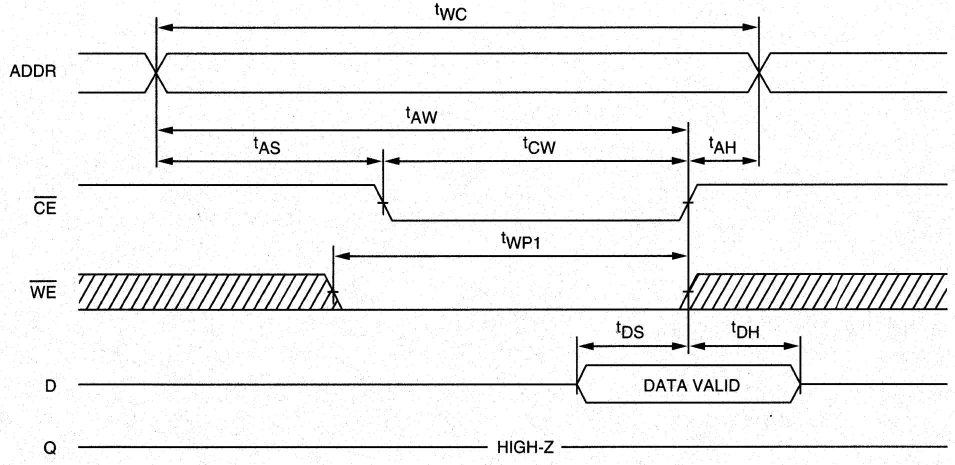


WRITE CYCLE NO. 1
(Write Enable Controlled)[12]



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 2
(Chip Enable Controlled)

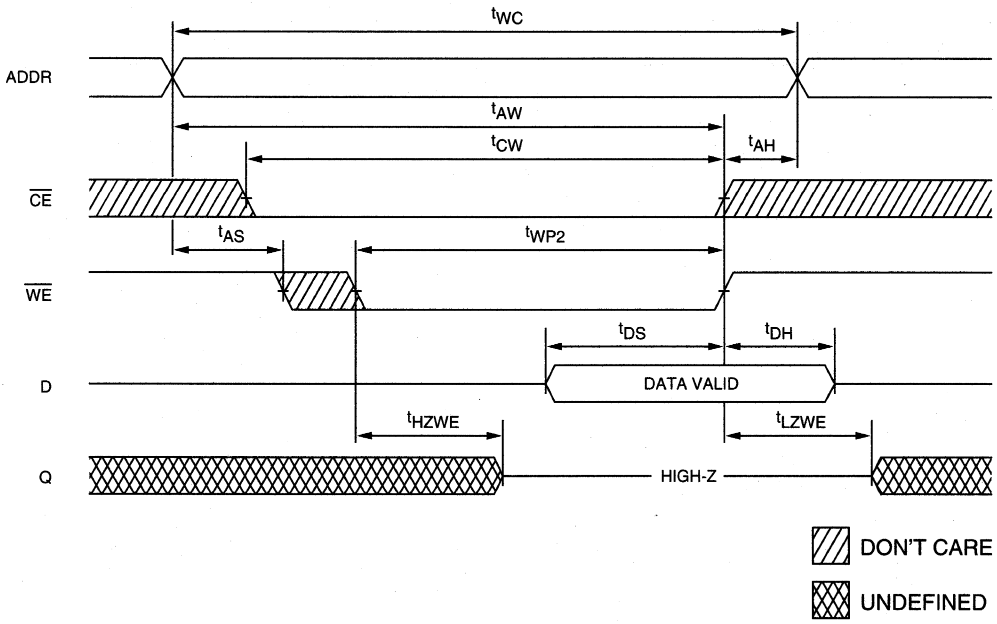


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 3

(Write Enable Controlled) 7, 12



4K x 4 SRAM

WITH SEPARATE INPUTS AND OUTPUTS

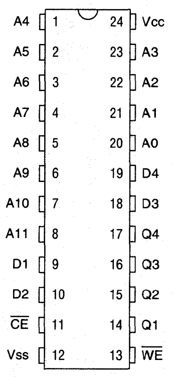
FEATURES

- High speed: 8, 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{\text{CE}}$ option
- All inputs and outputs are TTL compatible
- MT5C1606 – output tracks input during WRITE
- MT5C1607 – output is High-Z during WRITE

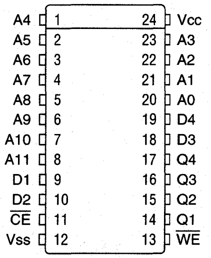
OPTIONS	MARKING
• Timing	
8ns access (preliminary)	- 8
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

24-Pin DIP
(A-7)



24-Pin SOJ
(E-4)



GENERAL DESCRIPTION

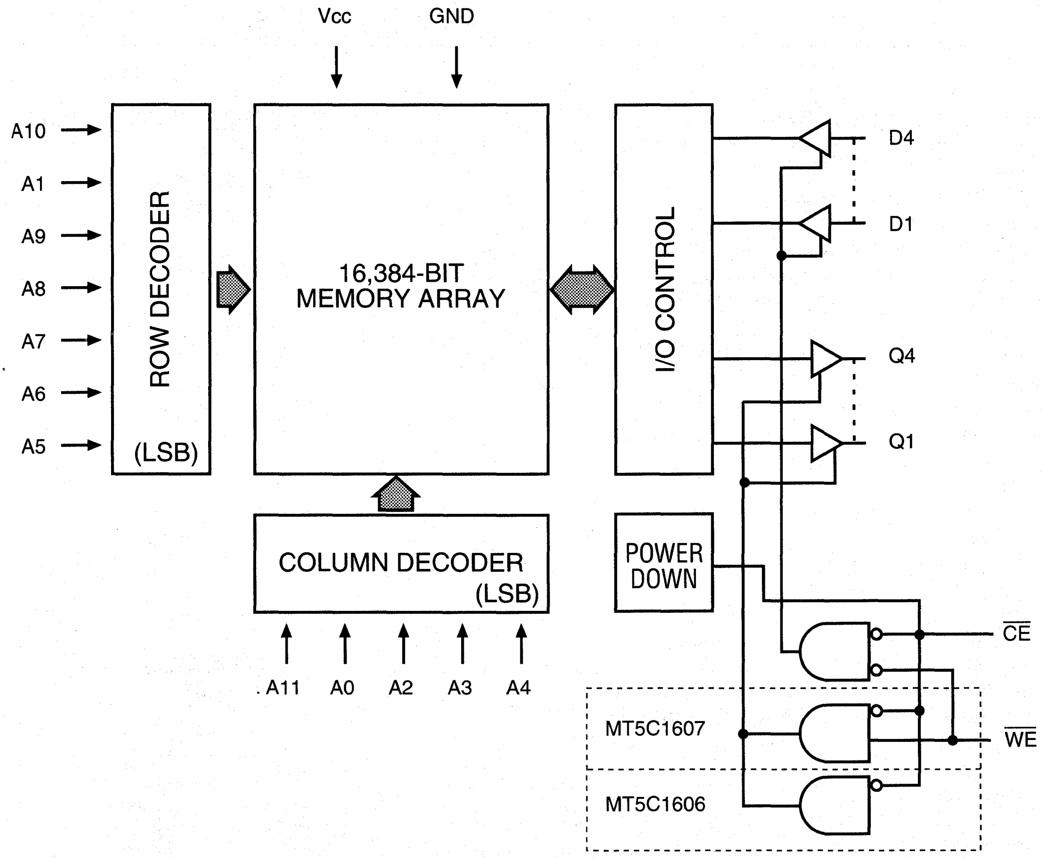
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{\text{CE}}$) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x4 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{\text{WE}}$) and $\overline{\text{CE}}$ inputs are both LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH and $\overline{\text{CE}}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE (1)	L	L	HIGH-Z	ACTIVE
WRITE (2)	L	L	D	ACTIVE

NOTE: 1. MT5C1607 ONLY
2. MT5C1606 ONLY

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS}	-1V to +7V
Storage Temperature (Plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX								
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-8	-10	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ${}^tRC$ Outputs Open	I_{CC}	65	160	150	140	120	110	100	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ${}^tRC$ Outputs Open	I_{SB1}	20	55	50	45	40	35	30	25	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	3	3	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Output Capacitance		C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	^tRC	8		10		12		15		20		25		35		ns	
Address access time	^tAA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^tACE		7		9		10		12		15		20		30	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		3		5		5		5		ns	
Chip disable to output in High-Z	^tHZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		8		10		12		15		20		25		35	ns	
WRITE Cycle																	
WRITE cycle time	^tWC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		9		10		12		15		20		25		ns	
Address valid to end of write	^tAW	8		9		11		12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		0		ns	
WRITE pulse width	^tWP	7		8		9		12		15		18		20		ns	
Data setup time	^tDS	5		6		7		8		10		10		12		ns	
Data hold time	^tDH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8		8	ns	6
Write Enable to output valid	^tAWE		10		12		14		17		20		25		35	ns	
Data valid to output valid	^tADV		10		12		14		17		20		25		35	ns	

*These specifications are preliminary.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

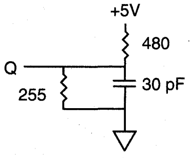


Fig. 1 OUTPUT LOAD EQUIVALENT

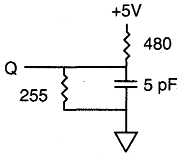


Fig. 2 OUTPUT LOAD EQUIVALENT

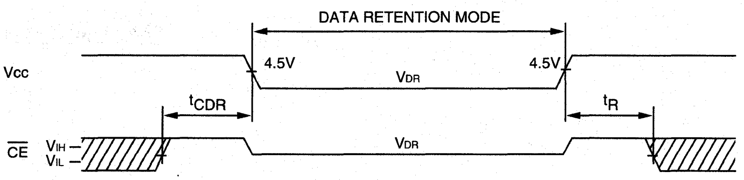
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-171.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{\text{CE}}$ ≥ (Vcc -0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

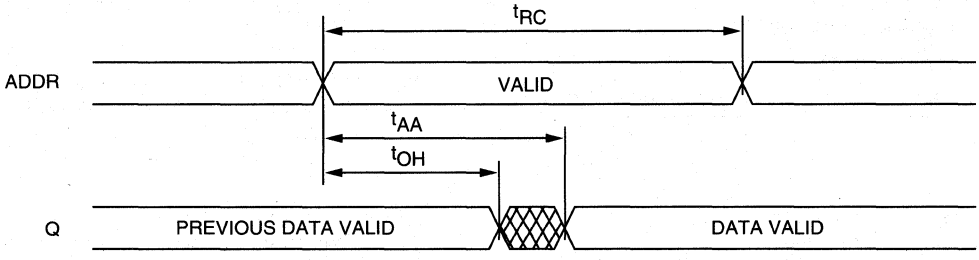
LOW Vcc DATA RETENTION WAVEFORM



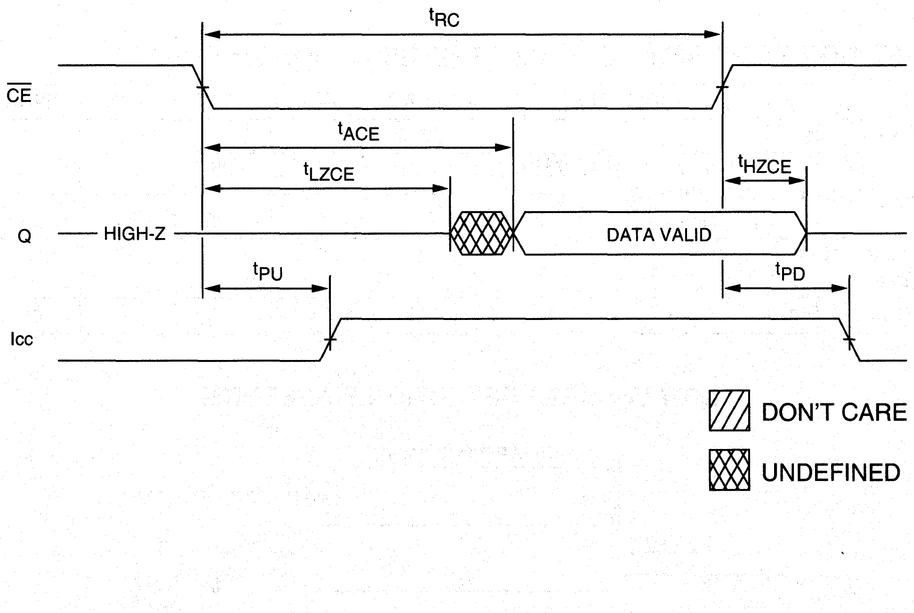
▨ DON'T CARE

▩ UNDEFINED

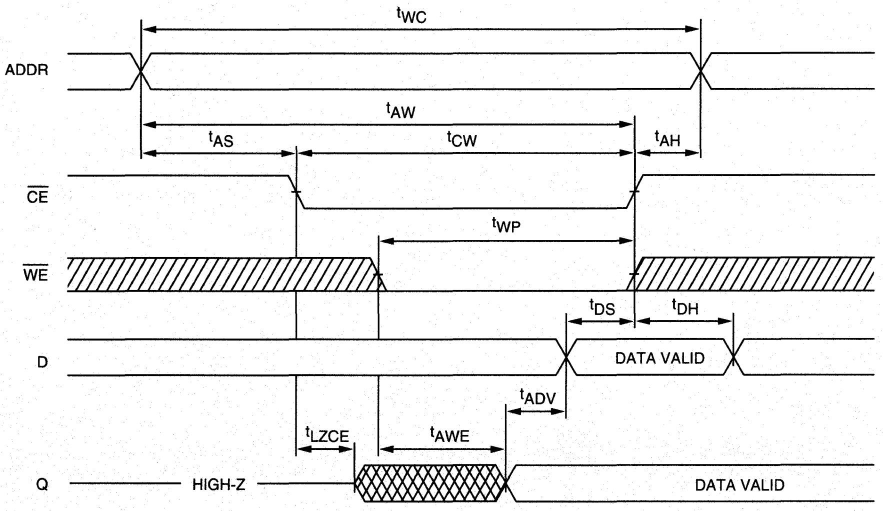
READ CYCLE NO. 1 [8, 9]



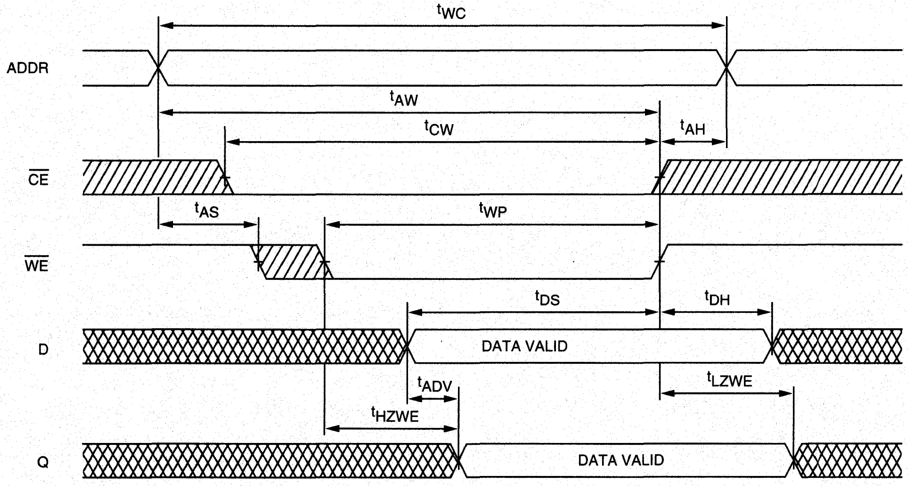
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2
(Write Enable Controlled)[7, 12]



▨ DON'T CARE

▩ UNDEFINED

SRAM

16K x 4 SRAM

FEATURES

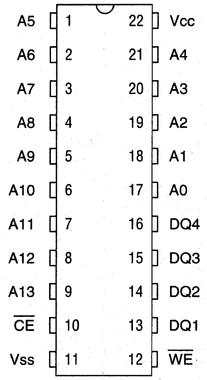
- High speed: 8, 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{\text{CE}}$ option
- All inputs and outputs are TTL compatible

OPTIONS

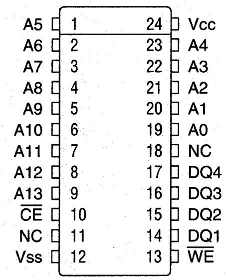
OPTIONS	MARKING
• Timing	
8ns access (preliminary)	- 8
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

22-Pin DIP
(A-6)



24-Pin SOJ
(E-4)



GENERAL DESCRIPTION

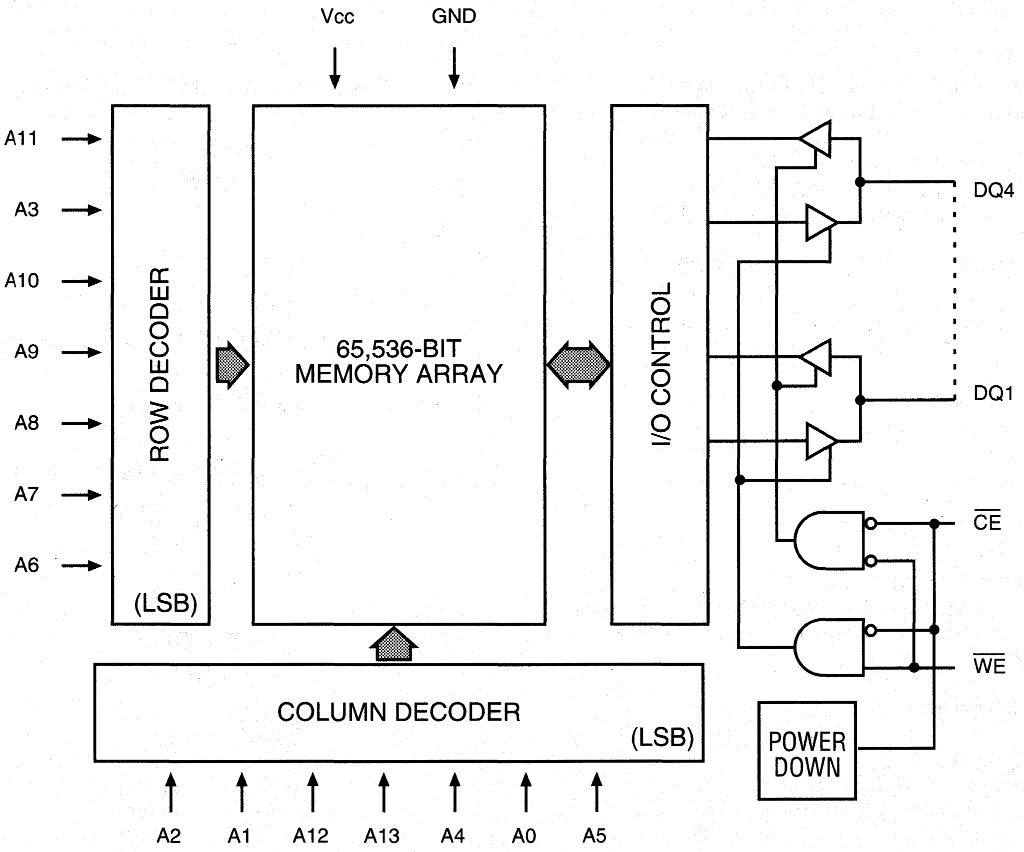
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{\text{CE}}$) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{\text{WE}}$) and $\overline{\text{CE}}$ inputs are both LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH and $\overline{\text{CE}}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve thier low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX								
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-8	-10	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	160	150	140	120	110	100	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	55	50	45	40	35	30	25	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	3	3	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Output Capacitance		C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYM	-8* MIN	-8* MAX	-10 MIN	-10 MAX	-12 MIN	-12 MAX	-15 MIN	-15 MAX	-20 MIN	-20 MAX	-25 MIN	-25 MAX	-35 MIN	-35 MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	^{t}RC	8		10		12		15		20		25		35		ns	
Address access time	^{t}AA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^{t}ACE		7		9		10		12		15		20		30	ns	
Output hold from address change	^{t}OH	3		3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^{t}LZCE	2		2		2		3		5		5		5		ns	
Chip disable to output in High-Z	^{t}HZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		8		10		12		15		20		25		35	ns	
WRITE Cycle																	
WRITE cycle time	^{t}WC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^{t}CW	8		9		10		12		15		20		25		ns	
Address valid to end of write	^{t}AW	8		9		11		12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		0		0		ns	
WRITE pulse width	^{t}WP1	7		8		9		12		15		18		20		ns	
WRITE pulse width	^{t}WP2	8		9		10		14		18		20		25		ns	
Data setup time	^{t}DS	5		6		7		8		10		10		12		ns	
Data hold time	^{t}DH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	2		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^{t}HZWE		4		5		5		6		8		8		8	ns	6

*These specifications are preliminary.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

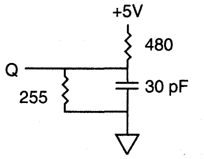


Fig. 1 OUTPUT LOAD EQUIVALENT

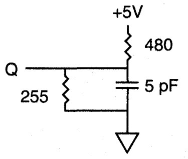


Fig. 2 OUTPUT LOAD EQUIVALENT

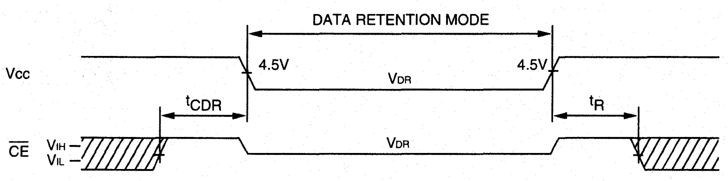
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-173.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{\text{CE}}$ ≥ (Vcc -0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

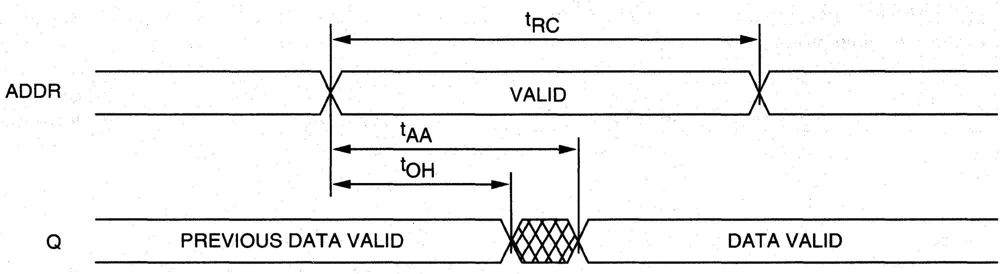
LOW Vcc DATA RETENTION WAVEFORM



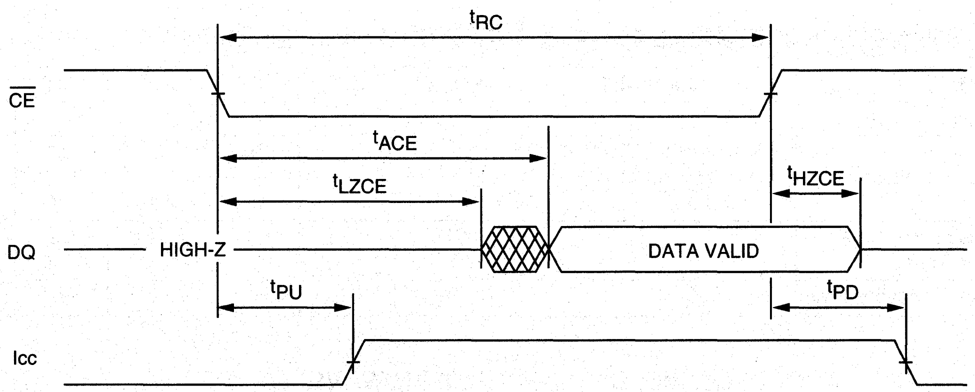
▨ DON'T CARE

▩ UNDEFINED

READ CYCLE NO. 1 [8, 9]



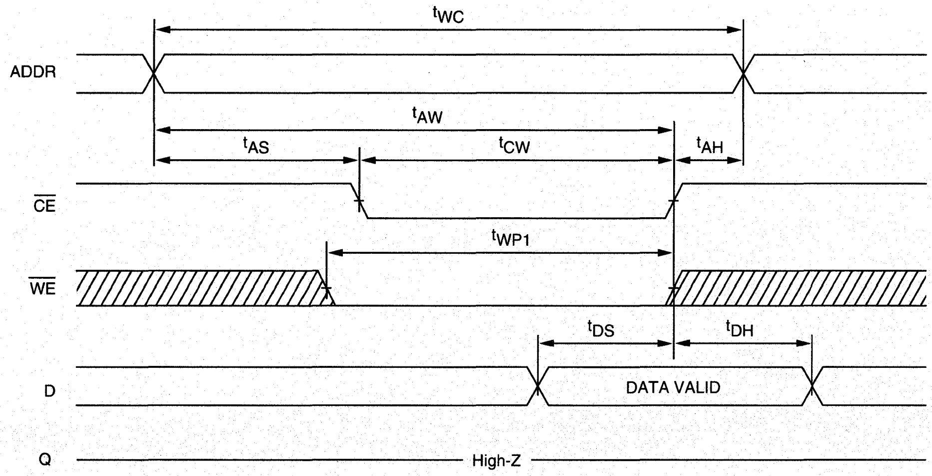
READ CYCLE NO. 2 [7, 8, 10]



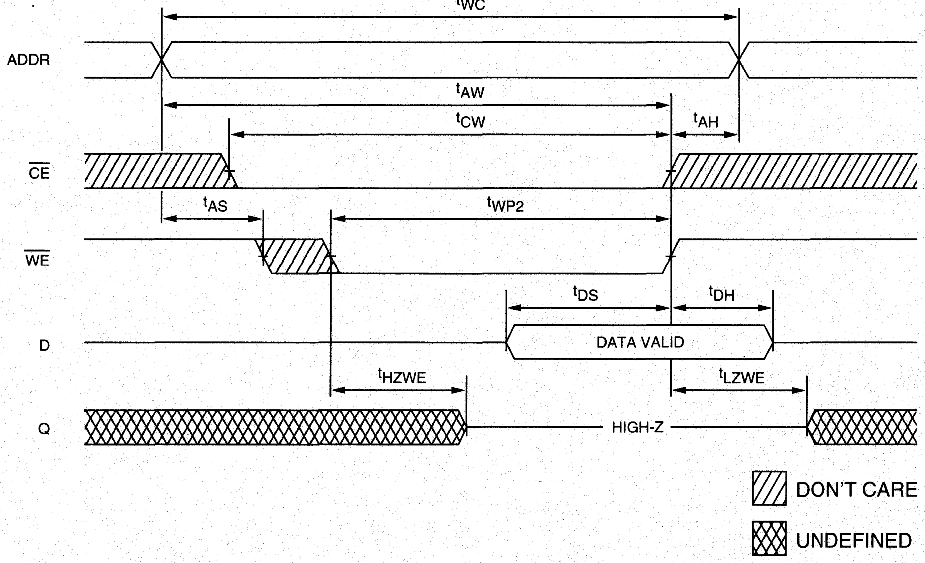
▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2
(Write Enable Controlled)[7, 12]



MICRON
TECHNOLOGY, INC.

MT5C6405

SRAM

16K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 8, 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ options
- All inputs and outputs are TTL compatible

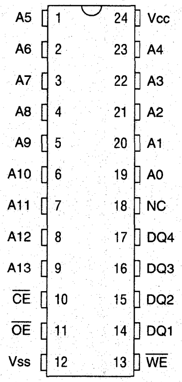
OPTIONS / MARKING

OPTIONS		MARKING
• Timing		
8ns access (preliminary)		- 8
10ns access		-10
12ns access		-12
15ns access		-15
20ns access		-20
25ns access		-25
35ns access		-35
• Packages		
Plastic DIP (300 mil)		None
Plastic SOJ (300 mil)		DJ
• 2V data retention		L
• Temperature		
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

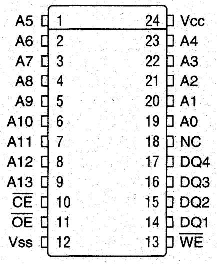
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***

PIN ASSIGNMENT (Top View)

24-Pin DIP
(A-7)



24-Pin SOJ
(E-4)



GENERAL DESCRIPTION

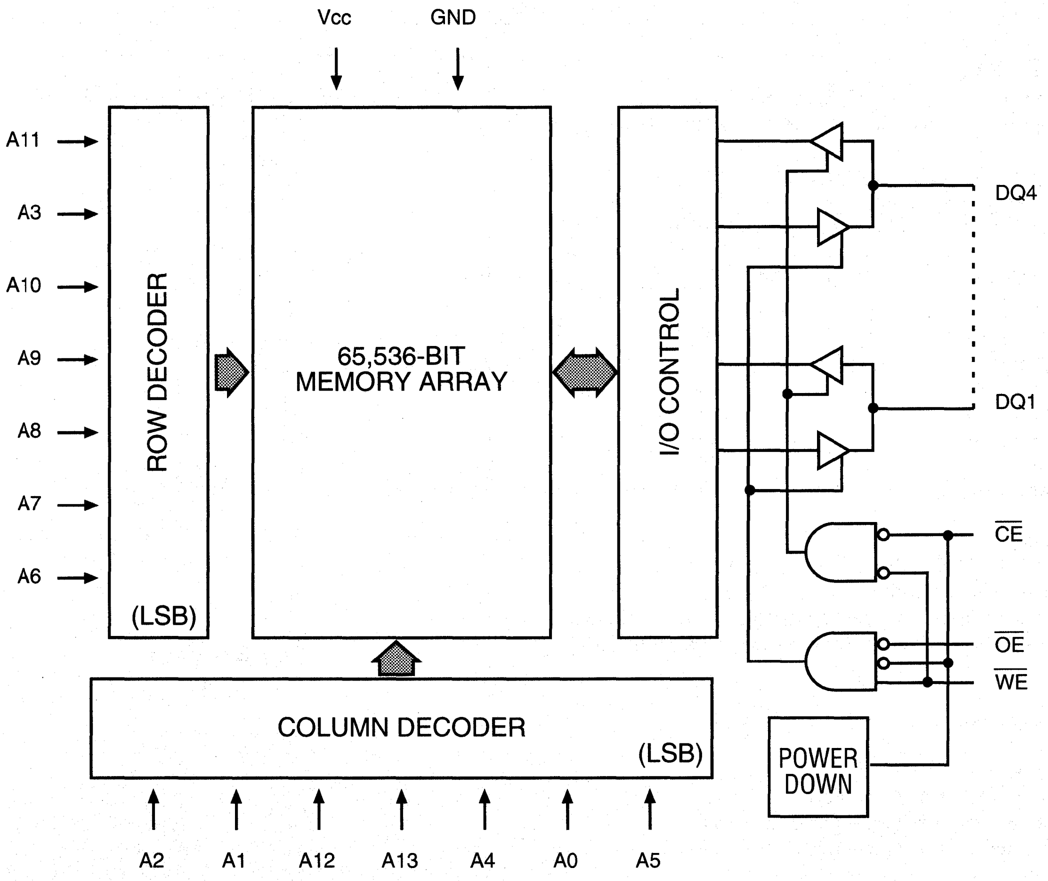
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{\text{CE}}$) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{\text{WE}}$) and $\overline{\text{CE}}$ inputs are both LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH and $\overline{\text{CE}}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \leq V_{OUT} \leq V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	$I_{OH} = -4.0mA$	V_{OH}	2.4		V	1
Output Low Voltage	$I_{OL} = 8.0mA$	V_{OL}		0.4	V	1

				MAX								
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-8**	**-10**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	160	150	140	120	110	100	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	55	50	45	40	35	30	25	mA	14
	$\overline{CE} \geq V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \leq V_{SS}$ +0.2V $V_{IH} \geq V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	3	3	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Output Capacitance		C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	^{t}RC	8		10		12		15		20		25		35		ns	
Address access time	^{t}AA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^{t}ACE		7		9		10		12		15		20		30	ns	
Output hold from address change	^{t}OH	3		3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^{t}LZCE	2		2		2		3		5		5		5		ns	
Chip disable to output in High-Z	^{t}HZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		8		10		12		15		20		25		35	ns	
Output Enable access time	^{t}AOE		3		4		5		6		7		8		15	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		0		0		0		ns	
Output disable to output in High-Z	^{t}HZOE		4		4		5		6		7		8		8	ns	6
WRITE Cycle																	
WRITE cycle time	^{t}WC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^{t}CW	8		9		10		12		15		20		25		ns	
Address valid to end of write	^{t}AW	8		9		11		12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		0		0		ns	
WRITE pulse width	^{t}WP1	7		8		9		12		15		18		20		ns	
WRITE pulse width	^{t}WP2	8		9		10		14		18		20		25		ns	
Data setup time	^{t}DS	5		6		7		8		10		10		12		ns	
Data hold time	^{t}DH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	2		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^{t}HZWE		4		5		5		6		8		8		8	ns	6

*These specifications are preliminary.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

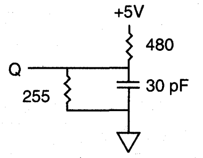


Fig. 1 OUTPUT LOAD EQUIVALENT

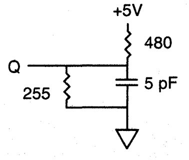


Fig. 2 OUTPUT LOAD EQUIVALENT

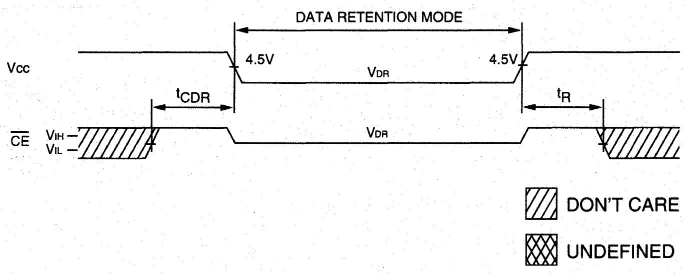
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-173.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

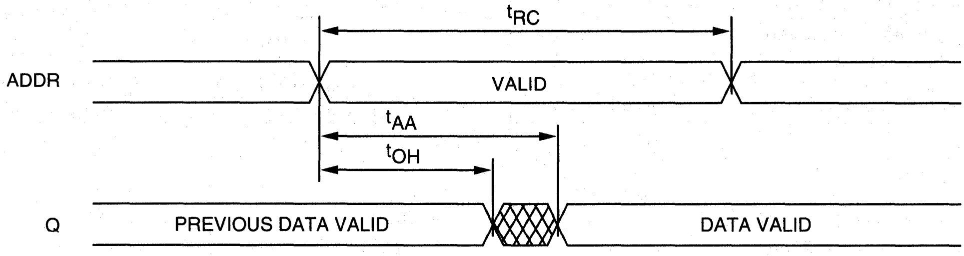
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE} \geq$ (Vcc -0.2V) $V_{IN} \geq$ (Vcc -0.2V) or $\leq$ 0.2V	Vcc = 2V	I_{CCDR}		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

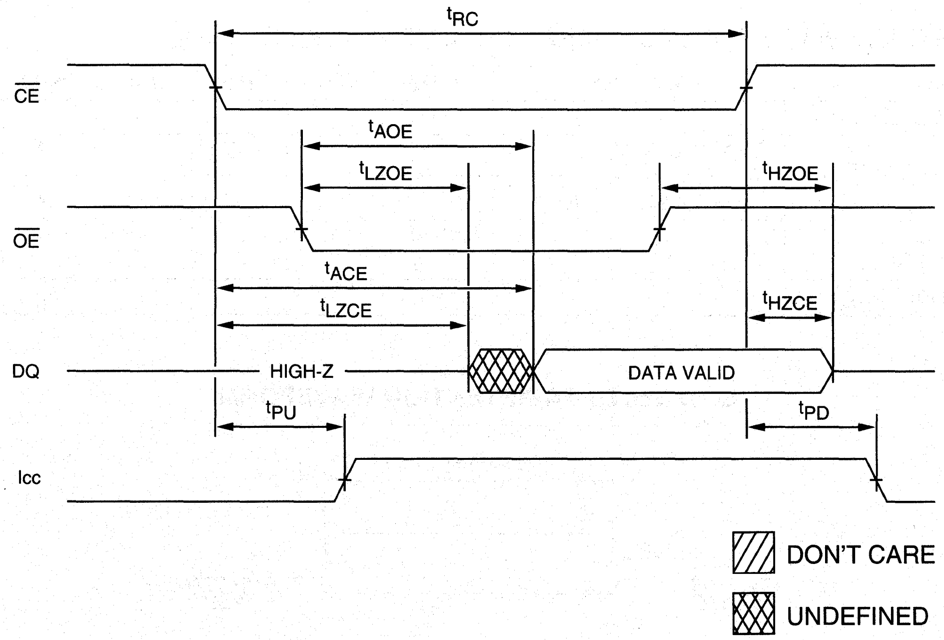
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1[8, 9]

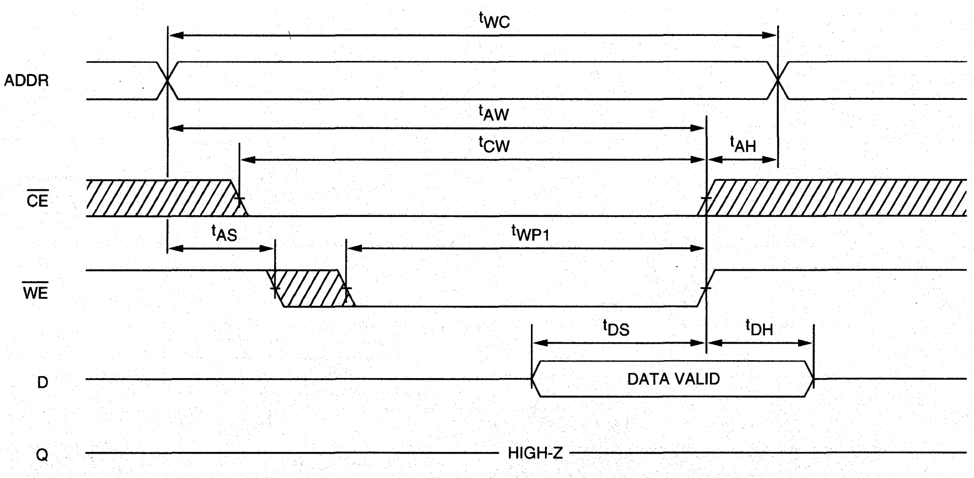


READ CYCLE NO. 2[7, 8, 10]



WRITE CYCLE NO. 1

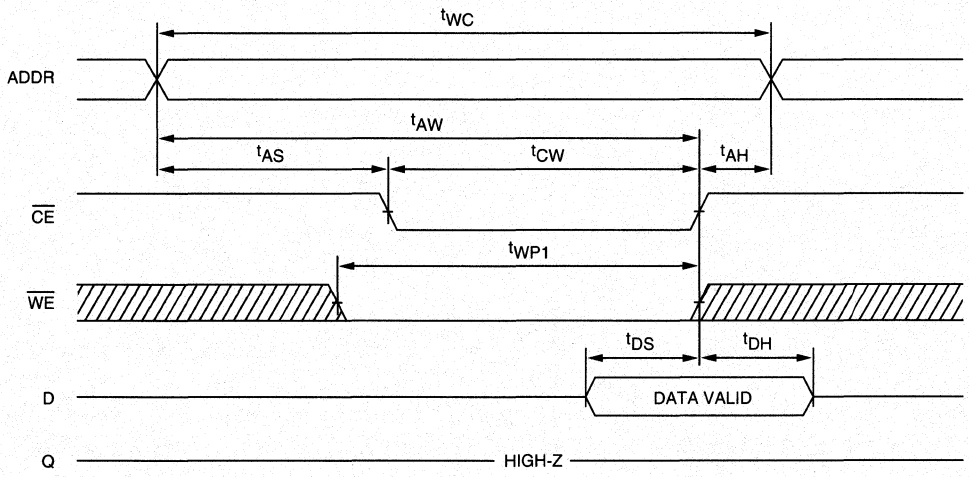
(Write Enable Controlled)[7, 12]



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 2

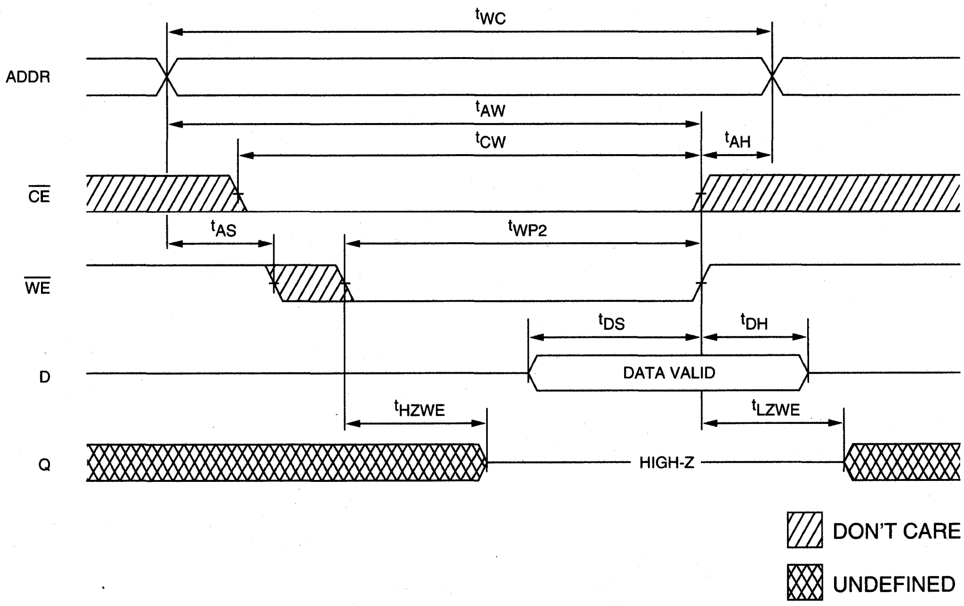
(Chip Enable Controlled)



▨ DON'T CARE

▦ UNDEFINED

WRITE CYCLE NO. 3
(Write Enable Controlled)



16K x 4 SRAM

WITH SEPARATE INPUTS AND OUTPUTS

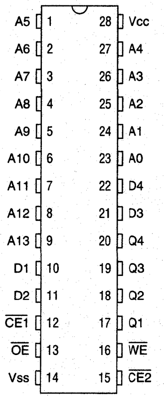
FEATURES

- High speed: 8, 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, $\overline{CE2}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- MT5C6406 – output tracks input during WRITE
- MT5C6407 – output High-Z during WRITE

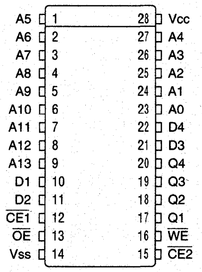
OPTIONS	MARKING
• Timing	
8ns access (preliminary)	- 8
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

28-Pin DIP
(A-9)



28-Pin SOJ
(E-8)



GENERAL DESCRIPTION

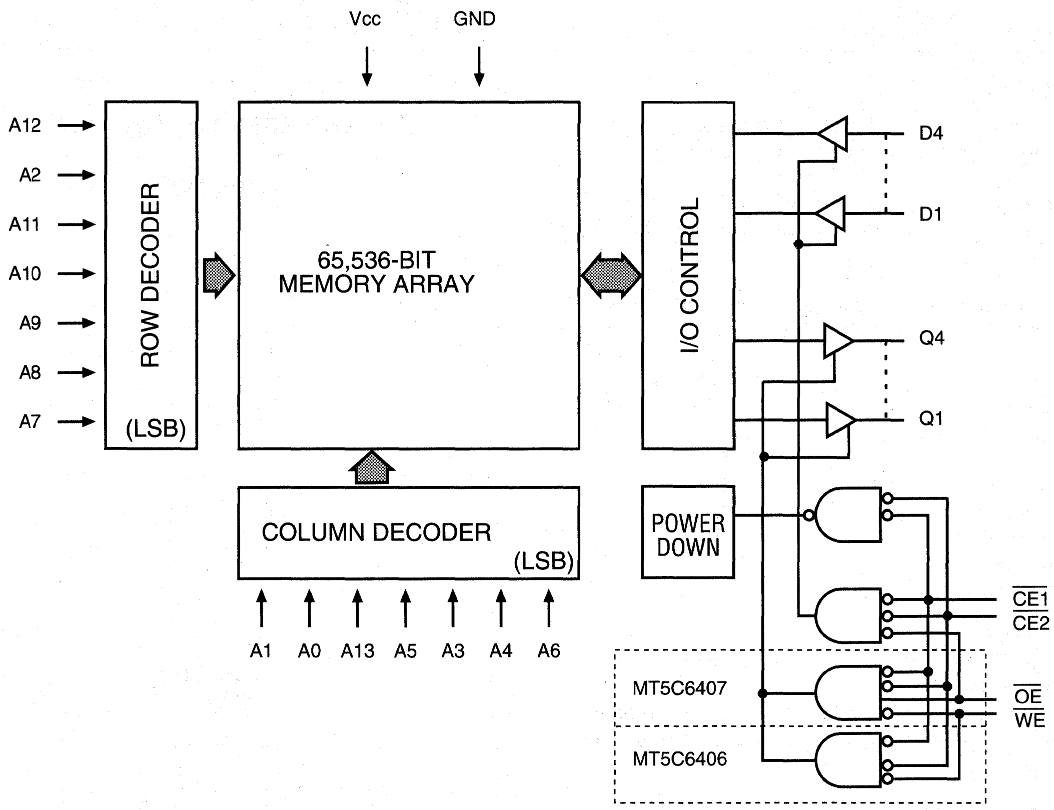
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x4 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE1}$	$\overline{CE2}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	X	X	HIGH-Z	STANDBY
STANDBY	X	H	X	X	HIGH-Z	STANDBY
READ	L	L	L	H	Q	ACTIVE
READ	L	L	H	H	HIGH-Z	ACTIVE
WRITE (1)	L	L	X	L	HIGH-Z	ACTIVE
WRITE (2)	L	L	L	L	D	ACTIVE
WRITE (2)	L	L	H	L	HIGH-Z	ACTIVE

NOTE: 1. MT5C6407 ONLY
2. MT5C6406 ONLY

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ....-1V to +7V
Storage Temperature (Plastic) ....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disable $0V \leq V_{OUT} \leq V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX							UNITS	NOTES
				-8	-10	-12	-15	-20	-25	-35		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}$; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	160	150	140	120	110	100	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}$; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	55	50	45	40	35	30	25	mA	14
	$\overline{CE} \geq V_{CC}$ -0.2V; Vcc = MAX $V_{IL} \leq V_{SS}$ +0.2V $V_{IH} \geq V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	3	3	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	C_I	5	pF	4
Output Capacitance		C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	^tRC	8		10		12		15		20		25		35		ns	
Address access time	^tAA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^tACE		7		9		10		12		15		20		30	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		3		5		5		5		ns	
Chip disable to output in High-Z	^tHZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		8		10		12		15		20		25		35	ns	
Output Enable access time	^tAOE		3		4		5		6		7		8		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4		4		5		6		7		8		8	ns	6
WRITE Cycle																	
WRITE cycle time	^tWC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		9		10		12		15		20		25		ns	
Address valid to end of write	^tAW	8		9		11		12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		0		ns	
WRITE pulse width	^tWP	7		8		9		12		15		18		20		ns	
Data setup time	^tDS	5		6		7		8		10		10		12		ns	
Data hold time	^tDH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8		8	ns	6
Write Enable to output valid	^tAWE		10		12		14		17		20		25		35	ns	
Data valid to output valid	^tADV		10		12		14		17		20		25		35	ns	

*These specifications are preliminary.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

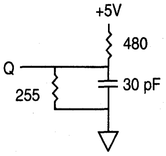


Fig. 1 OUTPUT LOAD EQUIVALENT

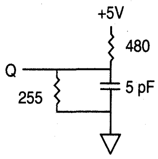


Fig. 2 OUTPUT LOAD EQUIVALENT

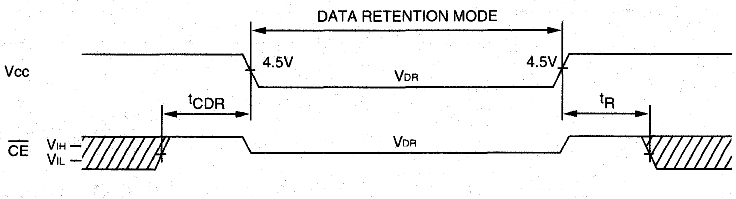
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-173.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

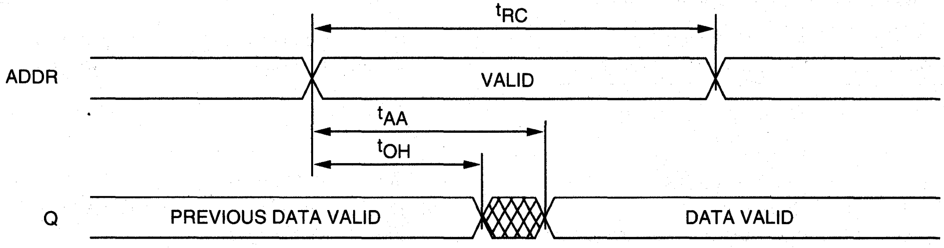
LOW Vcc DATA RETENTION WAVEFORM



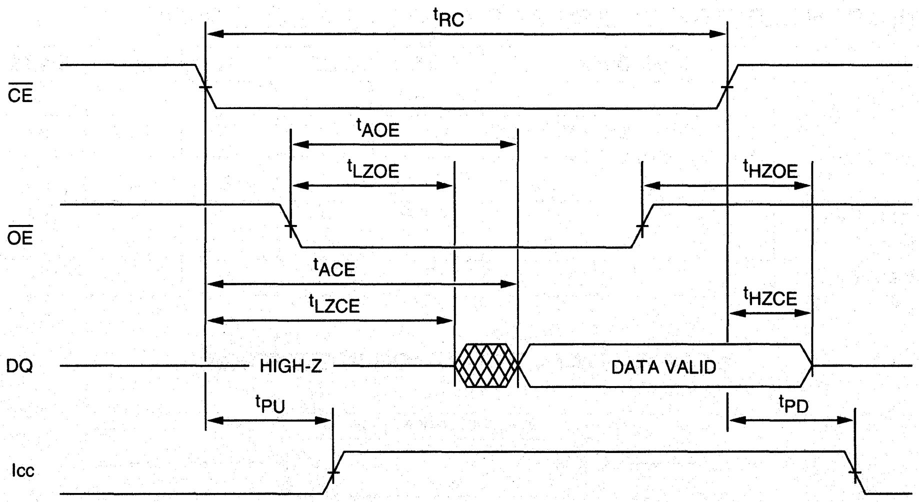
▨ DON'T CARE

▩ UNDEFINED

READ CYCLE NO. 1[8, 9]



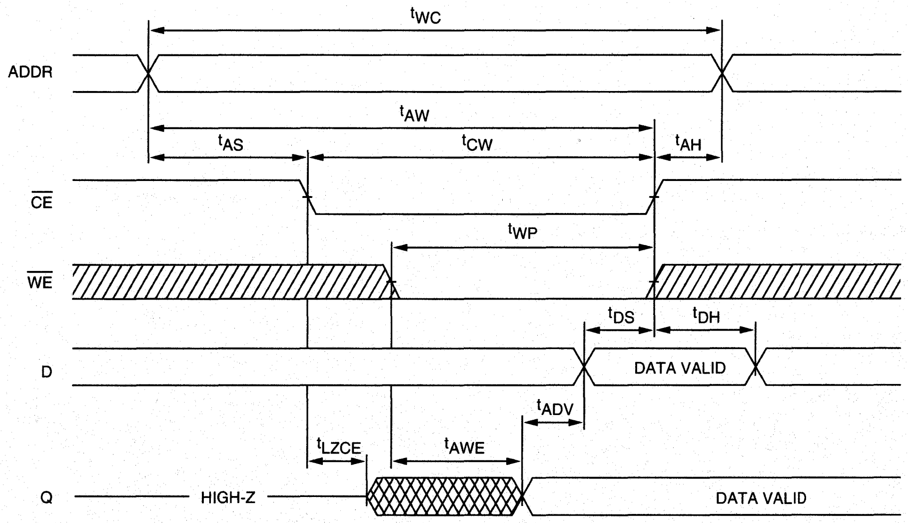
READ CYCLE NO. 2[7, 8, 10]



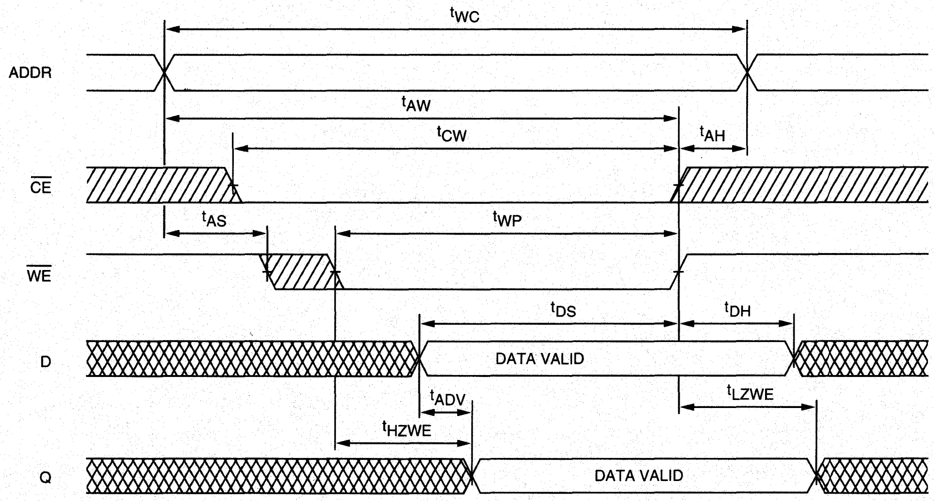
▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2
(Write Enable Controlled) 7, 12



▨ DON'T CARE

▩ UNDEFINED

SRAM

64K x 4 SRAM

FEATURES

- High speed: 15, 20, 25, 30, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{\text{CE}}$ option
- All inputs and outputs are TTL compatible

OPTIONS

OPTIONS	MARKING
• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic SOIC (300 mil)	SG
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

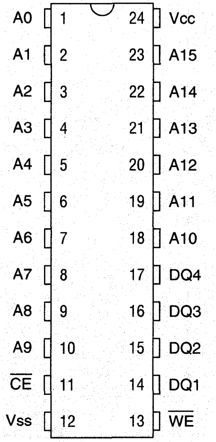
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{\text{CE}}$) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{\text{WE}}$) and $\overline{\text{CE}}$ inputs are both LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH and $\overline{\text{CE}}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

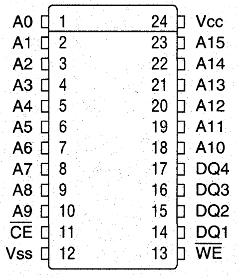
All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

PIN ASSIGNMENT (Top View)

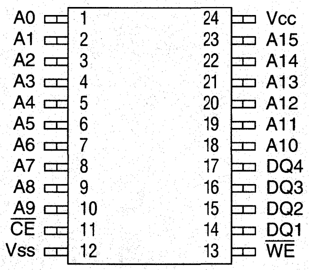
24-Pin DIP
(A-7)



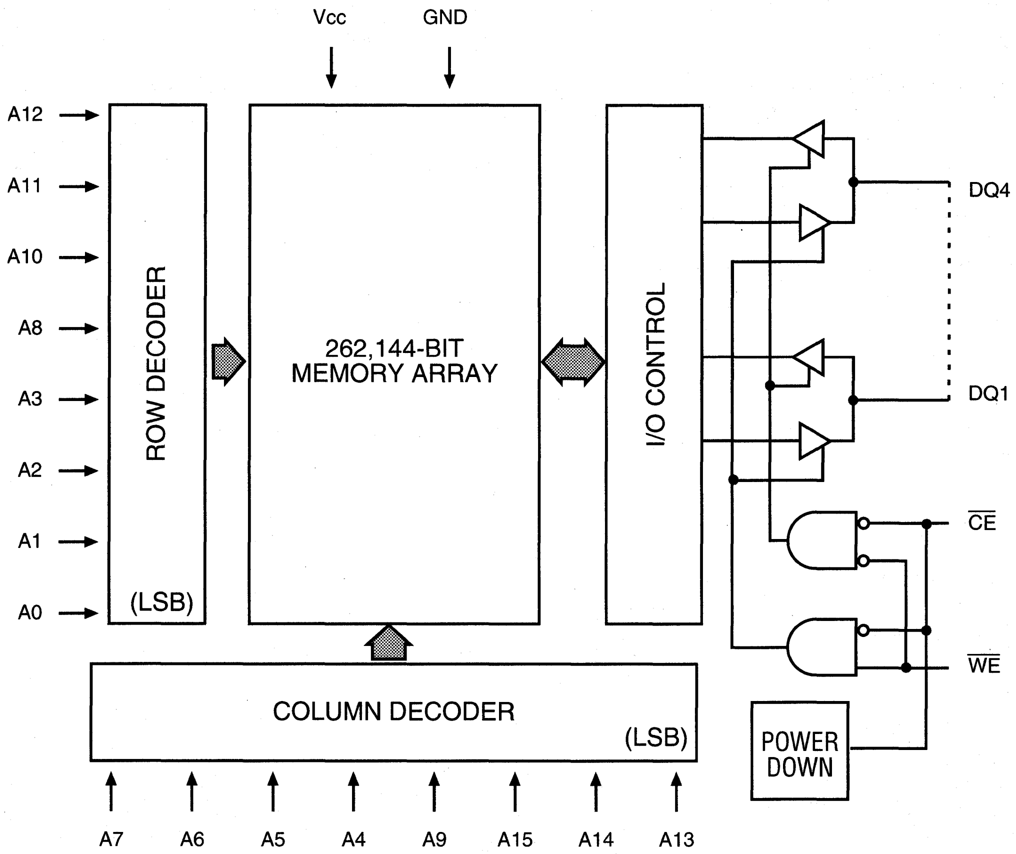
24-Pin SOJ
(E-4)



24-Pin SOIC
(F-1)



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS}	-1V to +7V
Storage Temperature (Plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	IL_I	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	IL_O	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX						UNITS	NOTES
				-15	-20	-25	-30	-35	-45		
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	75	140	120	110	95	90	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	11	30	30	25	25	25	25	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	.04	5	5	5	5	7	7	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	6	pF	4
Output Capacitance		C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-15		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^{t}RC	15		20		25		30		35		45		ns	
Address access time	^{t}AA		15		20		25		30		35		45	ns	
Chip Enable access time	^{t}ACE		15		20		25		30		35		45	ns	
Output hold from address change	^{t}OH	3		3		5		5		5		5		ns	
Chip Enable to output in Low-Z	^{t}LZCE	4		6		6		6		6		6		ns	
Chip disable to output in High-Z	^{t}HZCE		8		9		9		12		15		18	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		15		20		25		30		35		45	ns	
WRITE Cycle															
WRITE cycle time	^{t}WC	15		20		20		25		30		35		ns	
Chip Enable to end of write	^{t}CW	10		15		15		18		20		25		ns	
Address valid to end of write	^{t}AW	10		15		15		18		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		0		ns	
WRITE pulse width	^{t}WP1	10		15		15		18		20		25		ns	
WRITE pulse width	^{t}WP2	12		15		15		18		20		25		ns	
Data setup time	^{t}DS	10		10		10		12		15		20		ns	
Data hold time	^{t}DH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	4		5		5		5		5		5		ns	
Write Enable to output in High-Z	^{t}HZWE		7		10		10		12		15		18	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

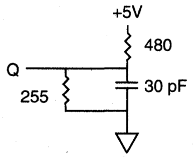


Fig. 1 OUTPUT LOAD EQUIVALENT

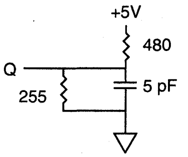


Fig. 2 OUTPUT LOAD EQUIVALENT

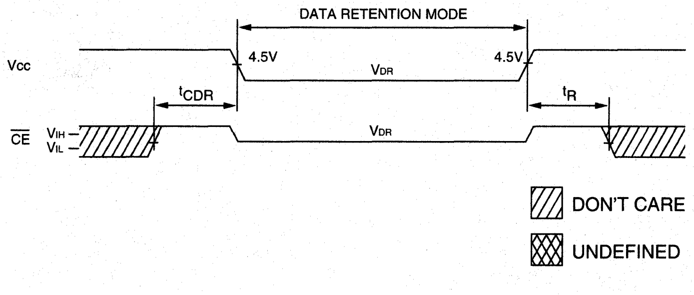
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-175.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

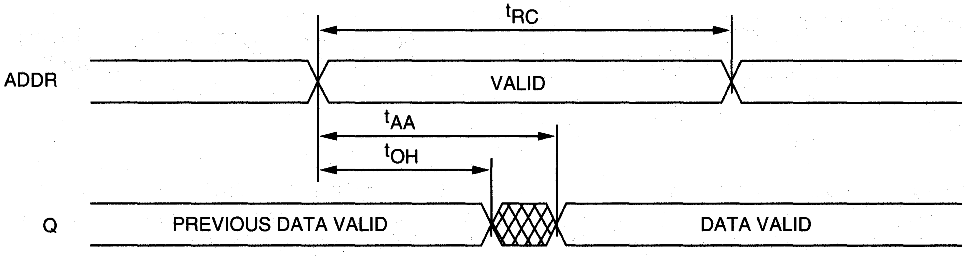
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	300	µA	
		Vcc = 3V			350	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

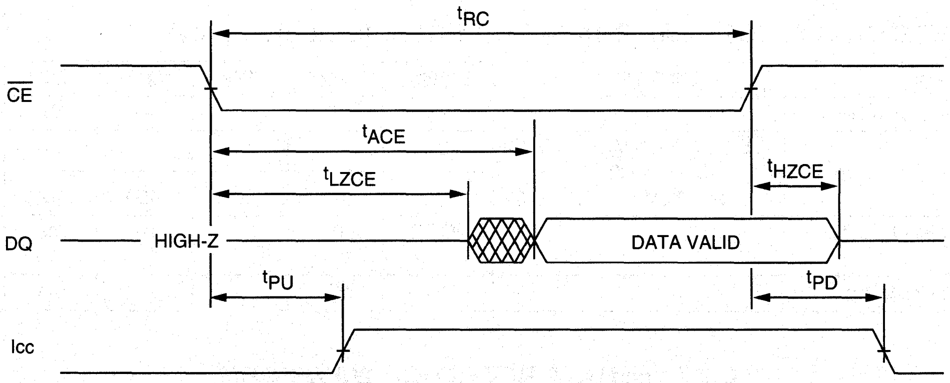
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



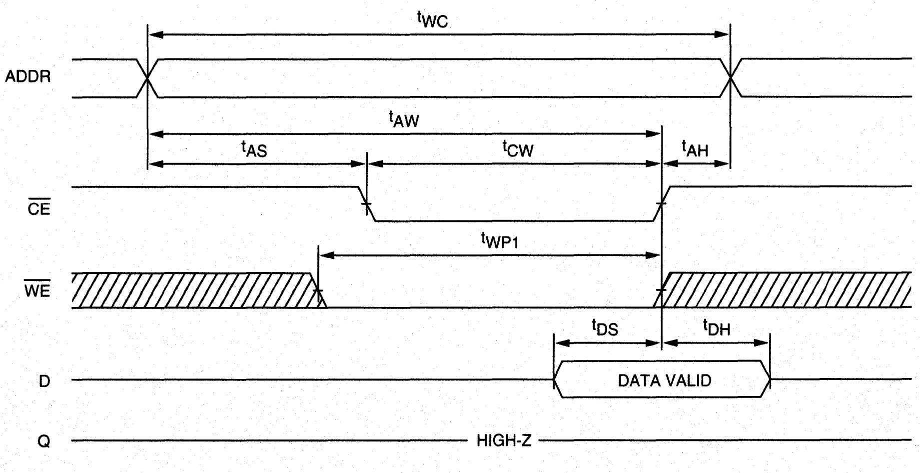
READ CYCLE NO. 2 [7, 8, 10]



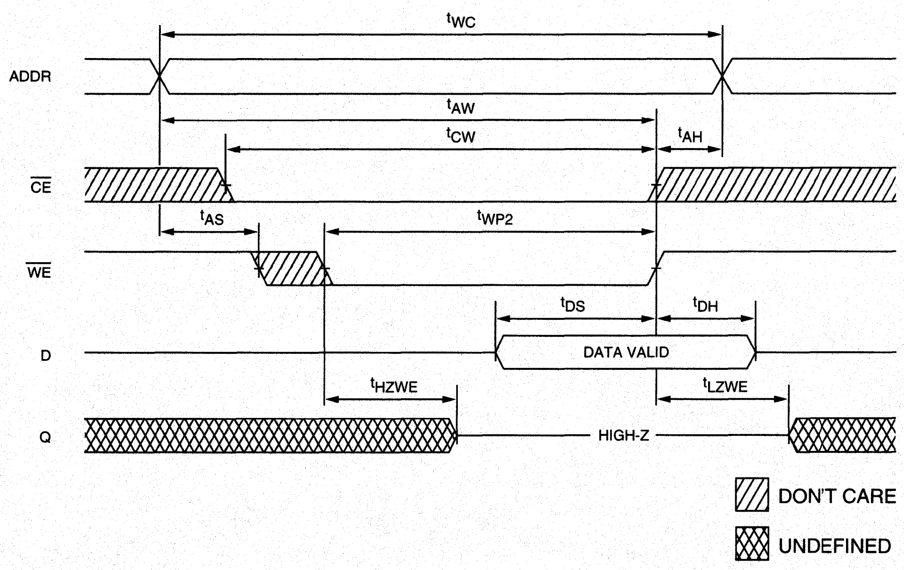
▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2
(Write Enable Controlled)[7, 12]



MICRON TECHNOLOGY, INC. **MT5C2565**

SRAM

64K x 4 SRAM

WITH OUTPUT ENABLE

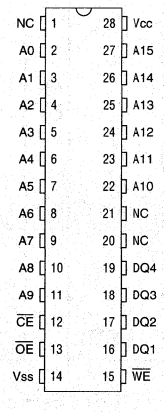
FEATURES

- High speed: 15, 20, 25, 30, 35, and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

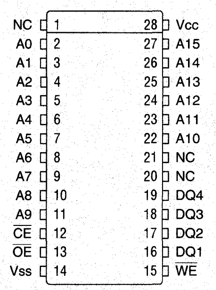
OPTIONS	MARKING
• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

28-Pin DIP
(A-9)



28-Pin SOJ
(E-8)



GENERAL DESCRIPTION

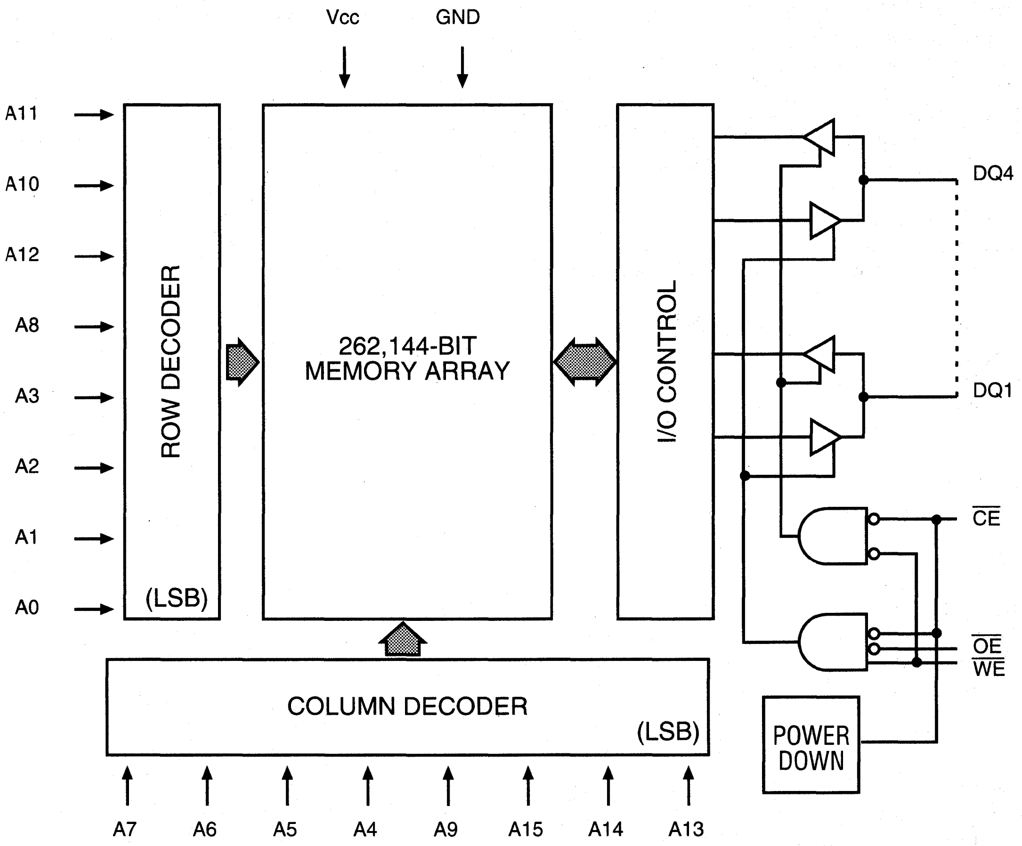
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) on this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-15	-20	-25	-30	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; Vcc = MAX f = MAX = 1/ ^{t}RC Outputs Open	I_{CC}	75	140	120	110	95	90	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; Vcc = MAX f = MAX = 1/ ^{t}RC Outputs Open	I_{SB1}	11	30	30	25	25	25	25	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; Vcc = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	.04	5	5	5	5	7	7	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	C_I	7	pF	4
Output Capacitance		C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-15		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^{t}RC	15		20		25		30		35		45		ns	
Address access time	^{t}AA		15		20		25		30		35		45	ns	
Chip Enable access time	^{t}ACE		15		20		25		30		35		45	ns	
Output hold from address change	^{t}OH	3		3		5		5		5		5		ns	
Chip Enable to output in Low-Z	^{t}LZCE	4		6		6		6		6		6		ns	
Chip disable to output in High-Z	^{t}HZCE		8		9		9		12		15		18	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		15		20		25		30		35		45	ns	
Output Enable access time	^{t}AOE		8		8		8		10		12		15	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		0		0		ns	
Output disable to out put in High-Z	^{t}HZOE		6		7		7		10		12		15	ns	
WRITE Cycle															
WRITE cycle time	^{t}WC	15		20		20		25		30		35		ns	
Chip Enable to end of write	^{t}CW	10		15		15		18		20		25		ns	
Address valid to end of write	^{t}AW	10		15		15		18		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		0		ns	
WRITE pulse width	^{t}WP1	10		15		15		18		20		25		ns	
WRITE pulse width	^{t}WP2	12		15		15		18		20		25		ns	
Data setup time	^{t}DS	7		10		10		12		15		20		ns	
Data hold time	^{t}DH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	4		5		5		5		5		5		ns	
Write Enable to output in High-Z	^{t}HZWE		7		10		10		12		15		18	ns	6

AC TEST CONDITIONS

Input pulse levels	V_{SS} to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

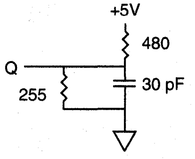


Fig. 1 OUTPUT LOAD EQUIVALENT

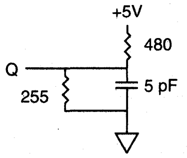


Fig. 2 OUTPUT LOAD EQUIVALENT

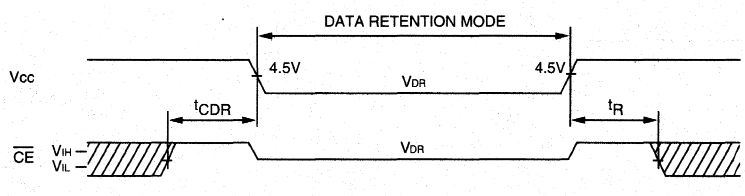
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3V for pulse width < 20ns.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-175.
14. Typical values are measured at 5V, 25°C and 25ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{\text{CE}} \geq (V_{CC}$ -0.2V) $V_{IN} \geq (V_{CC}$ -0.2V) or $\leq$ 0.2V	V_{CC} = 2V	I_{CCDR}		95	300	µA	
		V_{CC} = 3V			350	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

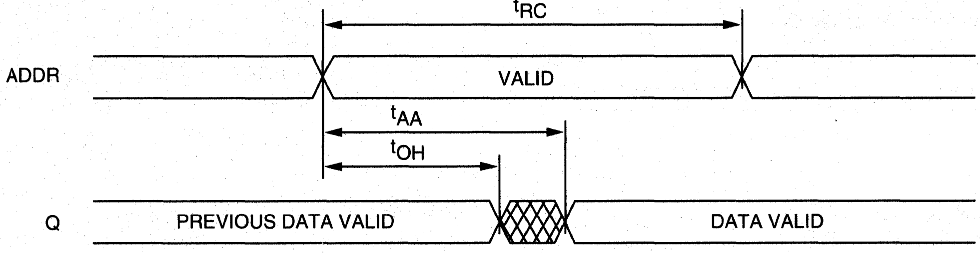
LOW Vcc DATA RETENTION WAVEFORM



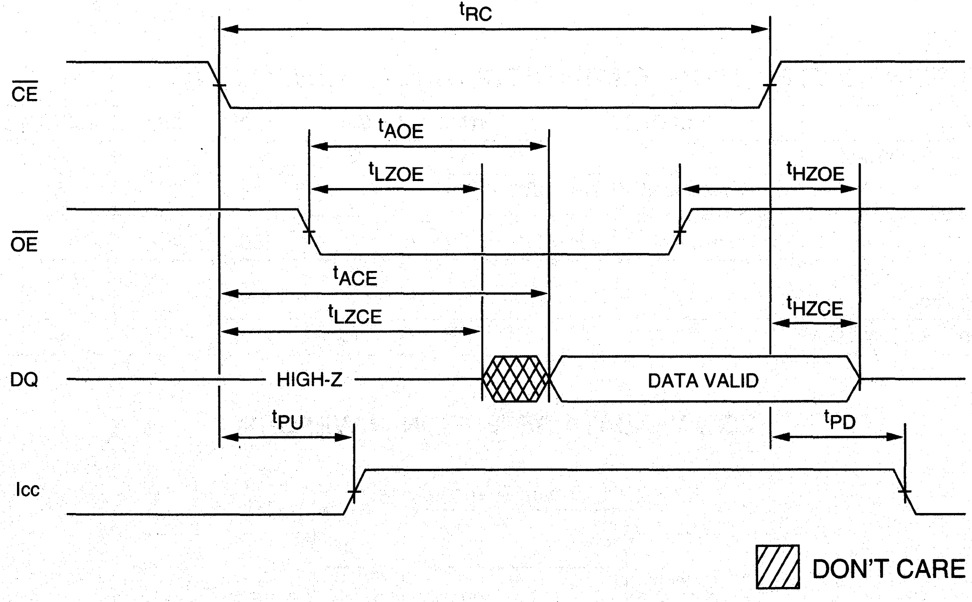
▨ DON'T CARE

▩ UNDEFINED

READ CYCLE NO. 1[8, 9]



READ CYCLE NO. 2[7, 8, 10]

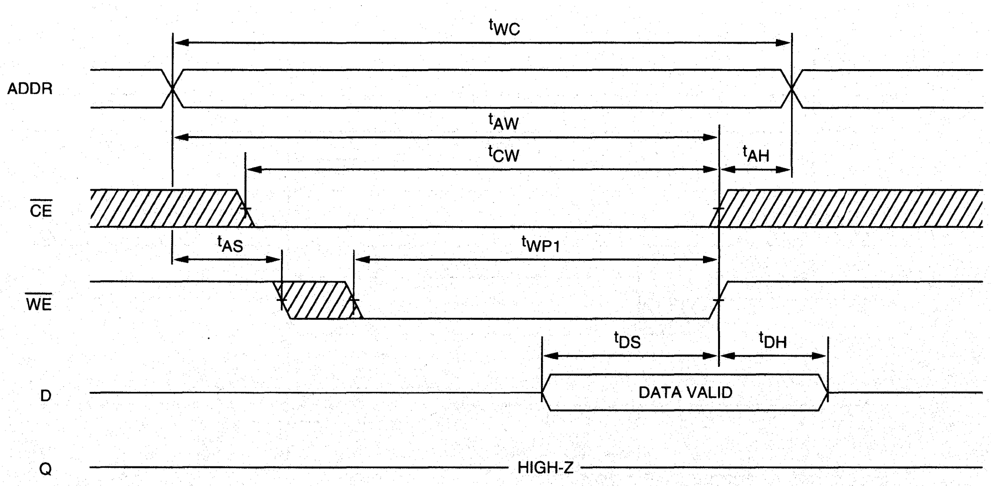


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 1

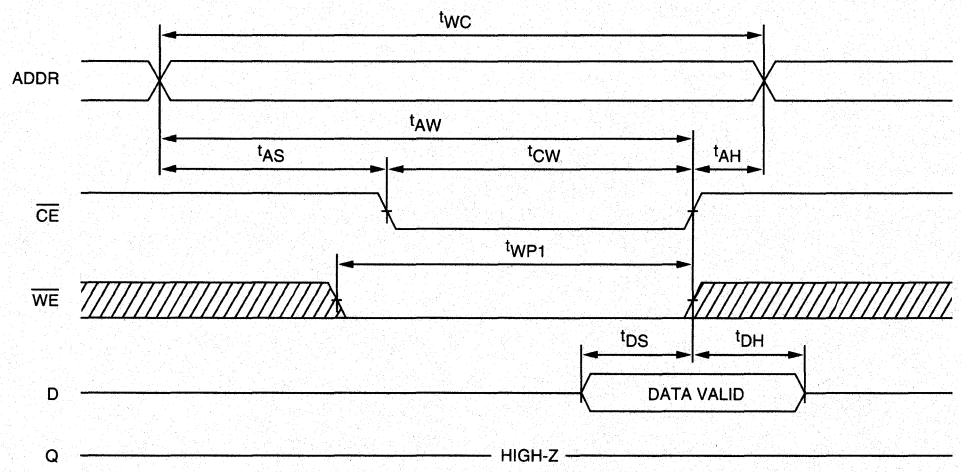
(Write Enable Controlled)[7, 12]



NOTE: Output enable (OE) is inactive (HIGH).

WRITE CYCLE NO. 2

(Chip Enable Controlled)

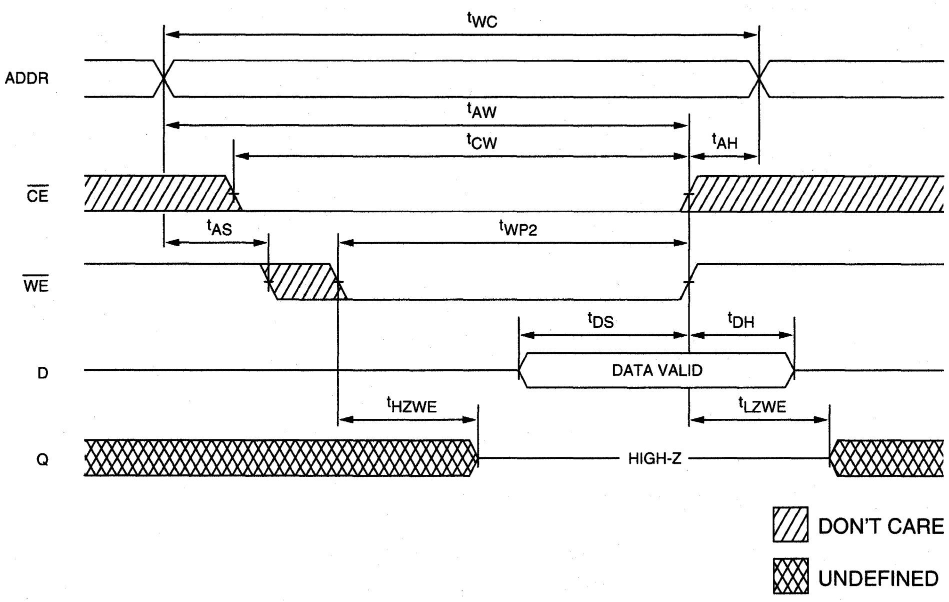


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 3

(Write Enable Controlled) 7, 12



SRAM

256K x 4 SRAM

WITH OUTPUT ENABLE

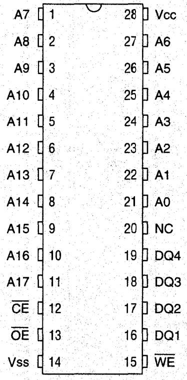
FEATURES

- High speed: 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast Output Enable access time: 8ns

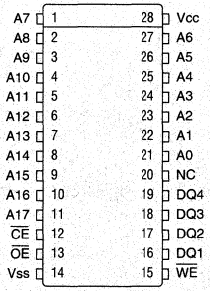
OPTIONS	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

28-Pin DIP
(A-10)



28-Pin SOJ
(E-9)



GENERAL DESCRIPTION

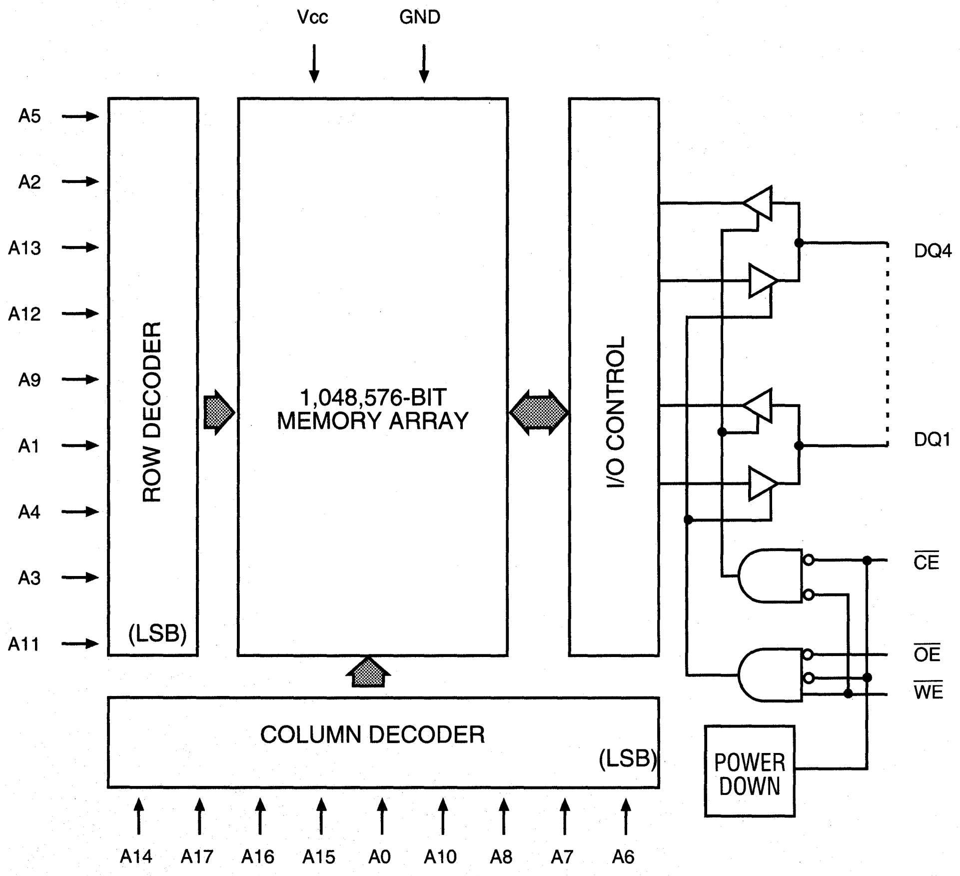
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A11 and A3) are encoded using a gray code.

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ Vcc	ILI	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ VOUT ≤ Vcc	ILO	-5	5	µA	
Output High Voltage	IOH = -4.0mA	VOH	2.4		V	1
Output Low Voltage	IOL = 8.0mA	VOL		0.4	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ VIL; Vcc = MAX f = MAX = 1/ ^{t}RC Outputs Open	Icc	95	140	125	115	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ VIH; Vcc = MAX f = MAX = 1/ ^{t}RC Outputs Open	ISB1	17	35	30	25	25	mA	14
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX VIL ≤ Vss +0.2V VIH ≥ Vcc -0.2V; f = 0	ISB2	0.4	5	5	5	5	mA	14
"L" version only	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX VIL ≤ Vss +0.2V VIH ≥ Vcc -0.2V; f = 0	ISB2	0.3	1.5	1.5	1.5	1.5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	CI	8	pF	4
Output Capacitance		Co	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
READ cycle time	^{t}RC	20		25		35		45		ns	
Address access time	^{t}AA		20		25		35		45	ns	
Chip Enable access time	^{t}ACE		20		25		35		45	ns	
Output hold from address change	^{t}OH	5		5		5		5		ns	
Chip Enable to output in Low-Z	^{t}LZCE	5		5		5		5		ns	
Chip disable to output in High-Z	^{t}HZCE		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		20		25		35		45	ns	
Output Enable access time	^{t}AOE		6		8		12		15	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		ns	
Output disable to output in High-Z	^{t}HZOE		6		10		12		15	ns	6
WRITE Cycle											
WRITE cycle time	^{t}WC	20		25		35		45		ns	
Chip Enable to end of write	^{t}CW	12		15		20		25		ns	
Address valid to end of write	^{t}AW	12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		ns	
WRITE pulse width	^{t}WP1	12		15		20		25		ns	
WRITE pulse width	^{t}WP2	15		15		20		25		ns	
Data setup time	^{t}DS	8		10		15		20		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	5		5		5		5		ns	
Write Enable to output in High-Z	^{t}HZWE	0	8	0	10	0	15	0	18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

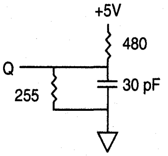


Fig. 1 OUTPUT LOAD EQUIVALENT

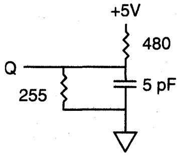


Fig. 2 OUTPUT LOAD EQUIVALENT

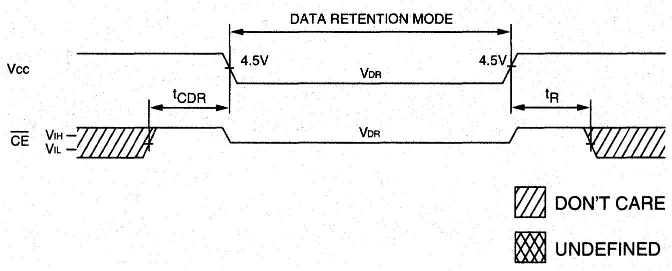
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-177.
14. Typical values are measured at 5V, 25°C and 25ns cycle time.

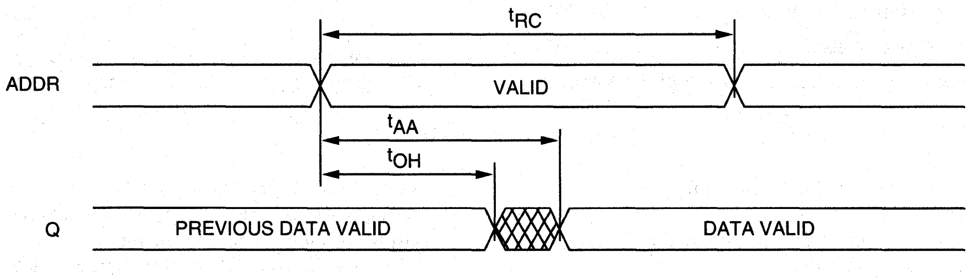
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE} \geq (V_{CC}$ -0.2V)	V_{CC} = 2V	I_{CCDR}		35	200	µA	
	$V_{IN} \geq (V_{CC}$ -0.2V)	V_{CC} = 3V			70	400	µA	
	or ≤ 0.2V	V_{CC} = 5V			250	1,300	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

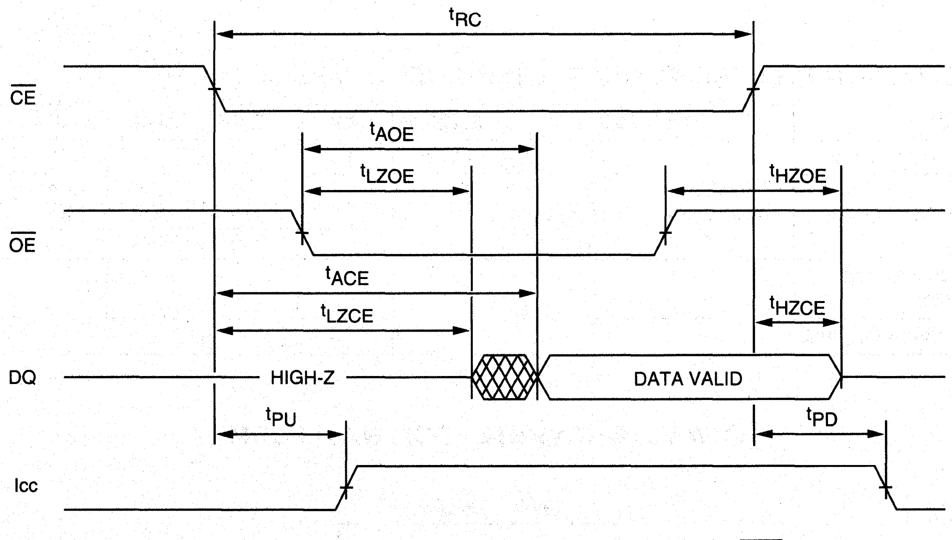
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10]

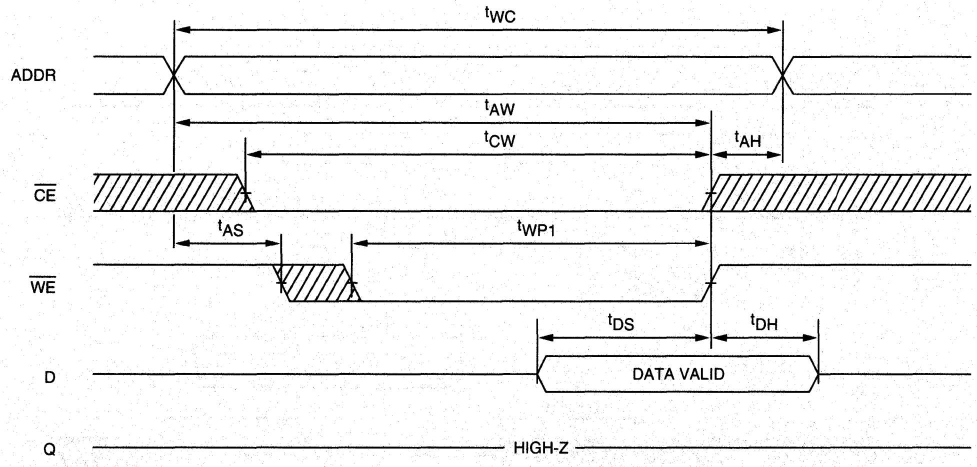


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 1

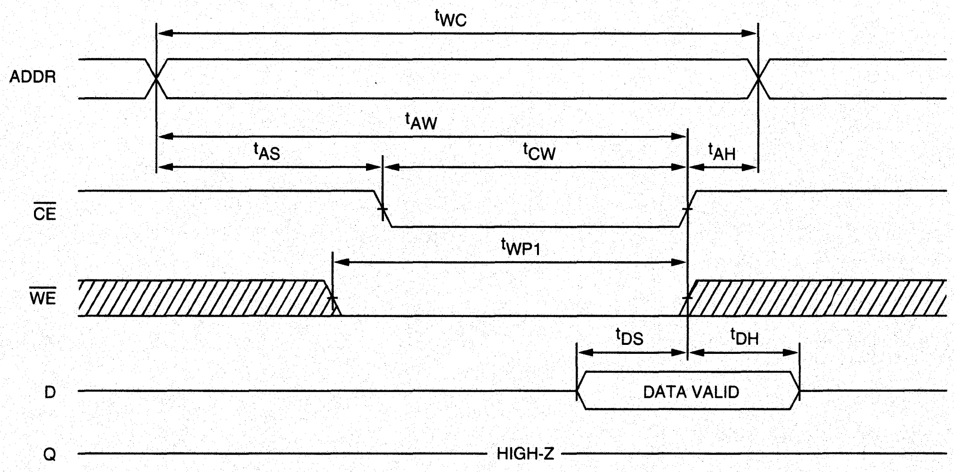
(Write Enable Controlled)[12]



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 2

(Chip Enable Controlled)

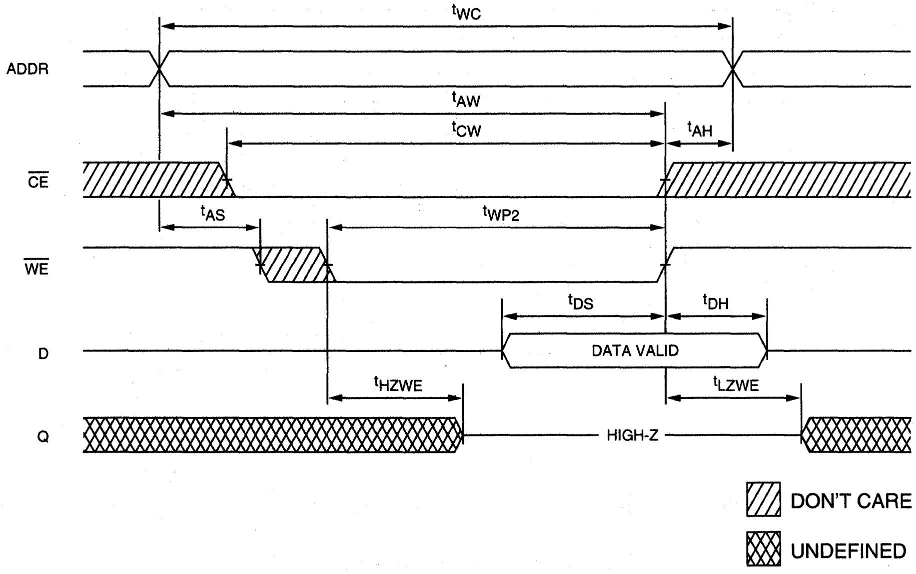


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 3

(Write Enable Controlled) 7, 12



SRAM

1 MEG x 4 SRAM

WITH OUTPUT ENABLE

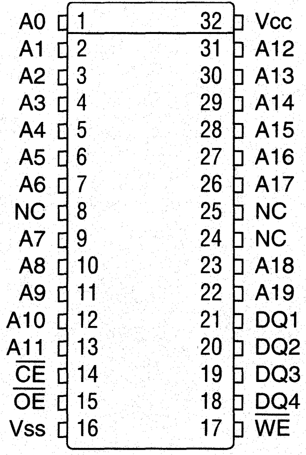
FEATURES

- High speed: 20, 25, 35 and 55ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast Output Enable access time: 8ns

OPTIONS	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
55ns access	-55
• Packages	
Plastic SOJ (400 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(E-11)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

1 MEG x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

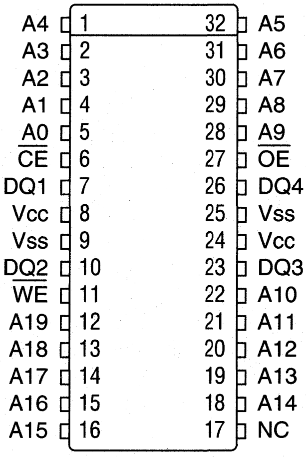
- High speed: 12, 15 and 17ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ options
- All inputs and outputs are TTL compatible
- Fast Output Enable access time: 6ns

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
12ns access	-12
15ns access	-15
17ns access	-17
• Packages	
Plastic SOJ (400 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(E-11)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center and ground pins for very high performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{\text{CE}}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{\text{WE}}$) and $\overline{\text{CE}}$ inputs are both LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH while output enable ($\overline{\text{OE}}$) and $\overline{\text{CE}}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

2K x 8 SRAM

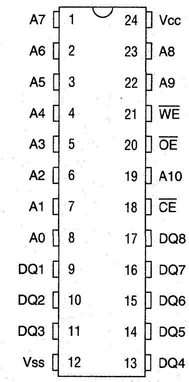
FEATURES

- High speed: 8, 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ options
- All inputs and outputs are TTL compatible

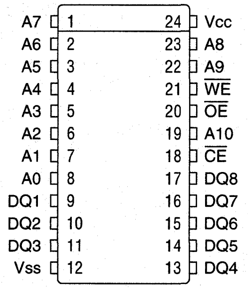
OPTIONS	MARKING
• Timing	
8ns access (preliminary)	- 8
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

24-Pin DIP
(A-7)



24-Pin SOJ
(E-4)



GENERAL DESCRIPTION

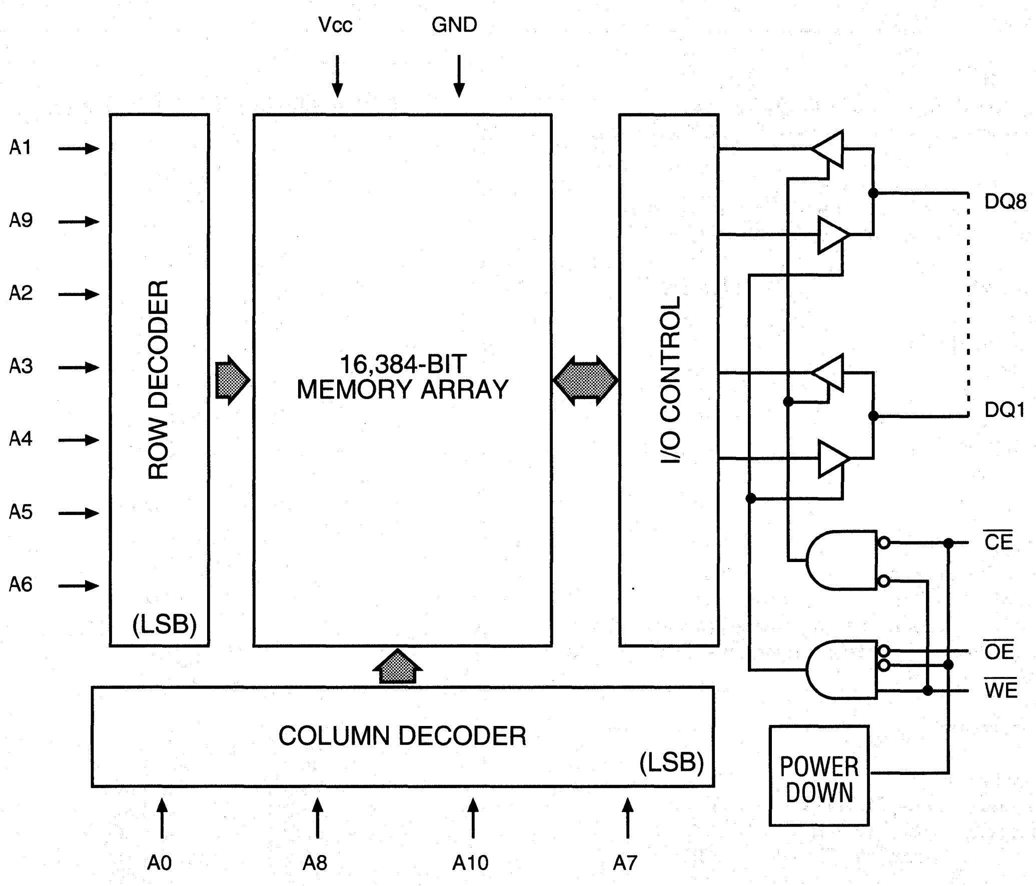
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{\text{CE}}$) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{\text{WE}}$) and $\overline{\text{CE}}$ inputs are both LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH and $\overline{\text{CE}}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX								
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-8**	**-10**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	160	150	140	120	110	100	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	55	50	45	40	35	30	25	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	3	3	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Output Capacitance		C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	^{t}RC	8		10		12		15		20		25		35		ns	
Address access time	^{t}AA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^{t}ACE		7		9		10		12		15		20		30	ns	
Output hold from address change	^{t}OH	3		3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^{t}LZCE	2		2		2		3		5		5		5		ns	
Chip disable to output in High-Z	^{t}HZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		8		10		12		15		20		25		35	ns	
Output Enable access time	^{t}AOE		4		5		6		7		8		8		15	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		0		0		0		ns	
Output disable to output in High-Z	^{t}HZOE		4		5		5		6		7		8		8	ns	6
WRITE Cycle																	
WRITE cycle time	^{t}WC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^{t}CW	8		9		10		12		15		20		25		ns	
Address valid to end of write	^{t}AW	8		9		11		12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		0		0		ns	
WRITE pulse width	^{t}WP1	7		8		9		12		15		18		20		ns	
WRITE pulse width	^{t}WP2	8		9		10		14		18		20		25		ns	
Data setup time	^{t}DS	5		6		7		8		10		10		12		ns	
Data hold time	^{t}DH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	2		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^{t}HZWE		4		5		5		6		8		8		8	ns	6

*These specifications are preliminary.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

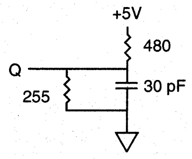


Fig. 1 OUTPUT LOAD EQUIVALENT

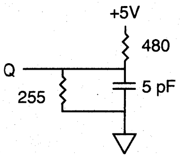


Fig. 2 OUTPUT LOAD EQUIVALENT

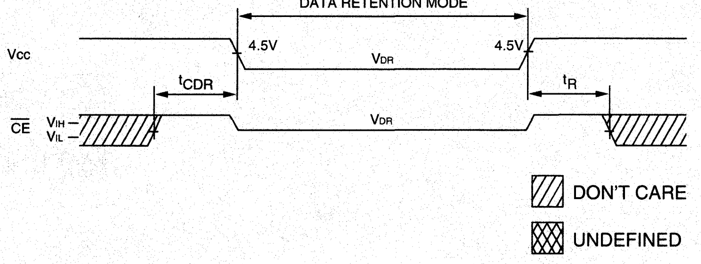
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-171.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

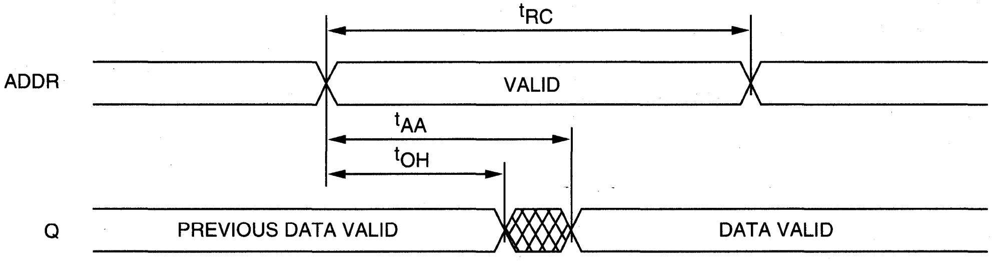
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

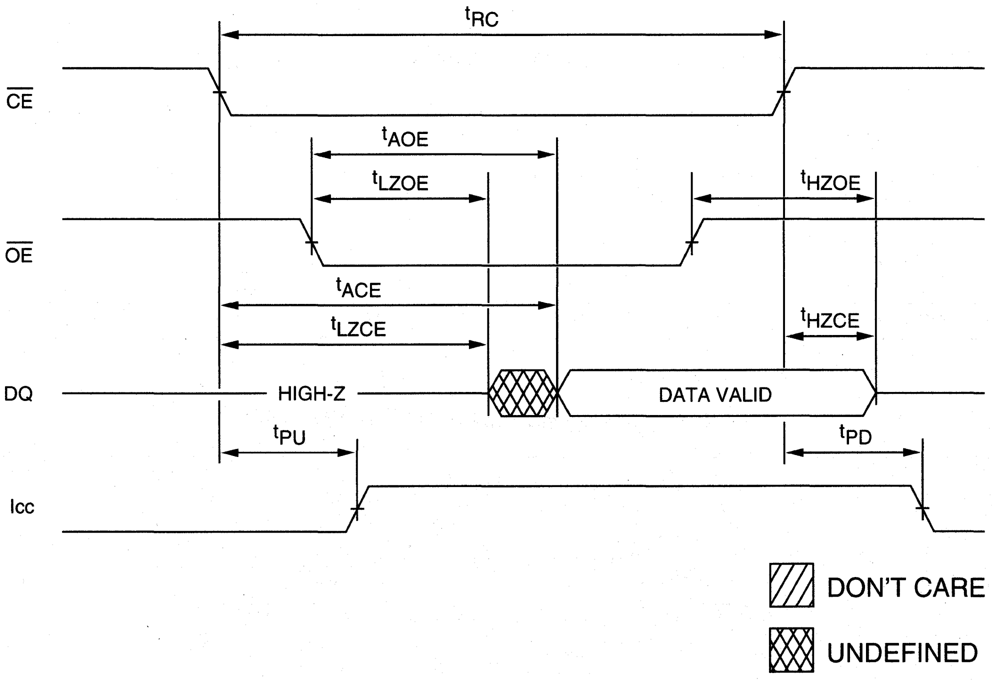
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]

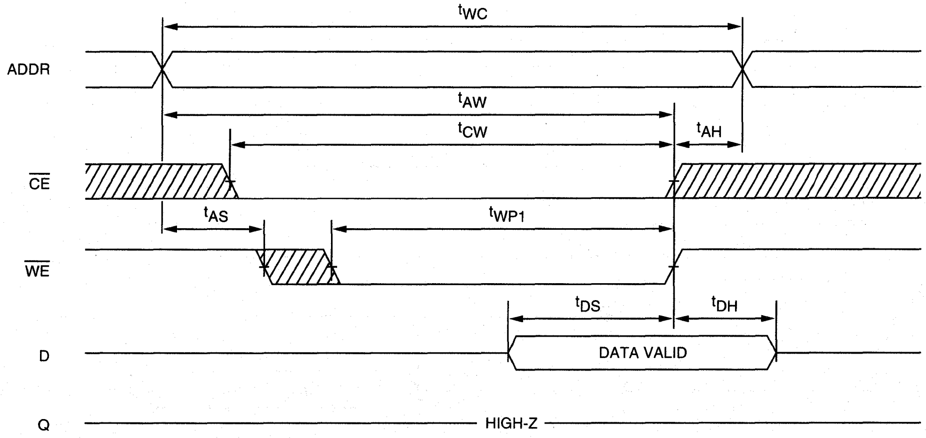


READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1

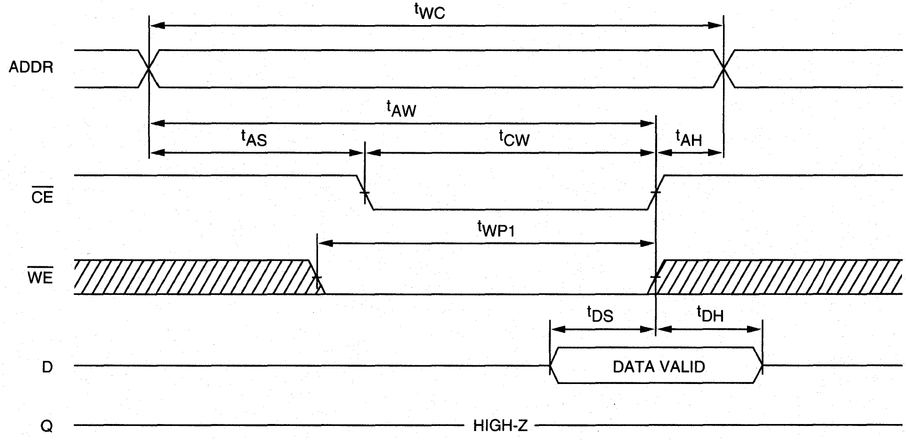
(Write Enable Controlled) [12]



NOTE: Output enable (OE) is inactive (HIGH).

WRITE CYCLE NO. 2

(Chip Enable Controlled)

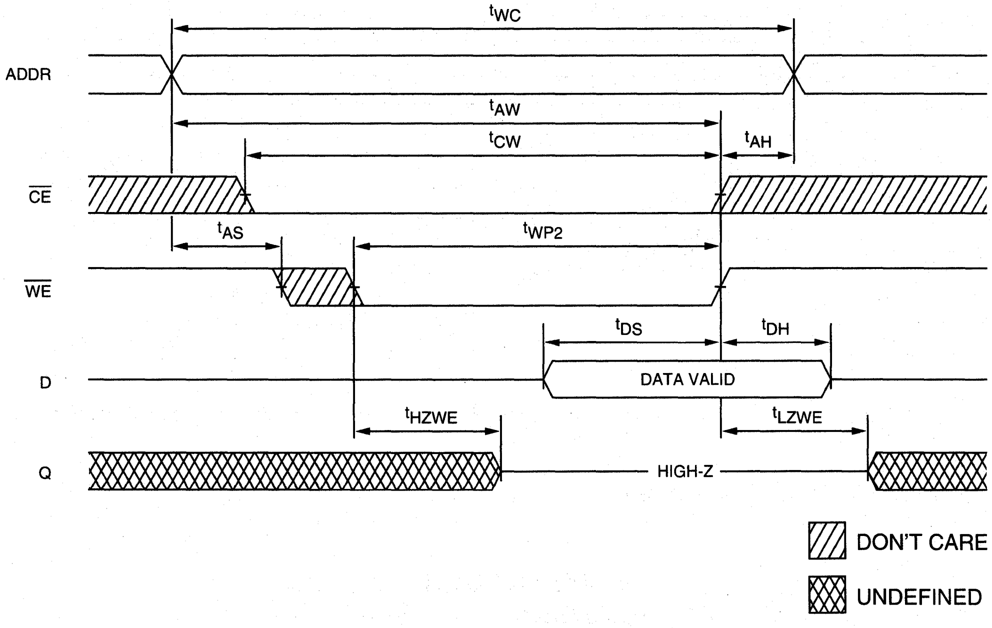


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 3

(Write Enable Controlled) 7, 12



8K x 8 SRAM

FEATURES

- High speed: 8, 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{\text{CE}}$1, CE2 and $\overline{\text{OE}}$ options
- All inputs and outputs are TTL compatible

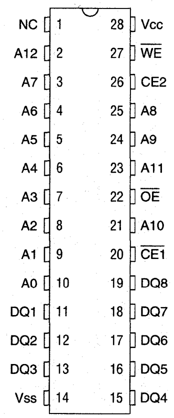
OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
8ns access (preliminary)	- 8
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

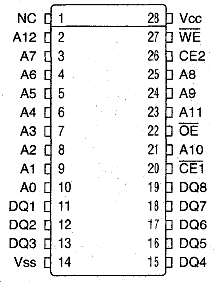
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***

PIN ASSIGNMENT (Top View)

28-Pin DIP
(A-9)



28-Pin SOJ
(E-8)



GENERAL DESCRIPTION

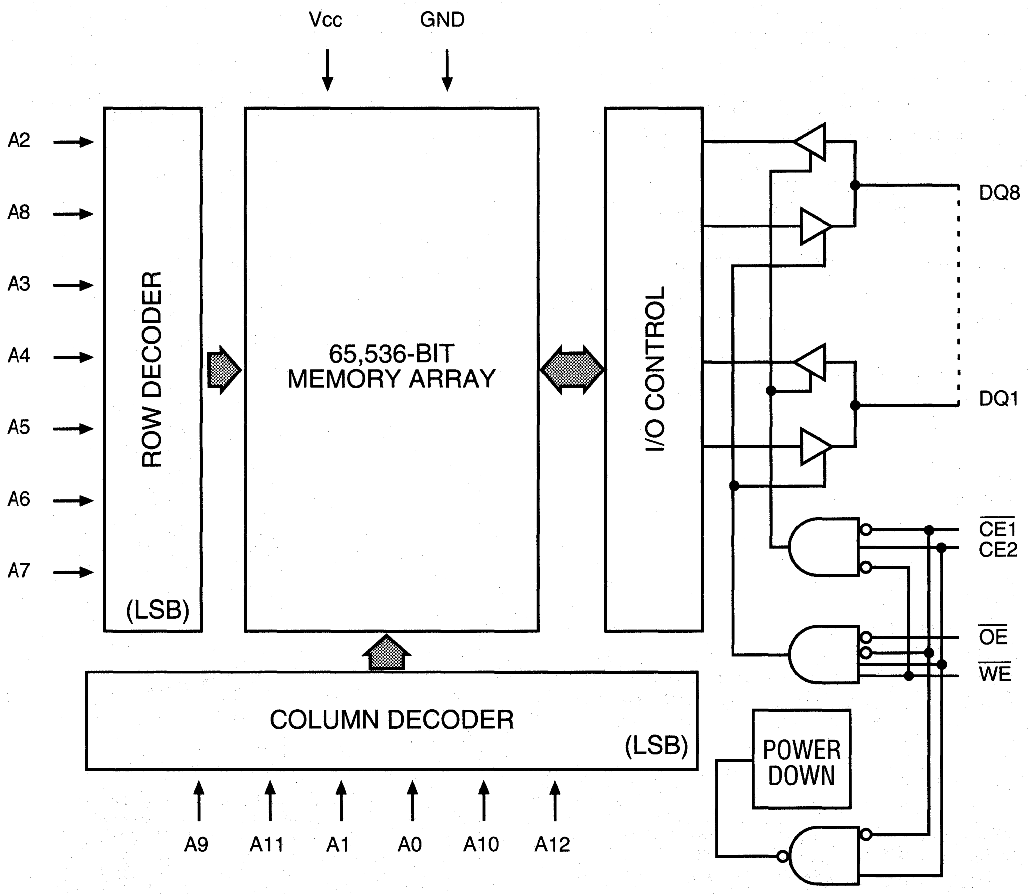
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers two chip enables on the x8 organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{\text{WE}}$) and $\overline{\text{CE}}$ inputs are both LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH and $\overline{\text{CE}}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	X	X	HIGH-Z	STANDBY
STANDBY	X	L	X	X	HIGH-Z	STANDBY
READ	L	H	H	L	Q	ACTIVE
READ	L	H	H	H	HIGH-Z	ACTIVE
WRITE	L	H	L	X	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .... -1.0V to +7.0V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	IL_I	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	IL_O	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX								
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-8	-10	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	Icc	65	160	150	140	120	110	100	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	55	50	45	40	35	30	25	mA	14
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IL} ≤ Vss +0.2V V_{IH} ≥ Vcc -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	3	3	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	C_I	5	pF	4
Output Capacitance		C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle																	
READ cycle time	^{t}RC	8		10		12		15		20		25		35		ns	
Address access time	^{t}AA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^{t}ACE		7		9		10		12		15		20		30	ns	
Output hold from address change	^{t}OH	3		3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^{t}LZCE	2		2		2		3		5		5		5		ns	
Chip disable to output in High-Z	^{t}HZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		8		10		12		15		20		25		35	ns	
Output Enable access time	^{t}AOE		4		5		6		7		8		8		15	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		0		0		0		ns	
Output disable to output in High-Z	^{t}HZOE		4		5		5		6		7		8		8	ns	6
WRITE Cycle																	
WRITE cycle time	^{t}WC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^{t}CW	8		9		10		12		15		20		25		ns	
Address valid to end of write	^{t}AW	8		9		11		12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		0		0		ns	
WRITE pulse width	^{t}WP1	7		8		9		12		15		18		20		ns	
WRITE pulse width	^{t}WP2	8		9		10		14		18		20		25		ns	
Data setup time	^{t}DS	5		6		7		8		10		10		12		ns	
Data hold time	^{t}DH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	2		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^{t}HZWE		4		5		5		6		8		8		8	ns	6

*These specifications are preliminary.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

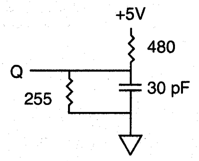


Fig. 1 OUTPUT LOAD EQUIVALENT

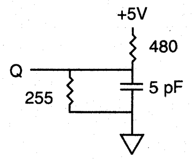


Fig. 2 OUTPUT LOAD EQUIVALENT

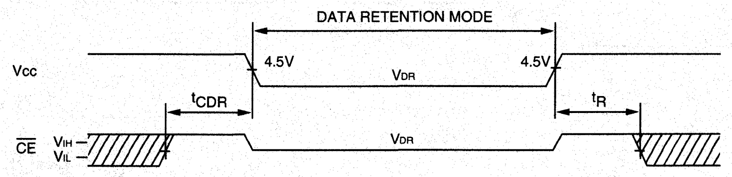
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-173.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{\text{CE}}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

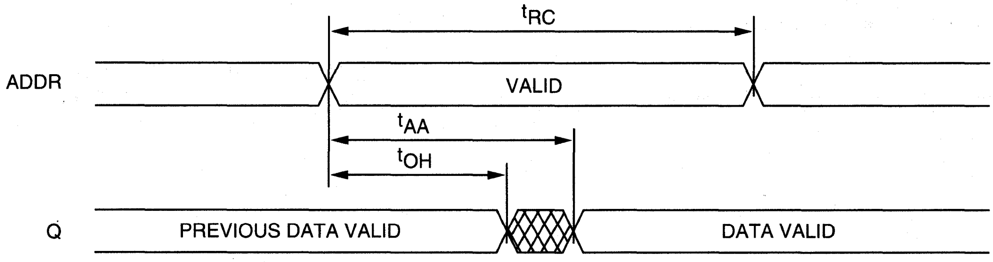
LOW Vcc DATA RETENTION WAVEFORM



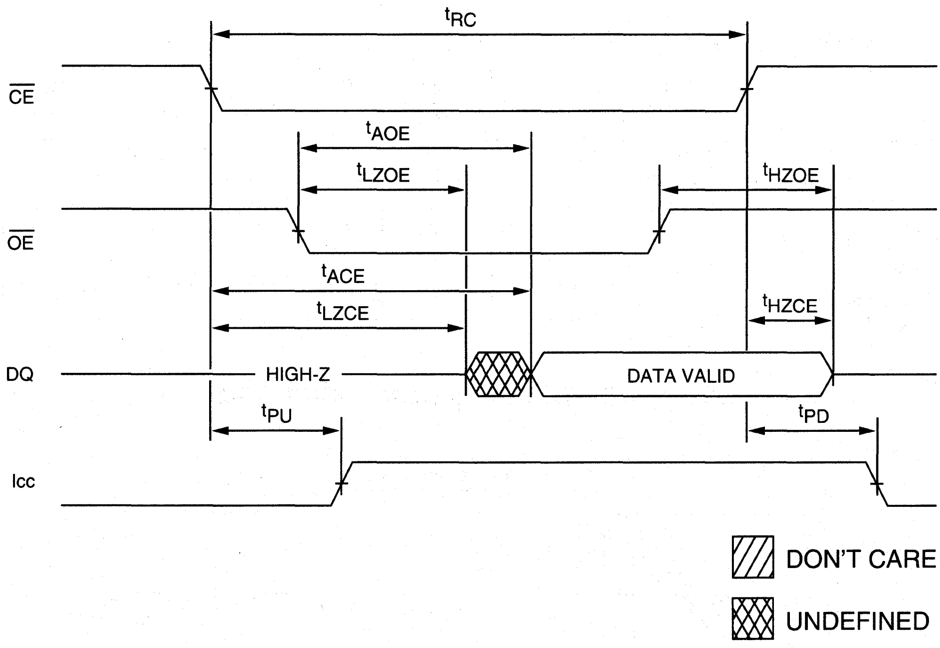
▨ DON'T CARE

▩ UNDEFINED

READ CYCLE NO. 1[8, 9]

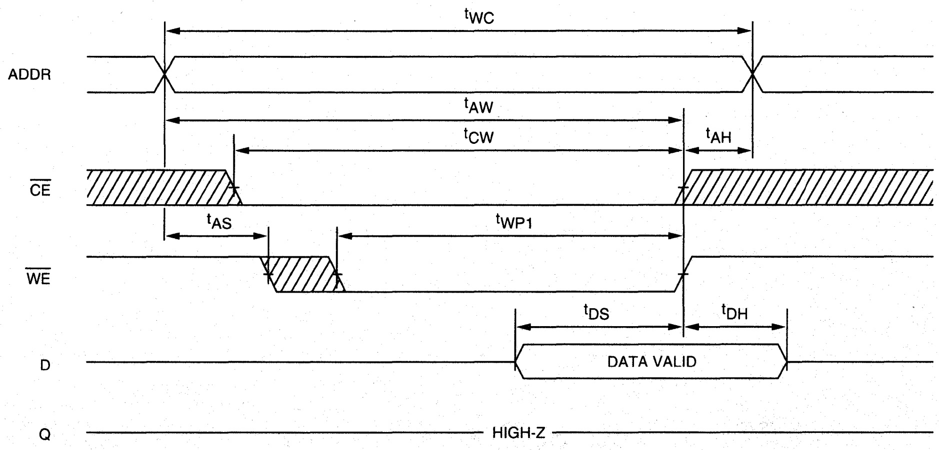


READ CYCLE NO. 2[7, 8, 10]



WRITE CYCLE NO. 1

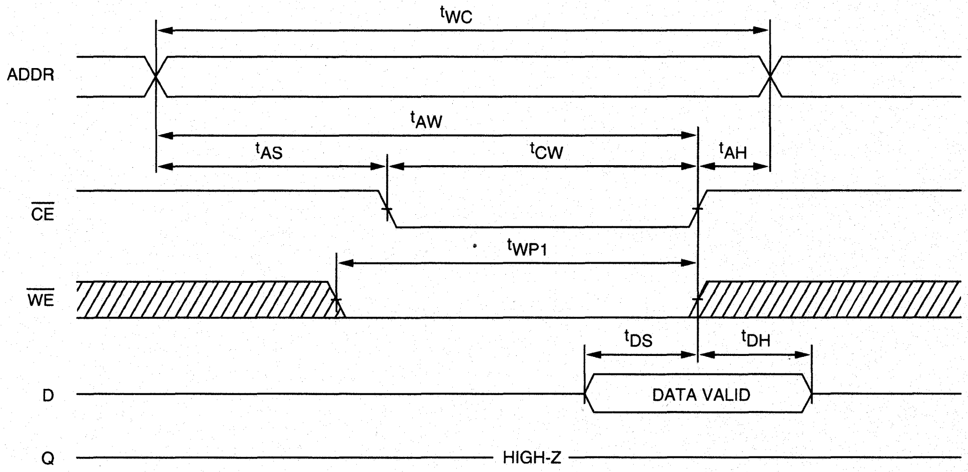
(Write Enable Controlled) [12]



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 2

(Chip Enable Controlled)

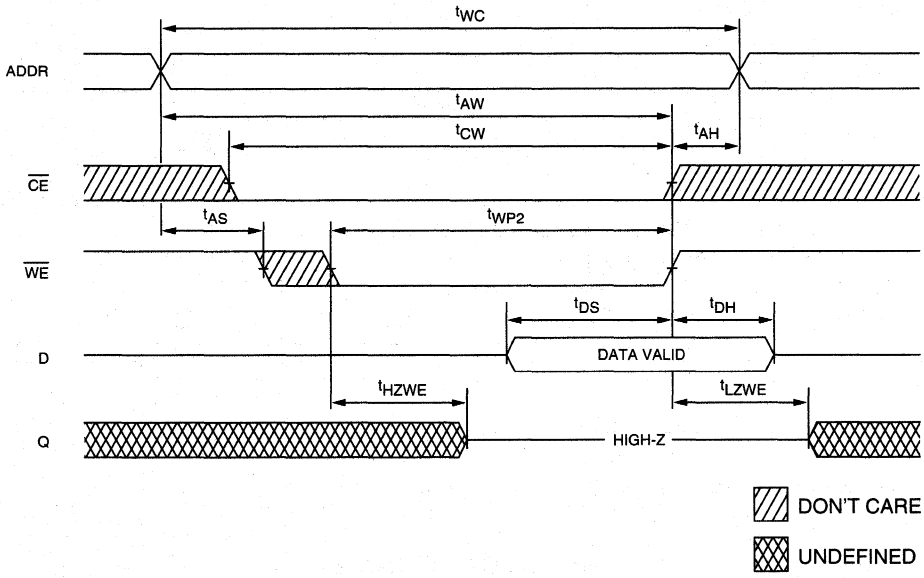


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 3

(Write Enable Controlled)[7, 12]



SRAM

32K x 8 SRAM

FEATURES

- High speed: 15, 20, 25, 30, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
Plastic SOJ (300 mil)	DJ
Plastic ZIP	Z
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

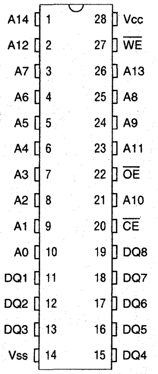
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) on this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

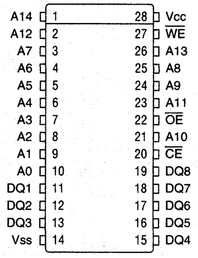
All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

PIN ASSIGNMENT (Top View)

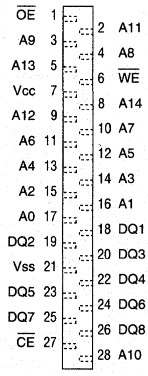
28-Pin DIP
(A-9, A-11)



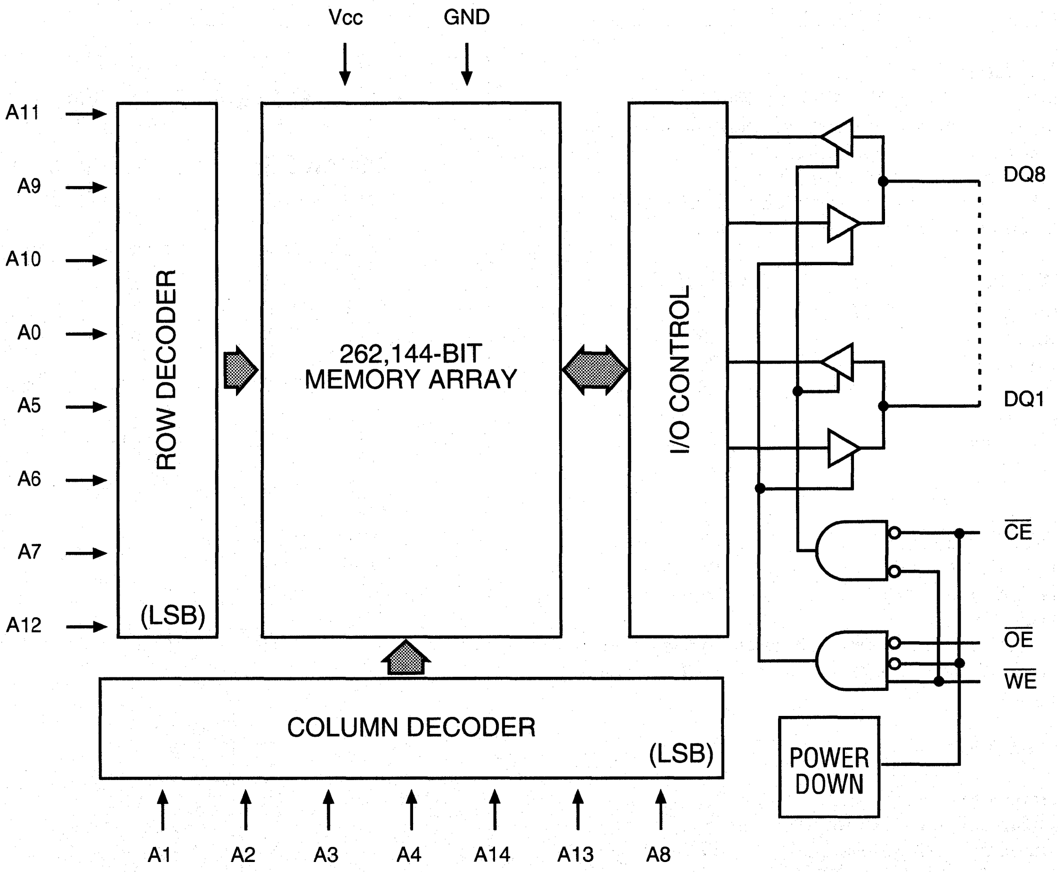
28-Pin SOJ
(E-8)



28-Pin ZIP
(C-5)



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	$V_{CC}+1$	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	$I_{OH} = -4.0mA$	V_{OH}	2.4		V	1
Output Low Voltage	$I_{OL} = 8.0mA$	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX						UNITS	NOTES
				-15	-20	-25	-30	-35	-45		
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ${}^tRC$ Outputs Open	I_{CC}	75	140	120	110	95	90	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ${}^tRC$ Outputs Open	I_{SB1}	11	30	30	25	25	25	25	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	.04	5	5	5	5	7	7	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	6	pF	4
Output Capacitance		C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-15		-20		-25		-30		-35		-45			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle															
READ cycle time	^{t}RC	15		20		25		30		35		45		ns	
Address access time	^{t}AA		15		20		25		30		35		45	ns	
Chip Enable access time	^{t}ACE		15		20		25		30		35		45	ns	
Output hold from address change	^{t}OH	3		3		5		5		5		5		ns	
Chip Enable to output in Low-Z	^{t}LZCE	4		6		6		6		6		6		ns	
Chip disable to output in High-Z	^{t}HZCE		8		9		9		12		15		18	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		15		20		25		30		35		45	ns	
Output Enable access time	^{t}AOE		8		8		8		10		12		15	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		0		0		ns	
Output disable to out put in High-Z	^{t}HZOE		6		7		7		10		12		15	ns	
WRITE Cycle															
WRITE cycle time	^{t}WC	15		20		20		25		30		35		ns	
Chip Enable to end of write	^{t}CW	10		15		15		18		20		25		ns	
Address valid to end of write	^{t}AW	10		15		15		18		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		0		ns	
WRITE pulse width	^{t}WP1	10		15		15		18		20		25		ns	
WRITE pulse width	^{t}WP2	12		15		15		18		20		25		ns	
Data setup time	^{t}DS	7		10		10		12		15		20		ns	
Data hold time	^{t}DH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	4		5		5		5		5		5		ns	
Write Enable to output in High-Z	^{t}HZWE		7		10		10		12		15		18	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

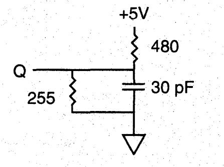


Fig. 1 OUTPUT LOAD EQUIVALENT

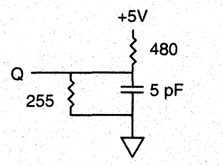


Fig. 2 OUTPUT LOAD EQUIVALENT

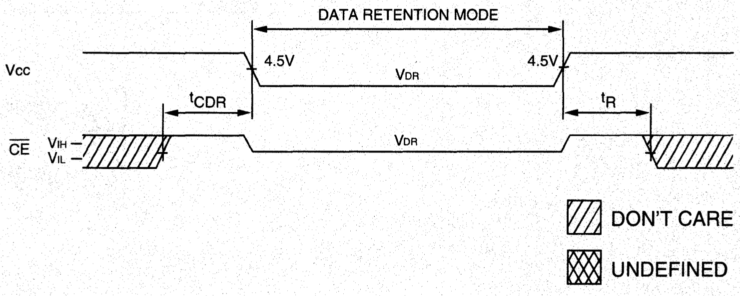
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-175.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

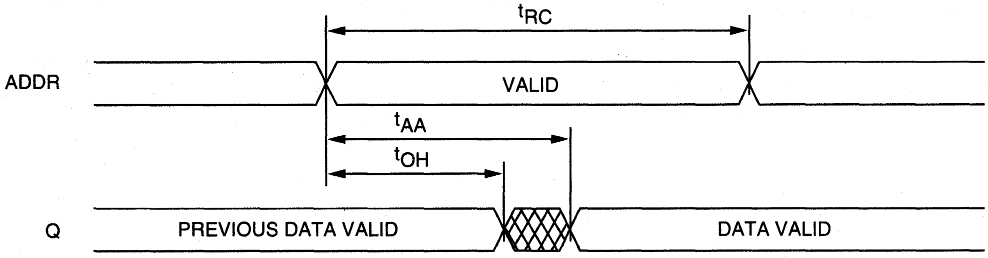
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	300	µA	
		Vcc = 3V			350	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

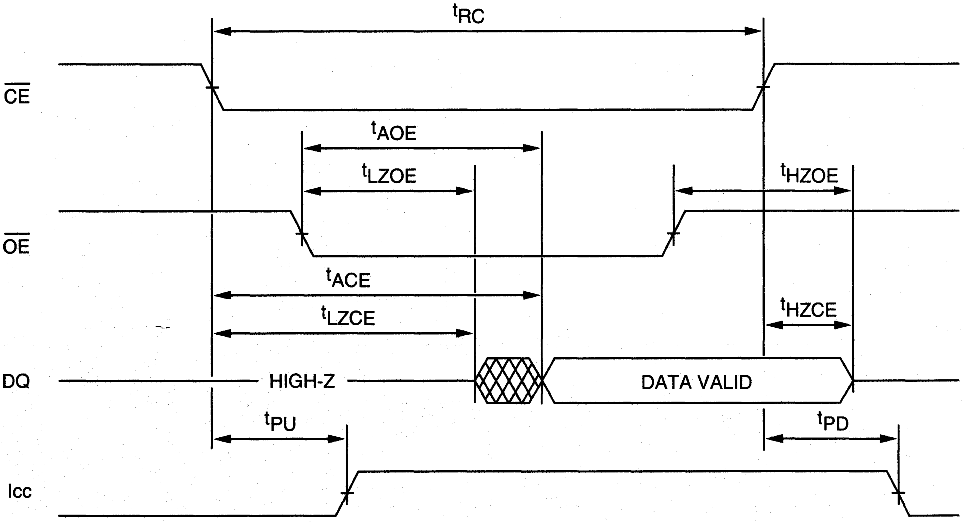
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1[8, 9]



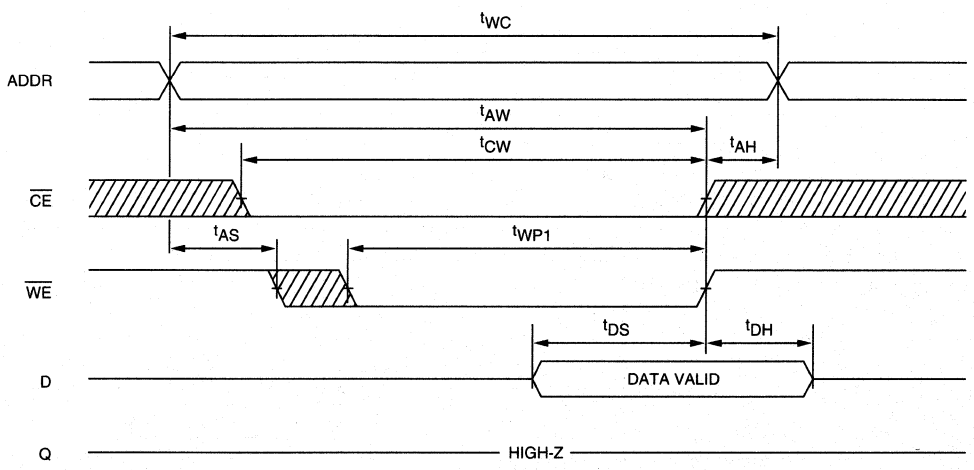
READ CYCLE NO. 2[7, 8, 10]



▨ DON'T CARE

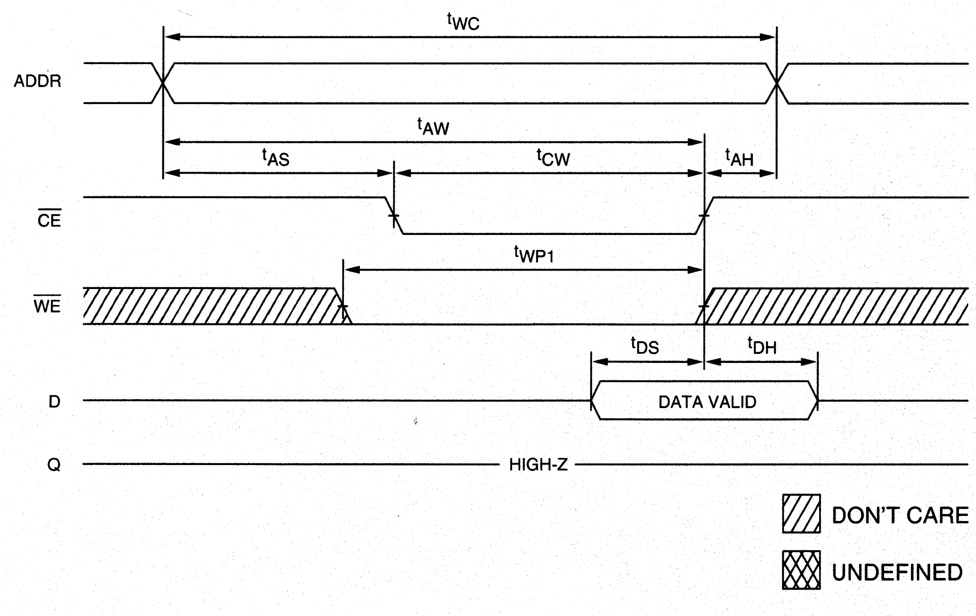
▩ UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled) [12]

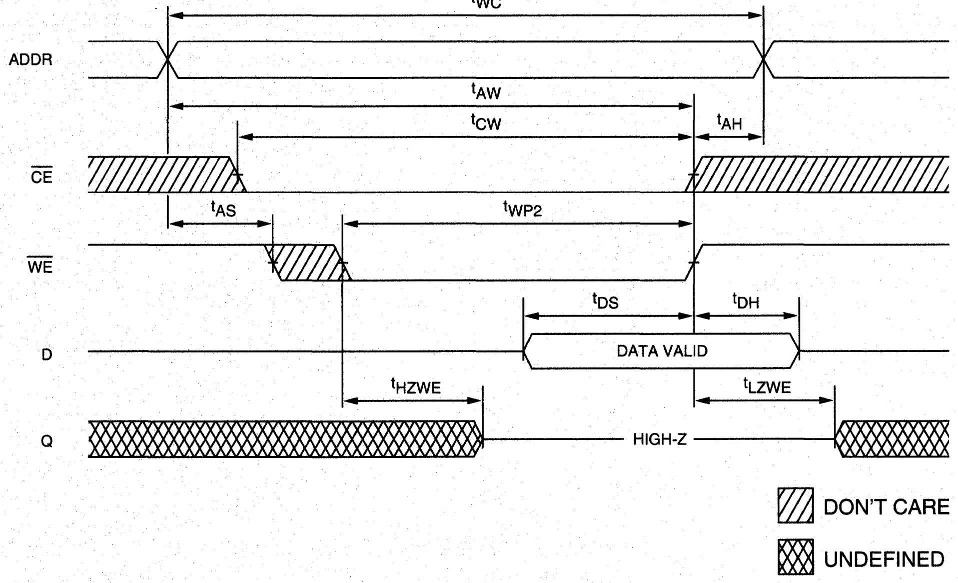


NOTE: Output enable (OE) is inactive (HIGH).

WRITE CYCLE NO. 2
(Chip Enable Controlled)



WRITE CYCLE NO. 3
(Write Enable Controlled) 7, 12



SRAM

128K x 8 SRAM

WITH OUTPUT ENABLE

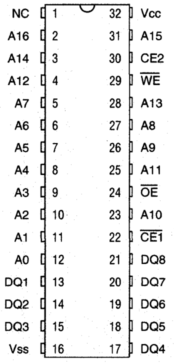
FEATURES

- High speed: 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast Output Enable access time: 8ns

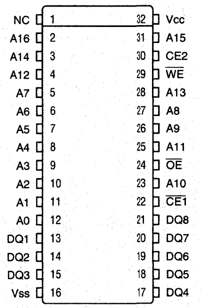
OPTIONS	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (400 mil)	None
Plastic DIP (600 mil)	W
Plastic SOJ (400 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

32-Pin DIP
(A-12, A-13)



32-Pin SOJ
(E-11)



GENERAL DESCRIPTION

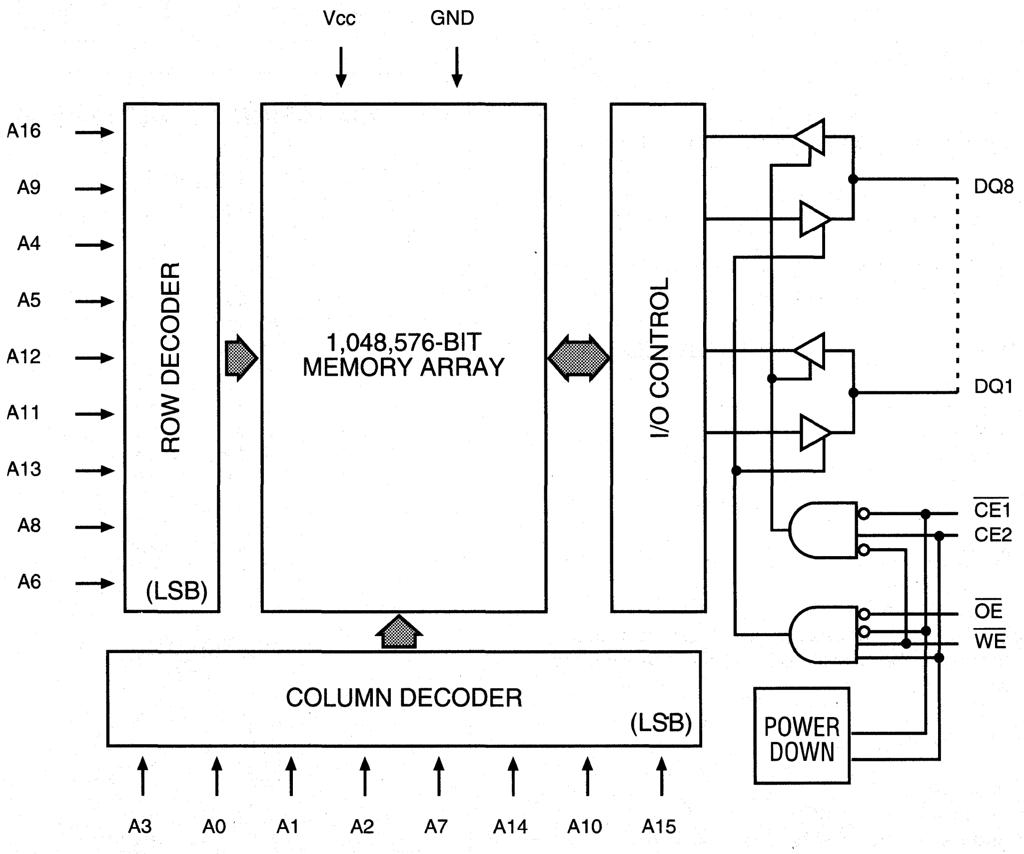
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2). This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A8 and A6) are encoded using a gray code.

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
READ	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	$I_{OH} = -4.0mA$	V_{OH}	2.4		V	1
Output Low Voltage	$I_{OL} = 8.0mA$	V_{OL}		0.4	V	1

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	95	140	125	115	110	mA	3, 15
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	17	35	30	25	25	mA	15
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	15
"L" version only	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.3	1.5	1.5	1.5	1.5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	8	pF	4
Output Capacitance		C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 14) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^{t}RC	20		25		35		45		ns	
Address access time	^{t}AA		20		25		35		45	ns	
Chip Enable access time	^{t}ACE		20		25		35		45	ns	
Output hold from address change	^{t}OH	5		5		5		5		ns	
Chip Enable to output in Low-Z	^{t}LZCE	5		5		5		5		ns	
Chip disable to output in High-Z	^{t}HZCE		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		20		25		35		45	ns	
Output Enable access time	^{t}AOE		6		8		12		15	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		ns	
Output disable to output in High-Z	^{t}HZOE		6		10		12		15	ns	6
WRITE Cycle											
WRITE cycle time	^{t}WC	20		25		35		45		ns	
Chip Enable to end of write	^{t}CW	12		15		20		25		ns	
Address valid to end of write	^{t}AW	12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		ns	
WRITE pulse width	^{t}WP1	12		15		20		25		ns	
WRITE pulse width	^{t}WP2	15		15		20		25		ns	
Data setup time	^{t}DS	8		10		15		20		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	5		5		5		5		ns	
Write Enable to output in High-Z	^{t}HZWE	0	8	0	10	0	15	0	18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

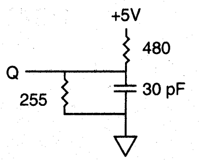


Fig. 1 OUTPUT LOAD EQUIVALENT

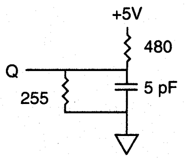


Fig. 2 OUTPUT LOAD EQUIVALENT

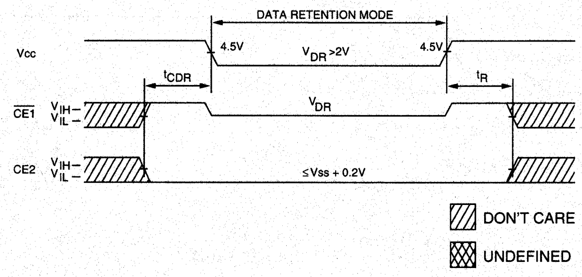
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. CE2 timing is the same as $\overline{\text{CE1}}$ timing. The wave form is inverted.
13. Chip enable ($\overline{\text{CE1}}$, CE2) and write enable ($\overline{\text{WE}}$) can initiate and terminate a WRITE cycle.
14. For automotive, industrial and extended temperature specifications, refer to page 1-177.
15. Typical values are measured at 5V, 25°C and 25ns cycle time.

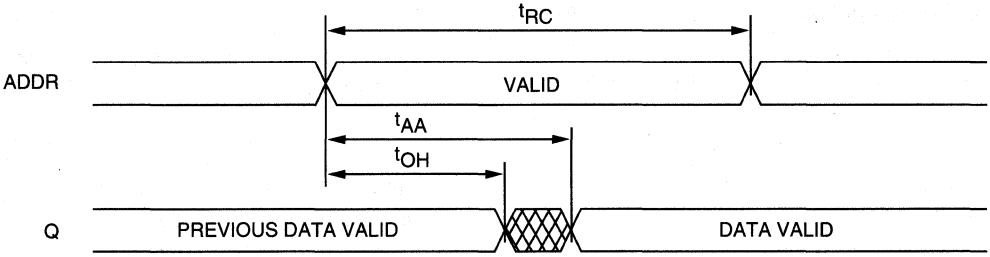
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{\text{CE1}}$ ≥ (Vcc -0.2V) or CE2 ≤ (Vss +0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		35	200	µA	
		Vcc = 3V			70	400	µA	
		Vcc = 5V			250	1,300	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

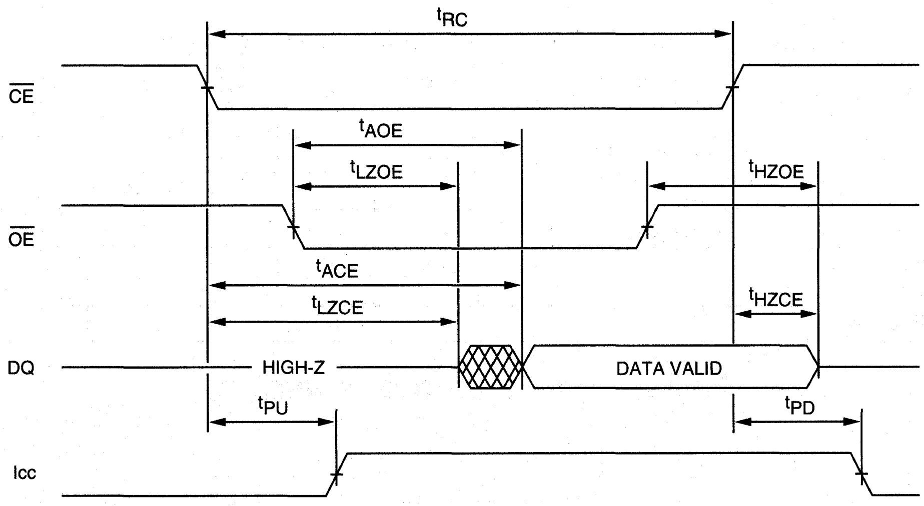
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10, 12]

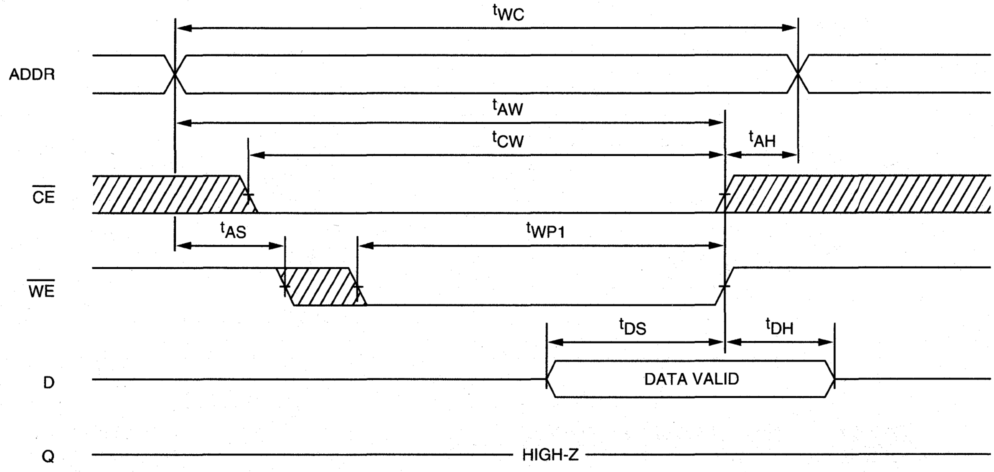


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 1

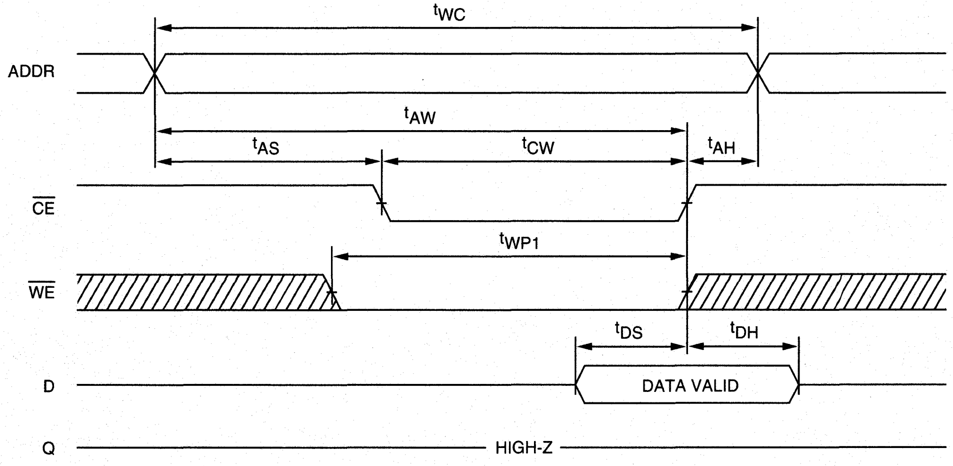
(Write Enable Controlled)[12, 13]



NOTE: Output enable (OE) is inactive (HIGH).

WRITE CYCLE NO. 2

(Chip Enable Controlled)[12]

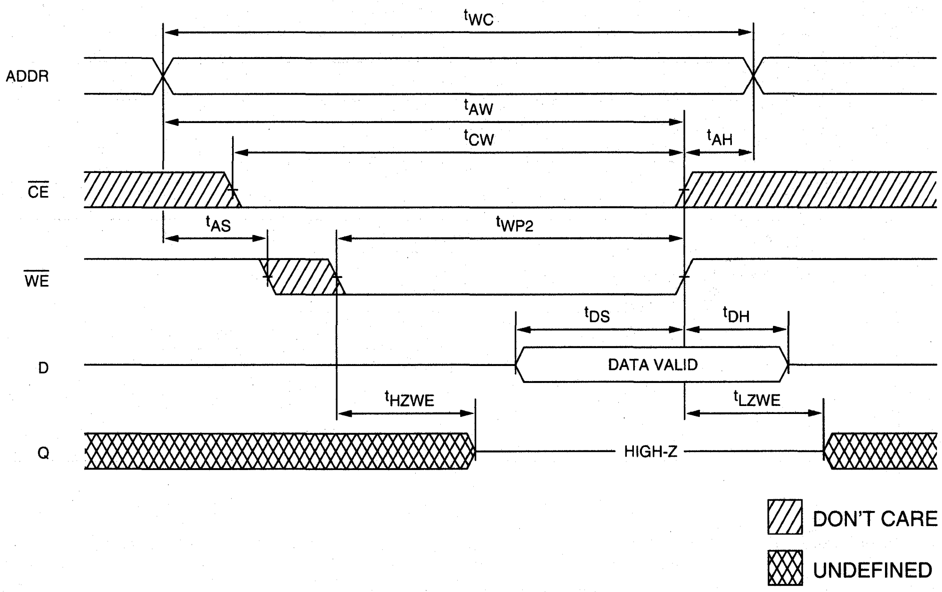


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 3

(Write Enable Controlled)[7, 12, 13]



MICRON
TECHNOLOGY, INC.

MT5C1009

SRAM

128K x 8 SRAM

WITH SINGLE CHIP ENABLE

FEATURES

- High speed: 20, 25, 35, 45, 55 and 70ns
- Automatic Chip Enable power down
- All inputs and outputs are TTL compatible
- High-performance, low-power CMOS double-metal process
- Single +5V ±10% power supply
- Fast Output Enable access time: 8ns
- Replaces industry standard 128K x 8 multichip SRAM module

OPTIONS

OPTIONS	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
55ns access	-55*
70ns access	-70*

*Electrical characteristics identical to those provided for the 45ns device.

• Packages	
Plastic DIP (400 mil)	None
Plastic DIP (600 mil)	W
Plastic SOJ (400 mil)	DJ

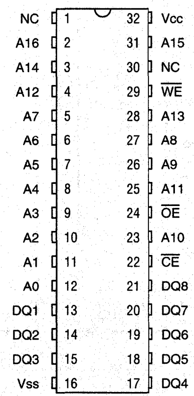
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***

• 2V data retention	L

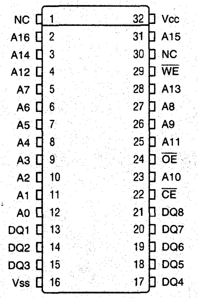
• Temperature		
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

32-Pin DIP
(A-12, A-13)



32-Pin SOJ
(E-11)



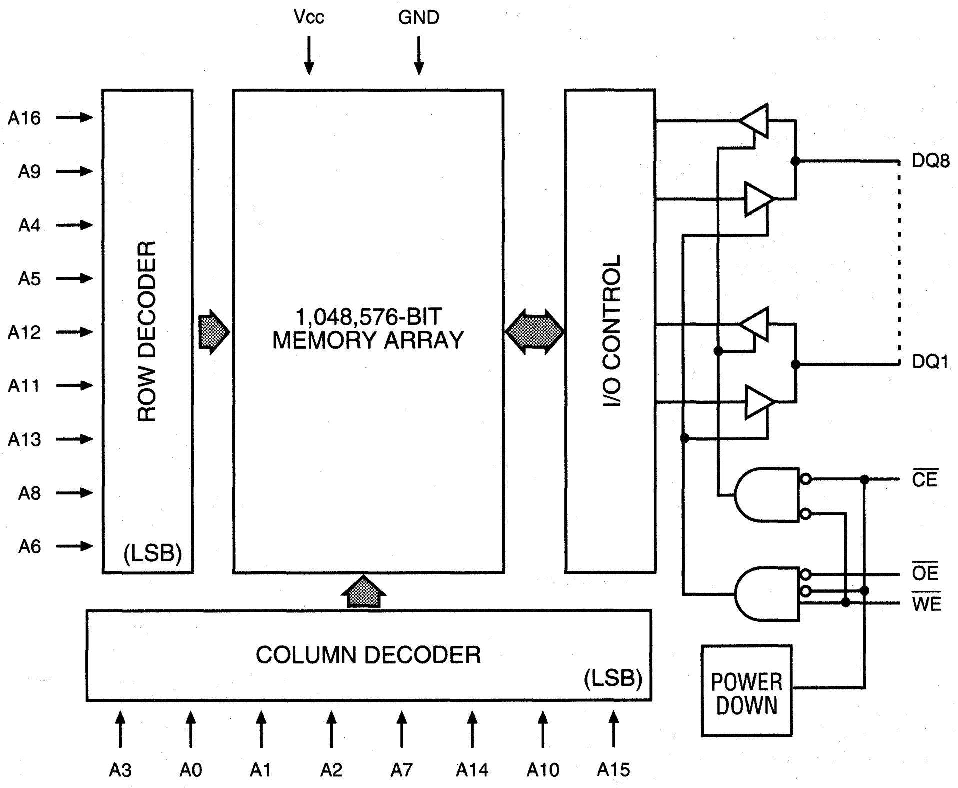
GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A8 and A6) are encoded using a gray code.

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	95	140	125	115	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	17	35	30	25	25	mA	14
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IL} ≤ Vss +0.2V V_{IH} ≥ Vcc -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	14
"L" version only	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IL} ≤ Vss +0.2V V_{IH} ≥ Vcc -0.2V; f = 0	I_{SB2}	0.3	1.5	1.5	1.5	1.5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	C_I	8	pF	4
Output Capacitance		C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^{t}RC	20		25		35		45		ns	
Address access time	^{t}AA		20		25		35		45	ns	
Chip Enable access time	^{t}ACE		20		25		35		45	ns	
Output hold from address change	^{t}OH	5		5		5		5		ns	
Chip Enable to output in Low-Z	^{t}LZCE	5		5		5		5		ns	
Chip disable to output in High-Z	^{t}HZCE		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		20		25		35		45	ns	
Output Enable access time	^{t}AOE		6		8		12		15	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		ns	
Output disable to output in High-Z	^{t}HZOE		6		10		12		15	ns	6
WRITE Cycle											
WRITE cycle time	^{t}WC	20		25		35		45		ns	
Chip Enable to end of write	^{t}CW	12		15		20		25		ns	
Address valid to end of write	^{t}AW	12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		ns	
WRITE pulse width	^{t}WP1	12		15		20		25		ns	
WRITE pulse width	^{t}WP2	15		15		20		25		ns	
Data setup time	^{t}DS	8		10		15		20		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	5		5		5		5		ns	
Write Enable to output in High-Z	^{t}HZWE	0	8	0	10	0	15	0	18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

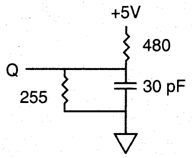


Fig. 1 OUTPUT LOAD EQUIVALENT

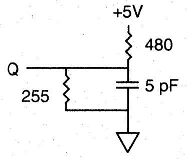


Fig. 2 OUTPUT LOAD EQUIVALENT

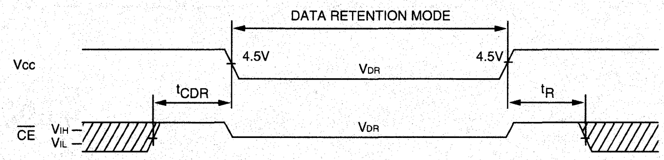
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{{}^{t}\text{RC (MIN)}}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-177.
14. Typical values are measured at 5V, 25°C and 25ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{\text{CE}}$ ≥ (Vcc -0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		35	200	µA	
		Vcc = 3V			70	400	µA	
		Vcc = 5V			250	1,300	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

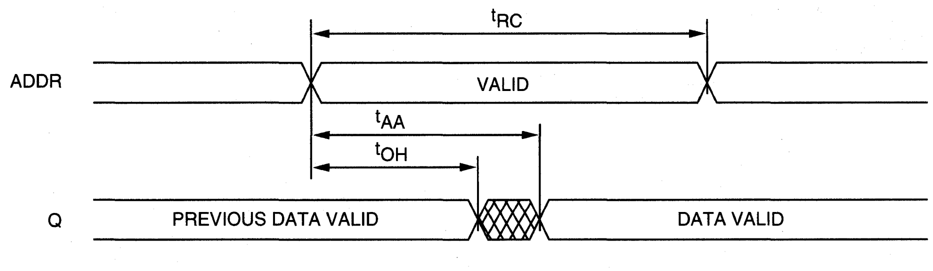
LOW Vcc DATA RETENTION WAVEFORM



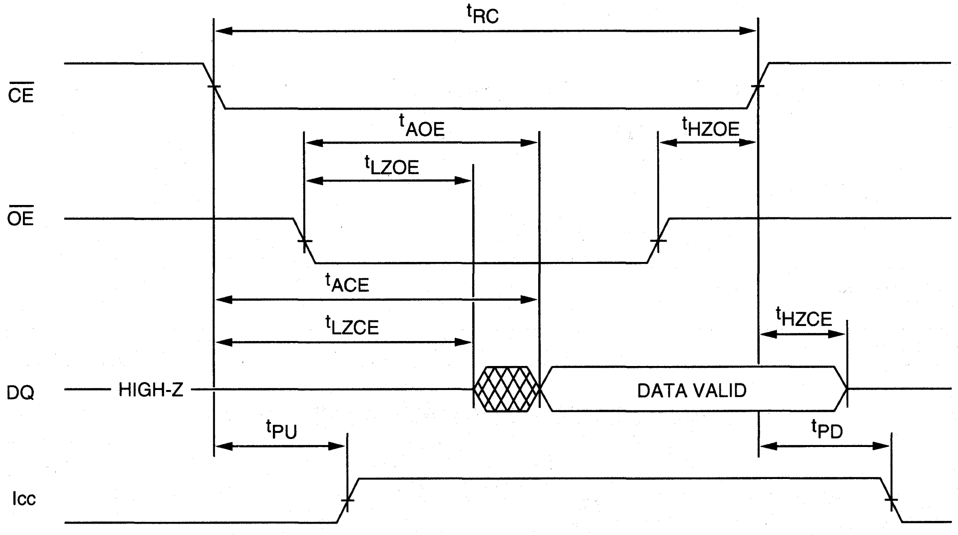
▨ DON'T CARE

▩ UNDEFINED

READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10]

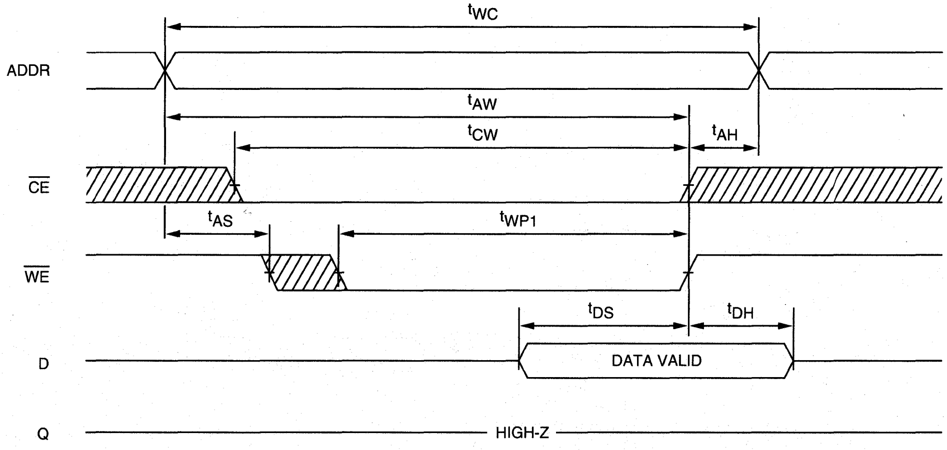


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 1

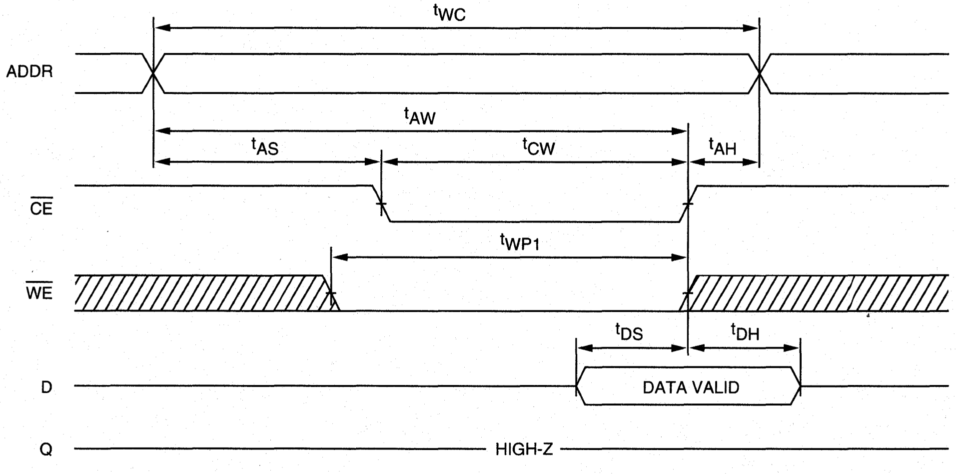
(Write Enable Controlled) [12]



NOTE: Output enable (OE) is inactive (HIGH).

WRITE CYCLE NO. 2

(Chip Enable Controlled)

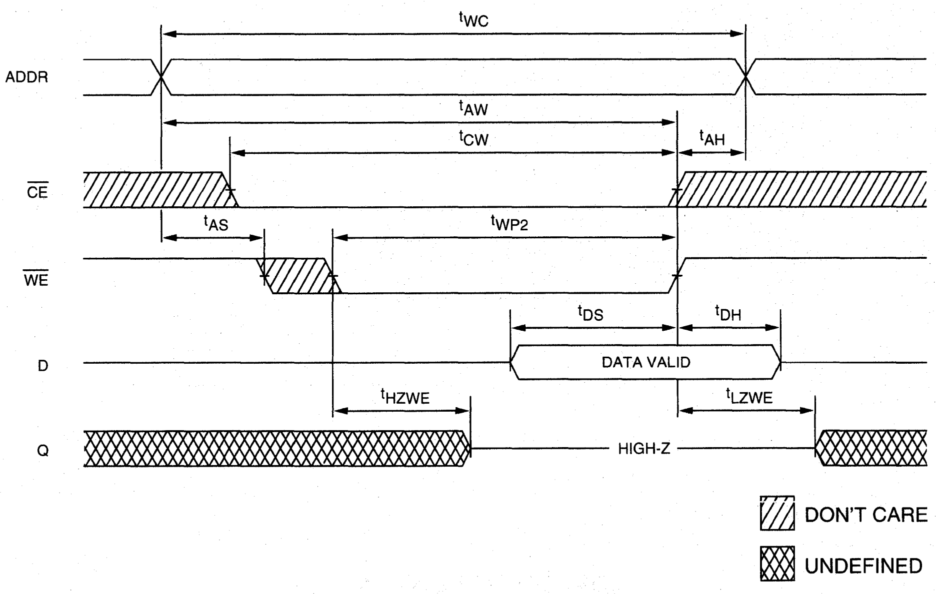


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 3

(Write Enable Controlled)[7, 12]



SRAM

512K x 8 SRAM

WITH OUTPUT ENABLE

FEATURES

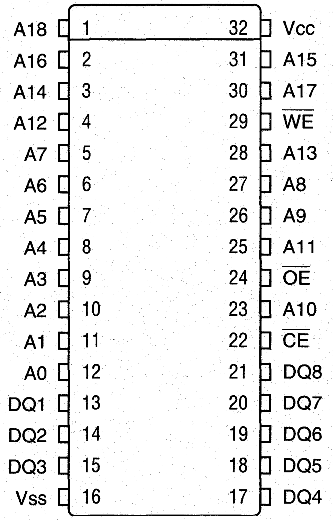
- High speed: 20, 25, 35 and 55ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast Output Enable access time: 8ns

OPTIONS

OPTIONS		MARKING
• Timing		
20ns access		-20
25ns access		-25
35ns access		-35
55ns access		-55
• Packages		
Plastic SOJ (400 mil)		DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***		
• 2V data retention		L
• Temperature		
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(E-11)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

ADVANCE

MICRON TECHNOLOGY, INC.

MT5C4108

SRAM

512K x 8 SRAM

WITH OUTPUT ENABLE

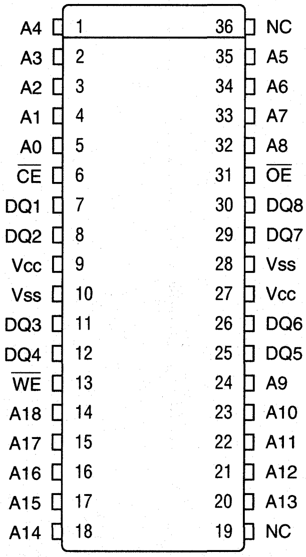
FEATURES

- High speed: 12, 15 and 17ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast Output Enable access time: 6ns

OPTIONS		MARKING
• Timing		
12ns access		-12
15ns access		-15
17ns access		-17
• Packages		
Plastic SOJ (400 mil)		DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***		
• 2V data retention		L
• Temperature		
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

36-Pin SOJ



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center power and ground poins for very high performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

SRAM

32K x 9 SRAM

FEATURES

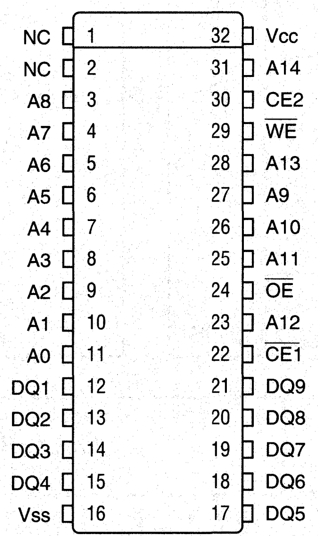
- High speed: 15, 17, 20 and 25ns
- High-performance, low-power CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

OPTIONS	MARKING
• Timing	
15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
• Packages	
Plastic SOJ (300 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(E-10)



GENERAL DESCRIPTION

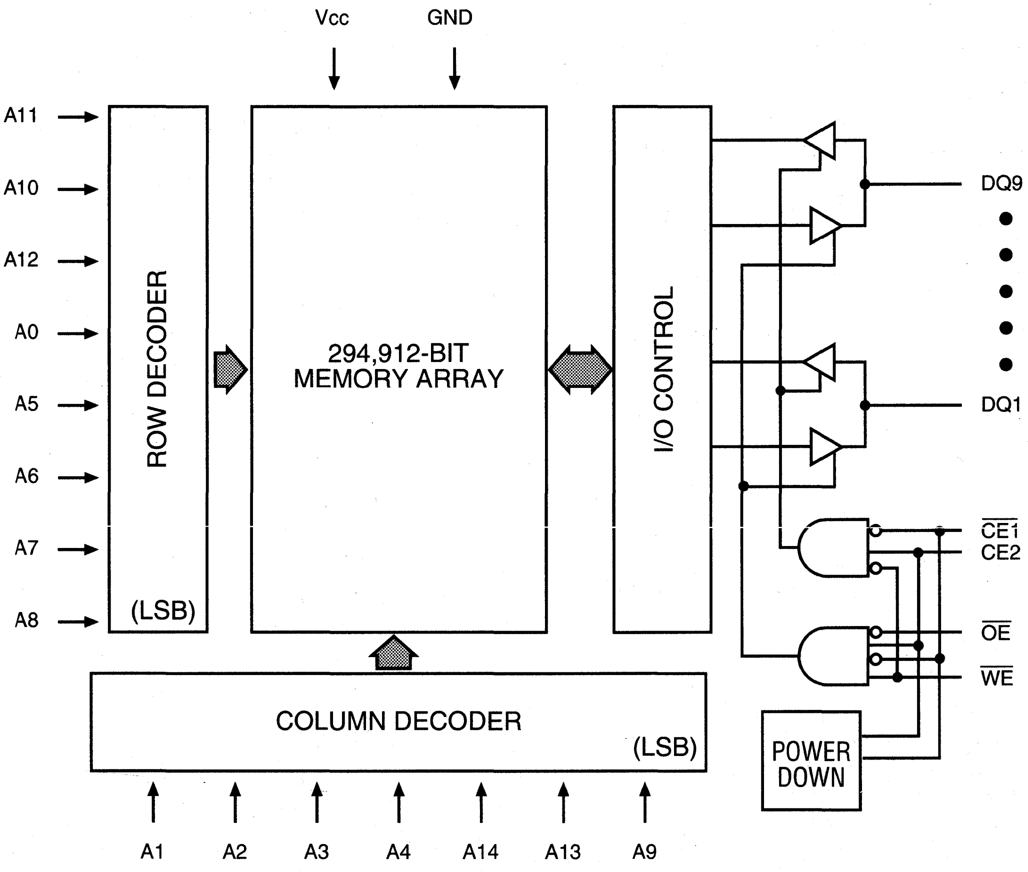
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. They are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2) and output enable ($\overline{OE}$) control signals. This enhancement can place the outputs in High-Z for additional flexibility in system design. The dual chip enables may be used to directly address multiple banks of SRAM without external logic.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW while CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH while $\overline{CE1}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
READ	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	-1V to +7V
Storage Temperature	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-15**	**-17**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE1} \le V_{IL}$; CE2, $\ge V_{IH}$ f = MAX = 1/ᵗRC Vcc = MAX; Outputs Open	I_{CC}	75	145	130	120	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE1} \ge V_{IH}$; CE2 $\le V_{IL}$ f = MAX = 1/ᵗRC Vcc = MAX; Outputs Open	I_{SB1}	11	35	35	30	30	mA	14
	$\overline{CE1} \ge V_{CC} - 0.2$; Vcc = MAX CE2 and $V_{IL} \le V_{SS} + 0.2$ $V_{IH} \ge V_{CC} - 0.2$; f = 0	I_{SB2}	0.5	7	7	7	7	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz	C_I	7	pF	4
Output Capacitance	Vcc = 5V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C, Vcc = 5V ±10%)

DESCRIPTION		-15		-17		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^{t}RC	15		17		20		25		ns	
Address access time	^{t}AA		15		17		20		25	ns	
Chip Enable access time	^{t}ACE		15		17		20		25	ns	
Output hold from address change	^{t}OH	3		3		3		5		ns	
Chip Enable to output in Low-Z	^{t}LZCE	4		4		4		4		ns	7
Chip disable to output in High-Z	^{t}HZCE		8		8		8		8	ns	6, 7
Chip Enable to power up time	^{t}PU	0		0		0		0		ns	
Chip disable to power down time	^{t}PD		15		17		20		25	ns	
Output Enable access time	^{t}AOE		8		8		8		8	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		ns	
Output disable to out put in High-Z	^{t}HZOE		7		7		7		7	ns	6
WRITE Cycle											
WRITE cycle time	^{t}WC	15		17		20		25		ns	
Chip Enable to end of write	^{t}CW	10		13		15		20		ns	
Address valid to end of write	^{t}AW	10		13		15		20		ns	
Address setup time	^{t}AS	0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		ns	
WRITE pulse width	^{t}WP1	10		13		15		20		ns	
WRITE pulse width	^{t}WP2	12		13		15		20		ns	
Data setup time	^{t}DS	7		8		10		10		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	4		4		4		4		ns	7
Write Enable to output in High-Z	^{t}HZWE	0	7	0	8	0	10	0	10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

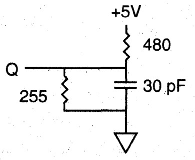


Fig. 1 OUTPUT LOAD EQUIVALENT

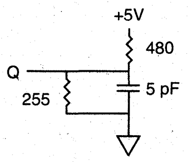


Fig. 2 OUTPUT LOAD EQUIVALENT

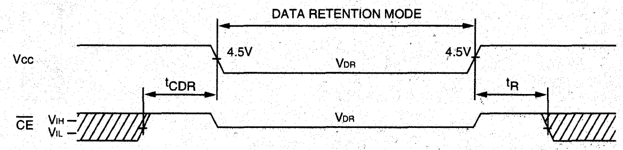
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. CE2 timing is identical to $\overline{CE1}$ timing. The waveform is inverted.
13. Either $\overline{CE1}$, CE2 or $\overline{WE}$ can initiate or terminate WRITE cycles.
14. For automotive, industrial and extended temperature specifications, refer to page 1-175.
15. Typical values are measured at 5V, 25°C and 20ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		200	400	µA	
		Vcc = 3V			300	500	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

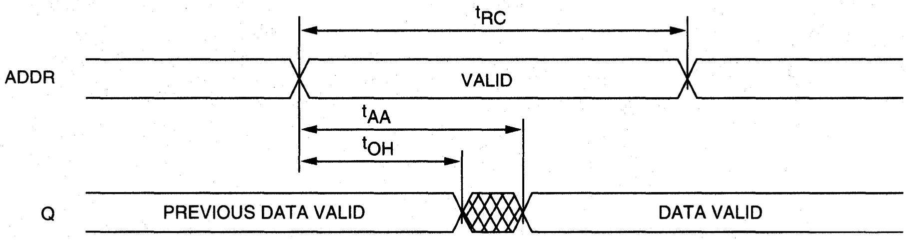
LOW Vcc DATA RETENTION WAVEFORM



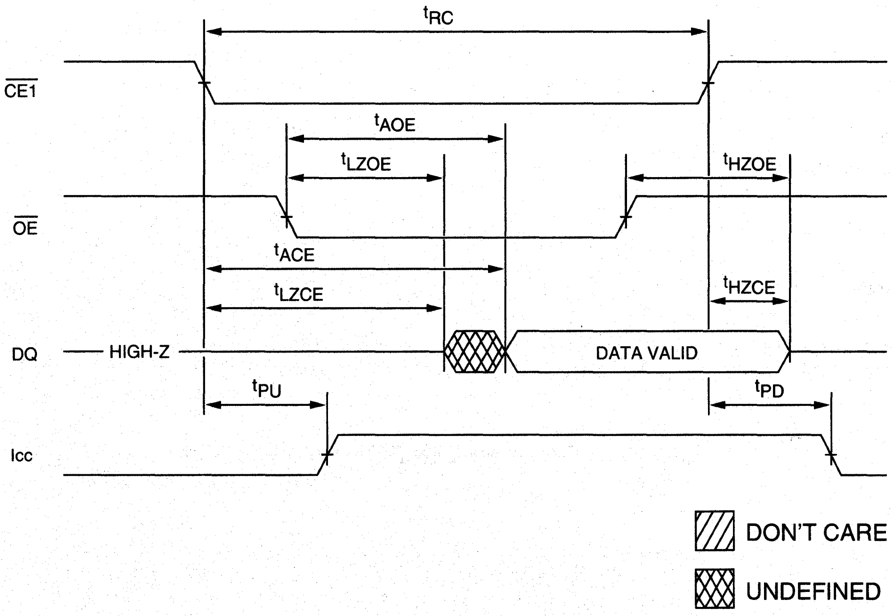
▨ DON'T CARE

▩ UNDEFINED

READ CYCLE NO. 1[8, 9]

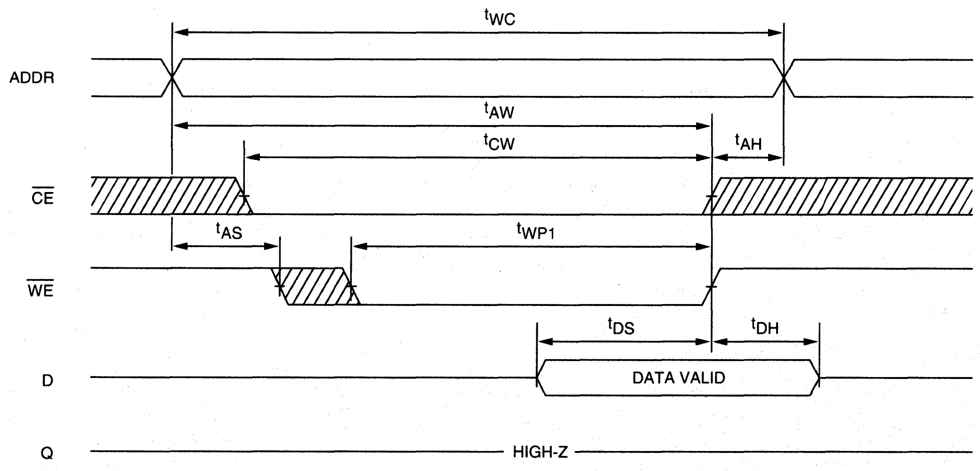


READ CYCLE NO. 2[7, 8, 10, 12]



WRITE CYCLE NO. 1

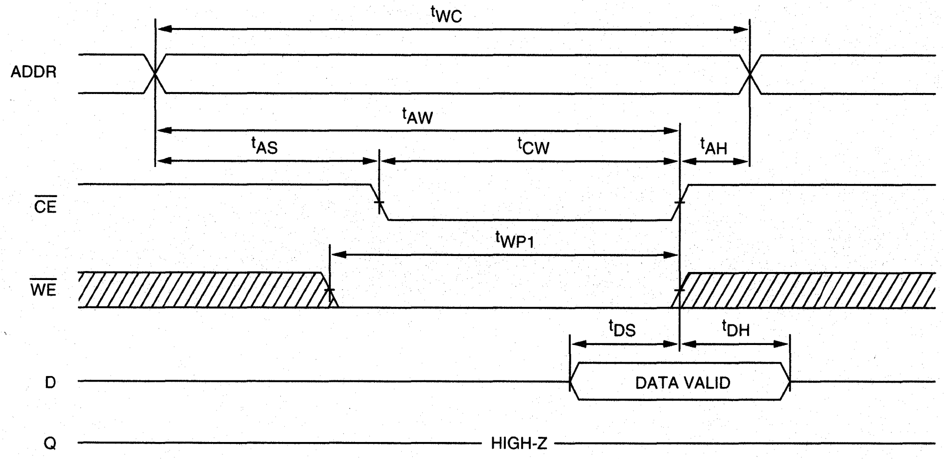
(Write Enable Controlled) 12



NOTE: Output enable (OE) is inactive (HIGH).

WRITE CYCLE NO. 2

(Chip Enable Controlled) 12

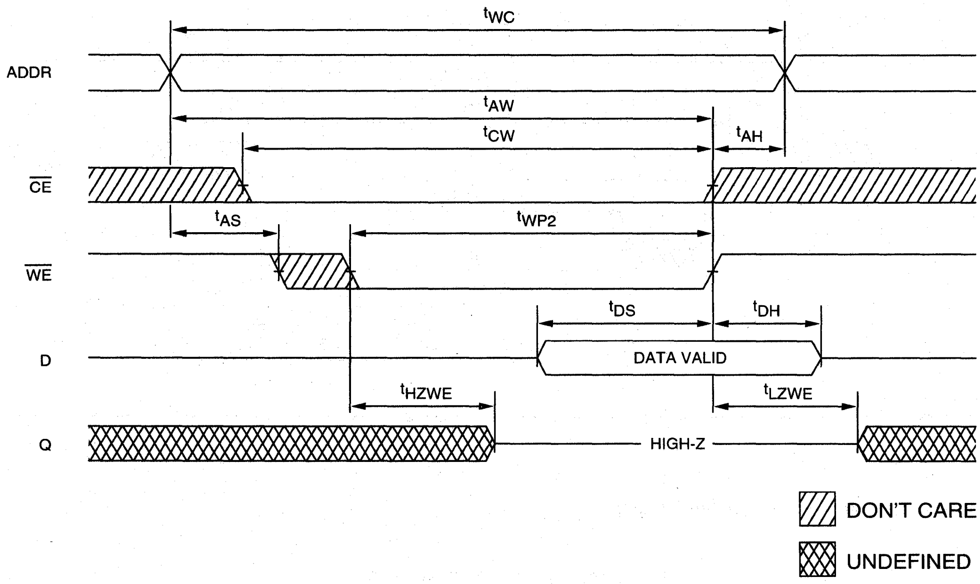


▨ DON'T CARE

▦ UNDEFINED

WRITE CYCLE NO. 3

(Write Enable Controlled) 7, 12, 13



SRAM

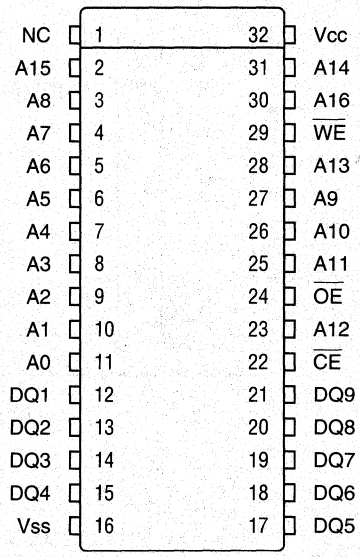
128K x 9 SRAM
WITH SINGLE CHIP ENABLE

FEATURES
- High speed: 17, 20, 25 and 35ns
- Automatic Chip Enable power down
- All inputs and outputs are TTL compatible
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Fast Output Enable access time: 6ns

OPTIONS	MARKING
• Timing	
17ns access	-17
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic SOJ (400 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(E-11)



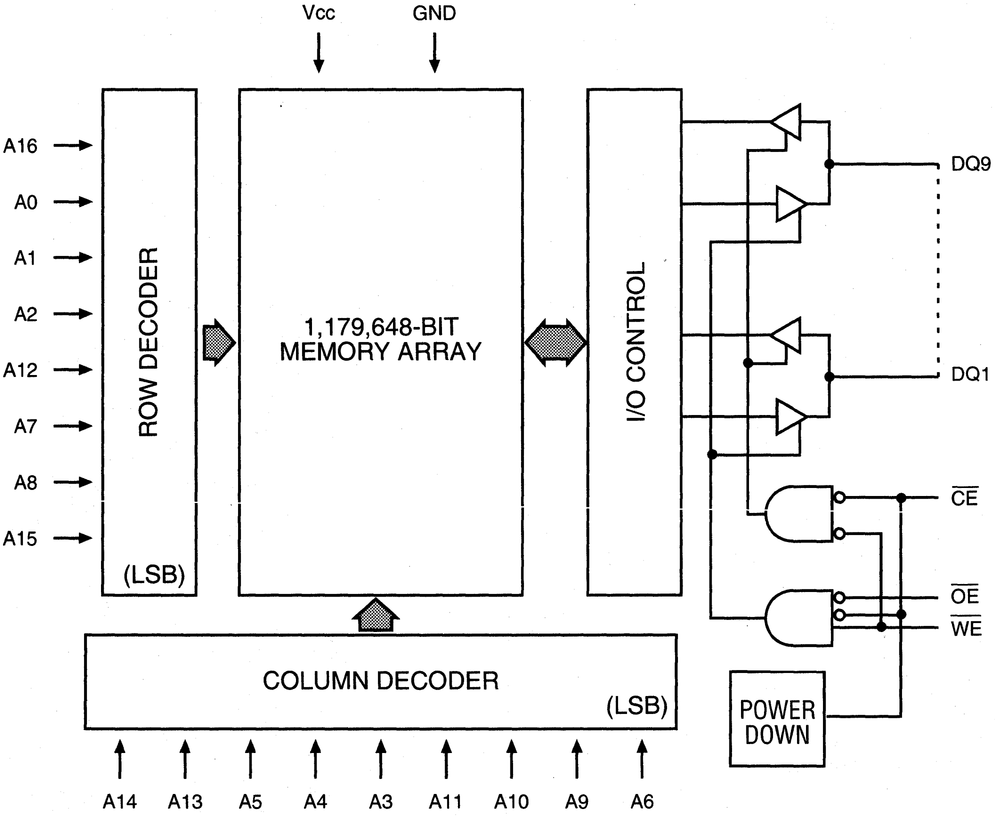
GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

Writing to these devices is accomplished when write enable ($\overline{\text{WE}}$) and $\overline{\text{CE}}$ inputs are both LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH and $\overline{\text{CE}}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_C \le 70°C$; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-17**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	95	160	140	125	115	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	17	40	35	30	25	mA	14
	$\overline{CE} \ge$ (Vcc -0.2V); Vcc = MAX All Other Inputs ≤ 0.2V or ≥ (Vcc -0.2V); f = 0Hz	I_{SB2}	0.4	5	5	5	5	mA	14
"L" version only	$\overline{CE} \ge$ (Vcc -0.2V); Vcc = MAX All Other Inputs ≤ 0.2V or ≥ (Vcc -0.2V); f = 0Hz	I_{SB2}	0.3	1.5	1.5	1.5	1.5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	C_I	6	pF	4
Output Capacitance		C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_C ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-17		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
READ cycle time	^{t}RC	17		20		25		35		ns	
Address access time	^{t}AA		17		20		25		35	ns	
Chip Enable access time	^{t}ACE		17		20		25		35	ns	
Output hold from address change	^{t}OH	5		5		5		5		ns	
Chip Enable to output in Low-Z	^{t}LZCE	5		5		5		5		ns	
Chip disable to output in High-Z	^{t}HZCE		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		17		20		25		35	ns	
Output Enable access time	^{t}AOE		5		6		8		12	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		ns	
Output disable to output in High-Z	^{t}HZOE		5		6		10		12	ns	6
WRITE Cycle											
WRITE cycle time	^{t}WC	17		20		25		35		ns	
Chip Enable to end of write	^{t}CW	10		12		15		20		ns	
Address valid to end of write	^{t}AW	10		12		15		20		ns	
Address setup time	^{t}AS	0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		ns	
WRITE pulse width	^{t}WP1	10		12		15		20		ns	
WRITE pulse width	^{t}WP2	13		15		15		20		ns	
Data setup time	^{t}DS	7		8		10		15		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	5		5		5		5		ns	
Write Enable to output in High-Z	^{t}HZWE	0	7	0	8	0	10	0	15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

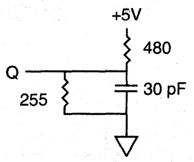


Fig. 1 OUTPUT LOAD EQUIVALENT

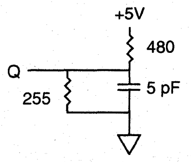


Fig. 2 OUTPUT LOAD EQUIVALENT

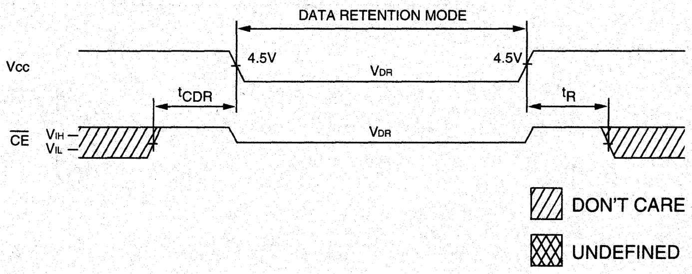
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{^{t}RC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-177.
14. Typical values are measured at 5V, 25°C and 25ns cycle time.

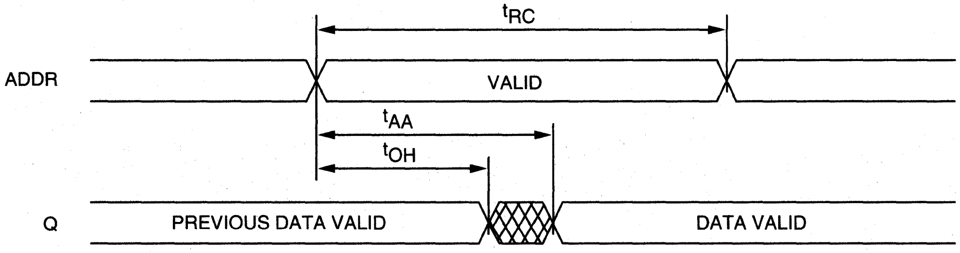
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		35	200	µA	
		Vcc = 3V			70	400	µA	
		Vcc = 5V			250	1,300	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

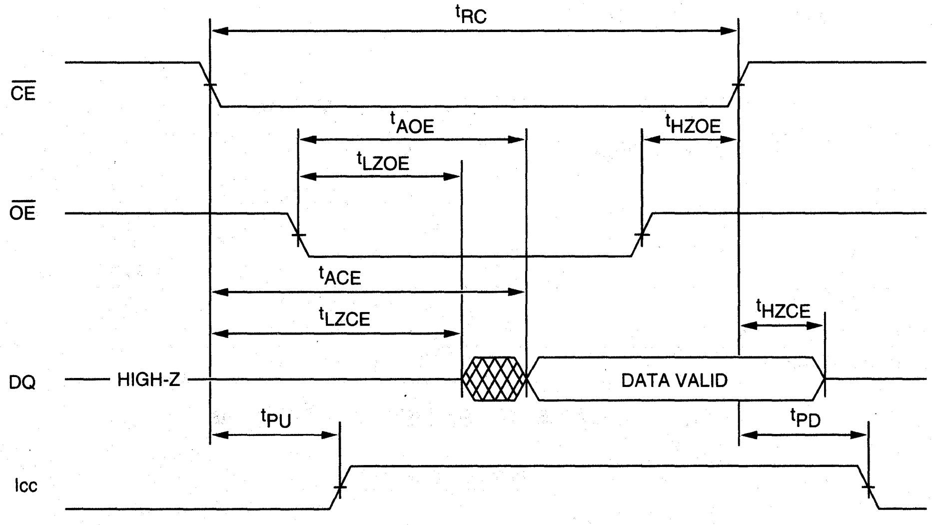
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1[8, 9]



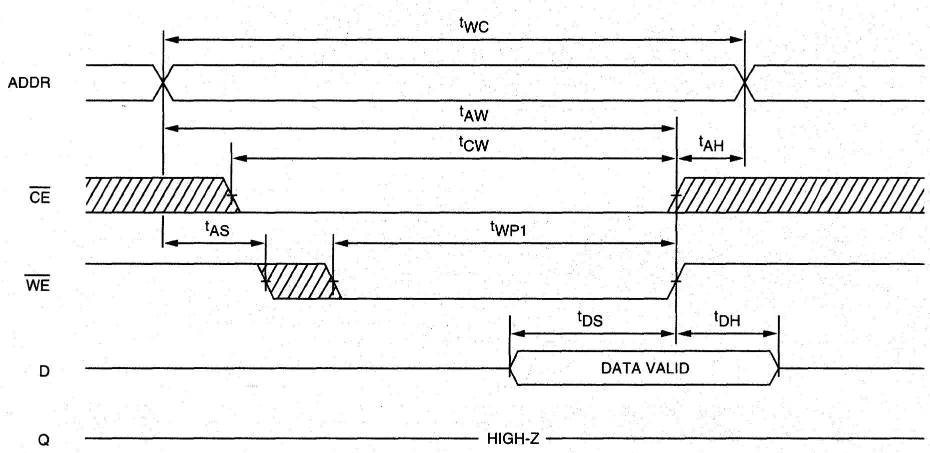
READ CYCLE NO. 2[7, 8, 10]



▨ DON'T CARE

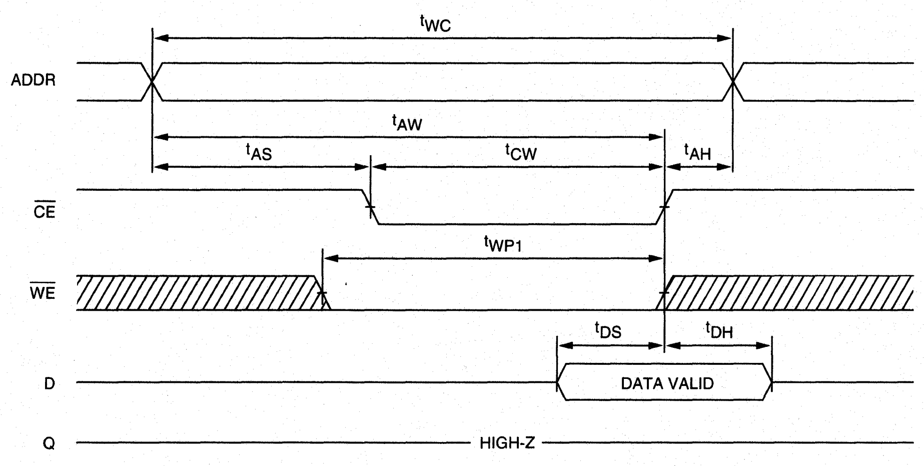
⊠ UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled)[12]



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 2
(Chip Enable Controlled)

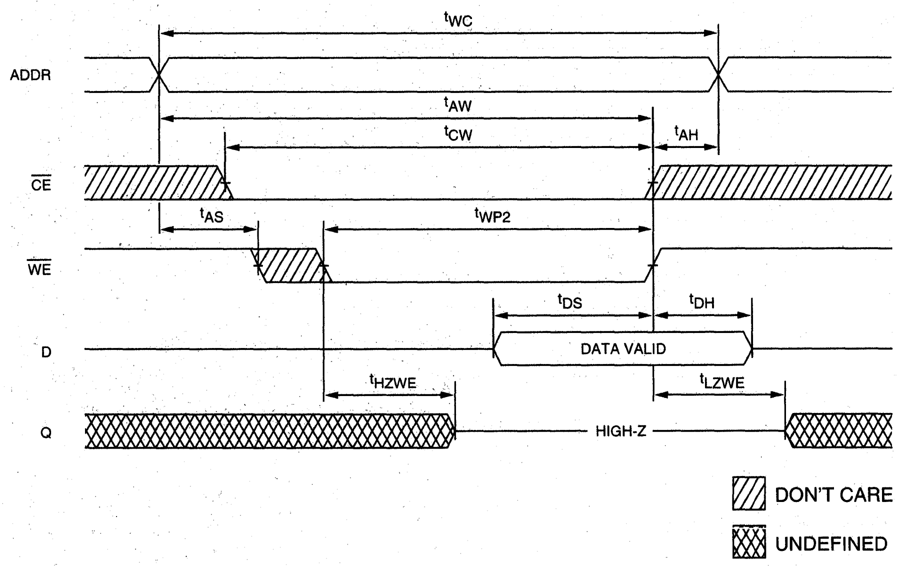


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 3

(Write Enable Controlled)[7, 12]



SRAM

256K x 16 SRAM

WITH OUTPUT ENABLE

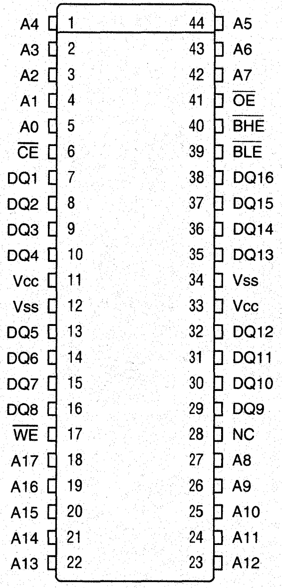
FEATURES

- High speed: 12, 15 and 17ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins
- Single +5V ±10% power supply
- Easy memory expansion with CE and OE options
- Separate upper and lower byte control (BHE, BLE)
- All inputs and outputs are TTL compatible
- Fast Output Enable access time: 6ns

OPTIONS	MARKING
• Timing	
12ns access	-12
15ns access	-15
17ns access	-17
• Packages	
Plastic SOJ (400 mil)	DJ
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book***.	
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

44-Pin SOJ



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center power and ground pins for very high performance. For flexibility in high-speed memory applications, Micron offers chip enable (CE) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH while output enable (OE) and CE go LOW. The high and low bytes of both the READ and WRITE operations are controlled by BHE and BLE respectively.

The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
**IT .... -40°C to +85°C
AT .... -40°C to +125°C
XT .... -55°C to +125°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-40°C \le T_A \le 85°C$; $-40°C \le T_A \le 125°C$; $-55°C \le T_A \le 125°C$; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX								
DESCRIPTION	CONDITIONS	SYMBOL	-8†	-10†	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; Vcc = MAX f = MAX = 1/ ᵗRC Outputs Open	I_{CC}	170	155	145	130	120	110	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; Vcc = MAX f = MAX = 1/ ᵗRC Outputs Open	I_{SB1}	65	60	55	45	40	35	35	mA	
	$\overline{CE} \ge$ Vcc -0.2V; Vcc = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge$ Vcc -0.2V; f = 0	I_{SB2}	5	5	5	5	5	5	5	mA	

† These are preliminary specifications.

DESCRIPTION	CONDITIONS		SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Data Retention	$\overline{CE} \ge$ (Vcc -0.2V) $V_{IN} \ge$ (Vcc -0.2V) or ≤ -0.2V	Vcc = 2V	I_{CCDR}	150	300	µA	
		Vcc = 3V		300	550	µA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	C_I	5††	pF	4
Output Capacitance		C_O	7	pF	4

†† The MT5C1601 device has an input capacitance maximum of 7pF.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($-40°C \leq T_A \leq 85°C$; $-40°C \leq T_A \leq 125°C$; $-55°C \leq T_A \leq 125°C$; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	^{t}RC	8		10		12		15		20		25		35		ns	
Address access time	^{t}AA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^{t}ACE		7		9		10		12		15		20		30	ns	
Output hold from address change	^{t}OH	2		2		2		3		3		3		3		ns	
Chip Enable to output in Low-Z	^{t}LZCE	1		2		2		3		3		3		3		ns	
Chip disable to output in High-Z	^{t}HZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		8		10		12		15		20		25		35	ns	
Output Enable access time	^{t}AOE		4		5		6		7		8		8		15	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		0		0		0		ns	
Output disable to output in High-Z	^{t}HZOE		4		5		5		6		7		8		8	ns	6
WRITE Cycle																	
WRITE cycle time	^{t}WC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^{t}CW	8		9		10		12		15		20		25		ns	
Address valid to end of write	^{t}AW	8		9		11		12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		0		0		ns	
WRITE pulse width	^{t}WP1	7		8		9		12		15		18		20		ns	
WRITE pulse width	^{t}WP2	8		9		10		14		15		20		25		ns	
Data setup time	^{t}DS	5		6		7		8		10		10		12		ns	
Data hold time	^{t}DH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	1		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^{t}HZWE		4		5		6		6		8		8		8	ns	6
Write Enable to output valid	^{t}AWE		10		12		14		17		20		25		35	ns	
Data valid to output valid	^{t}ADV		10		12		14		17		20		25		35	ns	

*These specifications are preliminary.

IT/AT/XT** SPECIFICATION - 64K SRAM FAMILY

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ....-1V to +7V
Storage Temperature (Plastic) ....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
**IT ....-40°C to +85°C
AT ....-40°C to +125°C
XT ....-55°C to +125°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-40°C \le T_A \le 85°C$; $-40°C \le T_A \le 125°C$; $-55°C \le T_A \le 125°C$; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		VIL	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ Vcc	ILI	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ VOUT ≤ Vcc	ILO	-5	5	µA	
Output High Voltage	IOH = -4.0mA	VOH	2.4		V	1
Output Low Voltage	IOL = 8.0mA	VOL		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MAX							UNITS	NOTES
			-8†	-10†	-12	-15	-20	-25	-35		
Power Supply Current: Operating	$\overline{CE}$ ≤ VIL; Vcc = MAX f = MAX = 1/ ᵗRC Outputs Open	Icc	170	155	145	130	120	110	100	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ VIH; Vcc = MAX f = MAX = 1/ ᵗRC Outputs Open	ISB1	65	60	55	45	40	35	35	mA	
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX VIL ≤ Vss +0.2V VIH ≥ Vcc -0.2V; f = 0	ISB2	5	5	5	5	5	5	5	mA	

† These are preliminary specifications.

DESCRIPTION	CONDITIONS		SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Data Retention	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ -0.2V	Vcc = 2V	ICCDR	150	300	µA	
		Vcc = 3V		300	550	µA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	CI	5††	pF	4
Output Capacitance		CO	7	pF	4

†† The MT5C6401 device has an input capacitance maximum of 7pF.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-40°C ≤ T_A ≤ 85°C; -40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	^{t}RC	8		10		12		15		20		25		35		ns	
Address access time	^{t}AA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^{t}ACE		7		9		10		12		15		20		30	ns	
Output hold from address change	^{t}OH	2		2		2		3		3		3		3		ns	
Chip Enable to output in Low-Z	^{t}LZCE	1		2		2		3		3		3		3		ns	
Chip disable to output in High-Z	^{t}HZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		8		10		12		15		20		25		35	ns	
Output Enable access time	^{t}AOE		4		5		6		7		8		8		15	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		0		0		0		ns	
Output disable to output in High-Z	^{t}HZOE		4		5		5		6		7		8		8	ns	6
WRITE Cycle																	
WRITE cycle time	^{t}WC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^{t}CW	8		9		10		12		15		20		25		ns	
Address valid to end of write	^{t}AW	8		9		11		12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		0		0		ns	
WRITE pulse width	^{t}WP1	7		8		9		12		15		18		20		ns	
WRITE pulse width	^{t}WP2	8		9		10		14		15		20		25		ns	
Data setup time	^{t}DS	5		6		7		8		10		10		12		ns	
Data hold time	^{t}DH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	1		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^{t}HZWE		4		5		6		6		8		8		8	ns	6
Write Enable to output valid	^{t}AWE		10		12		14		17		20		25		35	ns	
Data valid to output valid	^{t}ADV		10		12		14		17		20		25		35	ns	

*These specifications are preliminary.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ....-1V to +7V
Storage Temperature (Plastic) ....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
**IT ....-40°C to +85°C
AT ....-40°C to +125°C
XT ....-55°C to +125°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ 85°C; -40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-15**	**-20**	**-25**	**-30**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	160	130	120	100	100	100	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	35	30	30	30	30	30	mA	
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IL} ≤ Vss +0.2V V_{IH} ≥ Vcc -0.2V; f = 0	I_{SB2}	8	8	8	8	8	8	mA	

DESCRIPTION	CONDITIONS		SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Data Retention	$\overline{CE}$ ≥ (Vcc -0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ -0.2V	Vcc = 2V	I_{CCDR}	95	500	µA	
		Vcc = 3V		300	900	µA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz	C_I	6	pF	4
Output Capacitance	Vcc = 5V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-40°C ≤ T_A ≤ 85°C; -40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION		-15		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^{t}RC	15		20		25		30		35		45		ns	
Address access time	^{t}AA		15		20		25		30		35		45	ns	
Chip Enable access time	^{t}ACE		15		20		25		30		35		45	ns	
Output hold from address change	^{t}OH	3		3		5		5		5		5		ns	
Chip Enable to output in Low-Z	^{t}LZCE	3		6		6		6		6		6		ns	
Chip disable to output in High-Z	^{t}HZCE		8		9		9		12		15		18	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		15		20		25		30		35		45	ns	
Output Enable access time	^{t}AOE		8		10		10		12		15		15	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		0		0		ns	
Output disable to out put in High-Z	^{t}HZOE		7		7		7		10		12		15	ns	
WRITE Cycle															
WRITE cycle time	^{t}WC	15		20		20		25		30		35		ns	
Chip Enable to end of write	^{t}CW	12		15		18		20		20		25		ns	
Address valid to end of write	^{t}AW	12		15		18		20		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		0		ns	
WRITE pulse width	^{t}WP1	12		15		18		20		20		25		ns	
WRITE pulse width	^{t}WP2	12		15		18		20		20		25		ns	
Data setup time	^{t}DS	9		10		12		15		15		20		ns	
Data hold time	^{t}DH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	2		5		5		5		5		5		ns	
Write Enable to output in High-Z	^{t}HZWE		8		10		10		12		15		18	ns	6

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .... -1.0V to +7.0V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
**IT .... -40°C to +85°C
AT .... -40°C to +125°C
XT .... -55°C to +125°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-40°C \le T_A \le 85°C$; $-40°C \le T_A \le 125°C$; $-55°C \le T_A \le 125°C$; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^{t}RC Outputs Open	I_{CC}	95	150	135	125	120	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^{t}RC Outputs Open	I_{SB1}	17	45	40	35	32	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	7	7	7	7	mA	14
"L" version only	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.3	5	5	5	5	mA	

DESCRIPTION	CONDITIONS		SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Data Retention	$\overline{CE} \ge (V_{CC}$ -0.2V) $V_{IN} \ge (V_{CC}$ -0.2V) or ≤ -0.2V	V_{CC} = 2V	I_{CCDR}	35	1,000	µA	
		V_{CC} = 3V		70	1,500	µA	
		V_{CC} = 5V		250	4,000	µA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	8	pF	4
Output Capacitance		C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-40°C ≤ T_A ≤ 85°C; -40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^{t}RC	20		25		35		45		ns	
Address access time	^{t}AA		20		25		35		45	ns	
Chip Enable access time	^{t}ACE		20		25		35		45	ns	
Output hold from address change	^{t}OH	5		5		5		5		ns	
Chip Enable to output in Low-Z	^{t}LZCE	5		5		5		5		ns	
Chip disable to output in High-Z	^{t}HZCE		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^{t}PU	0		0		0		0		ns	
Chip disable to power-down time	^{t}PD		20		25		35		45	ns	
Output Enable access time	^{t}AOE		6		8		12		15	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		ns	
Output disable to output in High-Z	^{t}HZOE		6		10		12		15	ns	6
WRITE Cycle											
WRITE cycle time	^{t}WC	20		25		35		45		ns	
Chip Enable to end of write	^{t}CW	12		15		20		25		ns	
Address valid to end of write	^{t}AW	12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		ns	
WRITE pulse width	^{t}WP1	12		15		20		25		ns	
WRITE pulse width	^{t}WP2	15		15		20		25		ns	
Data setup time	^{t}DS	8		10		15		20		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	5		5		5		5		ns	
Write Enable to output in High-Z	^{t}HZWE	0	8	0	10	0	15	0	18	ns	6, 7

SYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package			Process	Page
				PLCC	PQFP	SOJ		
128K x 9	Synchronous SPARC™ Cache SRAM	MT58C1289	16, 20	-	-	32	CMOS	2-1
16K x 16	Registered Address, Write Control, Dual Chip Enable; Data Input Latch	MT58C1616	15, 17, 20, 25	52	52	-	CMOS	2-11
16K x 18	Registered Address, Write Control, Dual Chip Enable; Data Input Latch	MT58C1618	15, 17, 20, 25	52	52	-	CMOS	2-21

NOTE: Many Micron components are available in bare die form. Contact Micron Technology, Inc., for more information.

SYNCHRONOUS SRAM

128K x 9 SRAM

FULLY REGISTERED INPUTS AND OUTPUTS

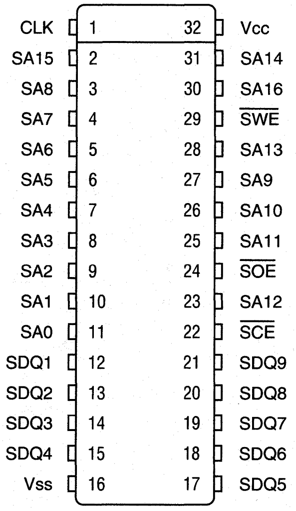
FEATURES

- Timing specific to SPARC™ microprocessor
- Fast access times: 16.6 and 20ns
- Fast clock to data valid: 10ns
- Single +5V ±10% power supply
- READ data and WRITE data registers
- Common, TTL compatible data inputs and outputs
- All inputs and outputs registered with clock
- Fully synchronous, pipelined architecture

OPTIONS	MARKING
• Timing	
16.6ns access	-16
20ns access	-20
• Packages	
32-pin SOJ	DJ
• Density	
128K x 9	MT58C1289

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(E-11)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

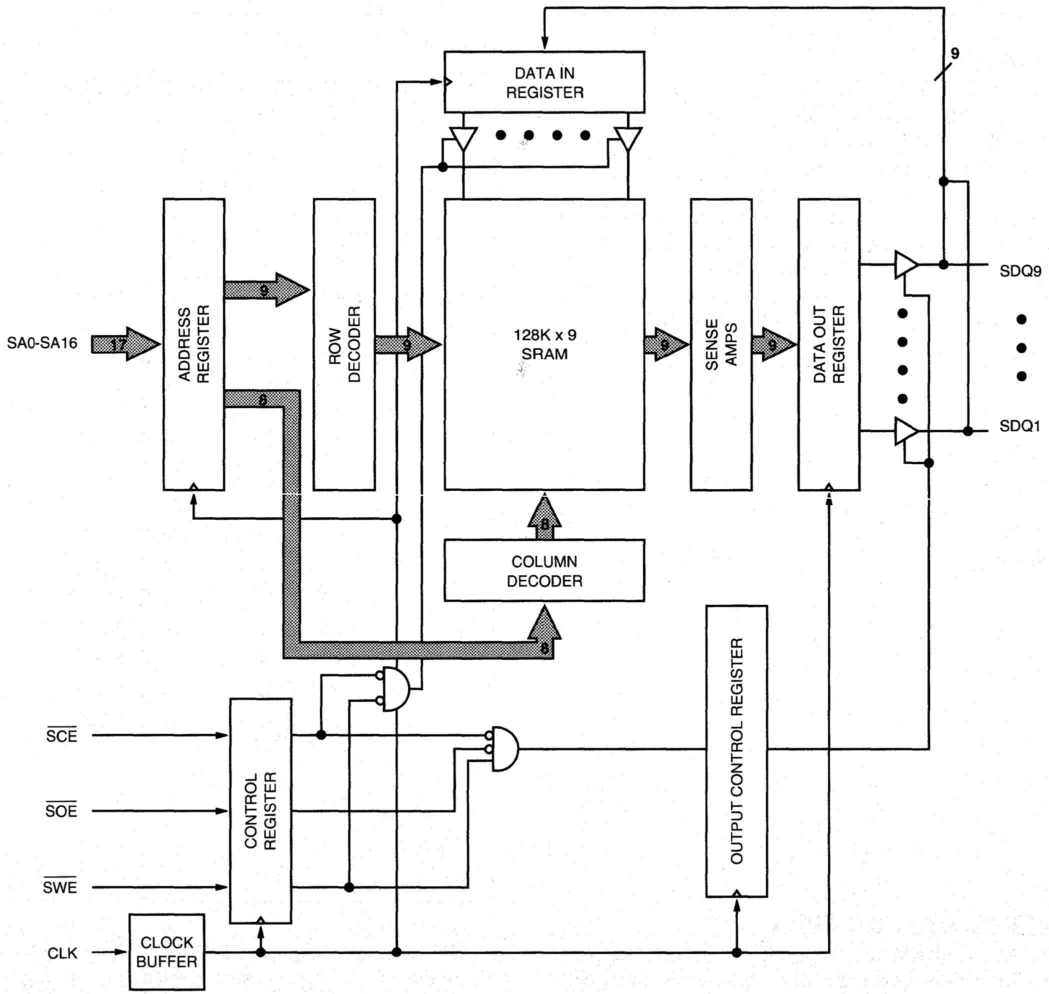
The MT58C1289 is a fully "pipelined" SRAM that integrates registers for address, data in, data out and synchronous chip enable ($\overline{\text{SCE}}$), output enable ($\overline{\text{SOE}}$) and write enable ($\overline{\text{SWE}}$). All registers are triggered with the positive edge of the clock signal (CLK).

READ cycles are performed when $\overline{\text{SWE}}$ is HIGH and $\overline{\text{SOE}}$ and $\overline{\text{SCE}}$ are LOW at the positive edge of CLK. Read data is then presented at the next positive edge of CLK.

WRITE cycles occur when $\overline{\text{SWE}}$ and $\overline{\text{SCE}}$ are LOW at the rising edge CLK. Data present at the data input registers is written to the SRAM address present at the address input registers on that same rising edge of CLK. The WRITE cycle is internally self-timed which eliminates the need for complex write pulse generation external to the SRAM. The WRITE cycle requires three preceding deselect cycles when a WRITE cycle follows a READ cycle. This allows the D/Q lines to be in the High-Z state when write data is applied. The SRAM is deselected if $\overline{\text{SCE}}$ is HIGH when a positive edge of CLK occurs.

The MT58C1289 operates from a +5V power supply.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC AND PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
11, 10, 9, 8, 7, 6, 5, 4, 3, 27, 26, 25, 23, 28, 31, 2, 30	SA0-SA16	Input	Address Inputs: These inputs are synchronous and must meet the setup and hold times around the positive edge of CLK. The address inputs are clocked into the address register on each positive edge of CLK.
29	$\overline{SWE}$	Input	Synchronous Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{SWE}$ is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{SWE}$ is registered on every positive edge of CLK and must meet the setup and hold times referenced to that edge. WRITE cycles are self-timed internally by the SRAM.
1	CLK	Input	CLOCK: All timing is controlled by the positive edge of CLK. All synchronous input and output signals are registered on the positive edge of CLK and must meet the setup and hold times referenced to that edge.
22	$\overline{SCE}$	Input	Synchronous Chip Enable: This signal is used to enable the device. This is a synchronous input and must meet the setup and hold times around CLK. When $\overline{SCE}$ is HIGH, the SRAM automatically goes into the standby power mode.
24	$\overline{SOE}$	Input	Synchronous Output Enable: This active LOW input enables the output drivers. This is a synchronous input and must meet the setup and hold times around CLK.
12, 13, 14, 15, 17, 18, 19, 20, 21	SDQ1-SDQ9	Input/ Output	SRAM Data I/O: For a READ, control signals and address are presented at the rising edge of CLK and data is valid ^{t}KQ after the next rising edge of CLK. Data presented for a WRITE cycle must meet the setup and hold times around CLK.
32	Vcc	Supply	Power Supply: +5V ±10%
16	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	$\overline{SCE}$	$\overline{SWE}$	CLK	$\overline{SOE}$	D	Q NEXT CLOCK	POWER
Deselected	H	X	↑	X	X	High-Z	Standby
READ	L	H	↑	H	X	High-Z	Active
READ	L	H	↑	L	X	Q1-Q9	Active
WRITE	L	L	↑	X	D1-D9	High-Z	Active

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +7V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1

			MAX			
DESCRIPTION	CONDITIONS	SYMBOL	-16	-20	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{CC}	150	130	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{SB1}	70	60	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2V; V_{CC} = MAX; $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	3	3	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYM	-16 MIN	-16 MAX	-20 MIN	-20 MAX	UNITS	NOTES
CLOCK							
Clock cycle time	^{t}KC	16.6		20		ns	
Clock HIGH time	^{t}KH	5		5		ns	
Clock LOW time	^{t}KL	5		5		ns	
READ Cycle							
READ cycle time	^{t}RC	16.6		20		ns	9
Address setup time	^{t}SAS	3		3		ns	9
Address hold time	^{t}SAH	0.5		1		ns	9
Chip Enable setup time	^{t}SCES	3		3		ns	9
Chip Enable hold time	^{t}SCEH	0.5		1		ns	9
Output Enable setup time	^{t}SOES	3		3		ns	9
Output Enable hold time	^{t}SOEH	0.5		1		ns	9
Write Enable setup time	^{t}SWES	3		3		ns	9
Write Enable hold time	^{t}SWEH	0.5		1		ns	9
Output hold time from clock	^{t}KOH	2		3		ns	
Clock to data valid	^{t}KQ		10		10	ns	
Clock to output High-Z	^{t}KQHZ		8		10	ns	4, 6, 7
Clock to output Low-Z	^{t}KQLZ	0		0		ns	4, 6, 7
WRITE Cycle							
WRITE cycle time	^{t}WC	16.6		20		ns	
Address setup time	^{t}SAS	3		3		ns	9
Address hold time	^{t}SAH	0.5		1		ns	9
Chip Enable setup time	^{t}SCES	3		3		ns	9
Chip Enable hold time	^{t}SCEH	0.5		1		ns	9
Write Enable setup time	^{t}SWES	3		3		ns	9
Write Enable hold time	^{t}SWEH	0.5		1		ns	9
Data setup time	^{t}SDS	3		3		ns	
Data hold time	^{t}SDH	0.5		1		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

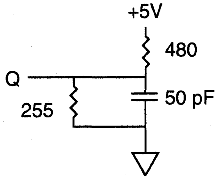


Fig. 1 OUTPUT LOAD EQUIVALENT

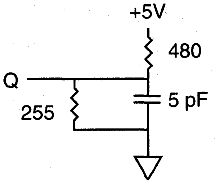
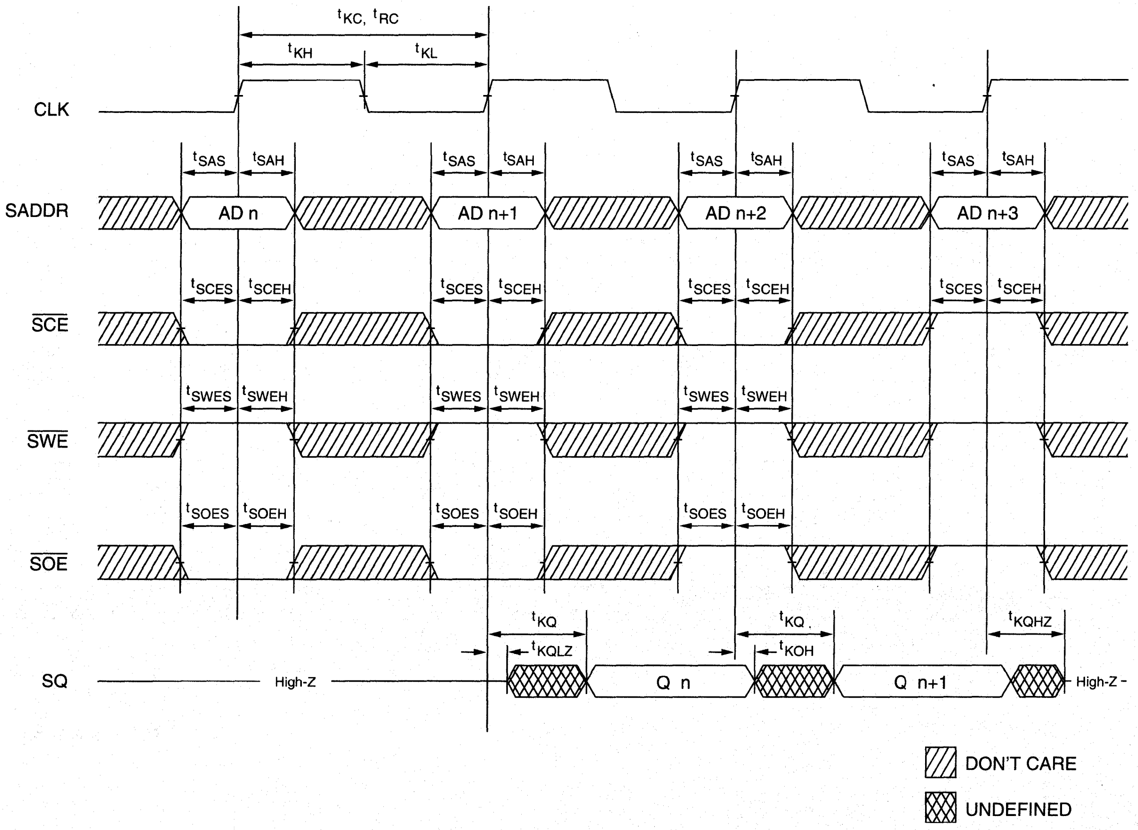


Fig. 2 OUTPUT LOAD EQUIVALENT

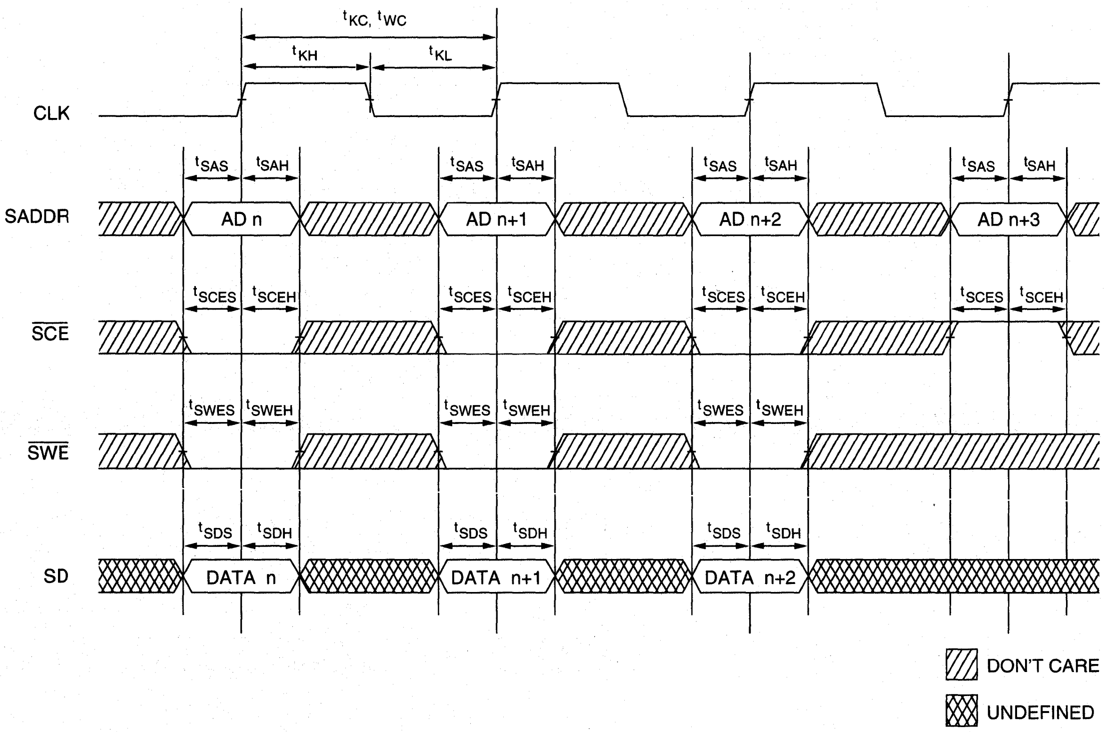
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}KQHZ is less than ^{t}KQLZ.
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. This is a synchronous device. All synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK.

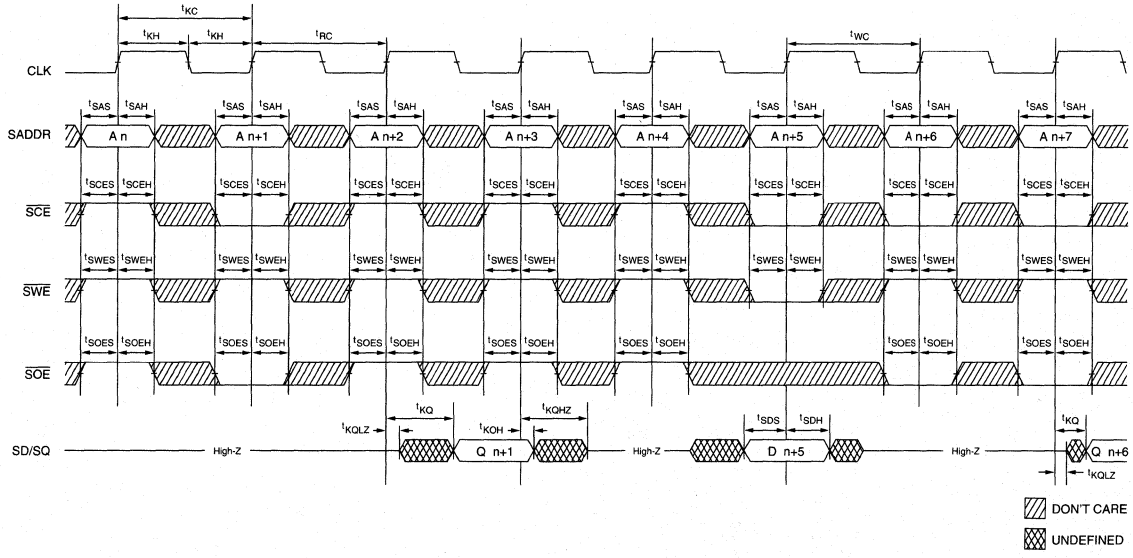
READ CYCLE[7, 8, 9]



WRITE CYCLE[7, 9]



READ/WRITE CYCLE [7, 8, 9]



SYNCHRONOUS SRAM

16K x 16 SRAM

WITH CLOCKED, REGISTERED INPUTS

FEATURES

- Fast access times: 15, 17, 20 and 25ns
- Fast Output Enable: 6, 7, 8 and 10ns
- Single +5V ±10% power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Optional +3.3V ±10% output buffer operation
- Data input latch
- Common data inputs and data outputs
- BYTE WRITE capability via dual write strobes
- Clock-controlled, registered address, write control and dual Chip Enables

OPTIONS	MARKING
• Timing	
15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG
• Density	
16K x 16	MT58C1616

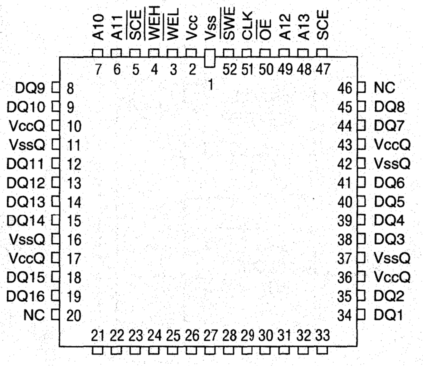
GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58C1616 SRAM integrates a 16K x 16 SRAM core with advanced synchronous peripheral circuitry. All synchronous inputs pass through registers controlled by a positive-edge-triggered, single-clock input (CLK). The synchronous inputs include all addresses, the two chip selects ($\overline{\text{SCE}}$, SCE) and the synchronous write enable ($\overline{\text{SWE}}$). Asynchronous inputs include the byte write enables ($\overline{\text{WEL}}$, $\overline{\text{WEH}}$), output enable ($\overline{\text{OE}}$), data latch enable (DLE) and the clock. Input data can be asynchronously latched by DLE to provide simplified data-in (D) timing during WRITE cycles. Data-out (Q), enabled by $\overline{\text{OE}}$ during READ cycles, is asynchronous. The entire data word (DQ1 - DQ16) is output during each READ cycle. The devices are ideally suited for "pipelined" systems and those systems which benefit from a wide data bus.

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-5)

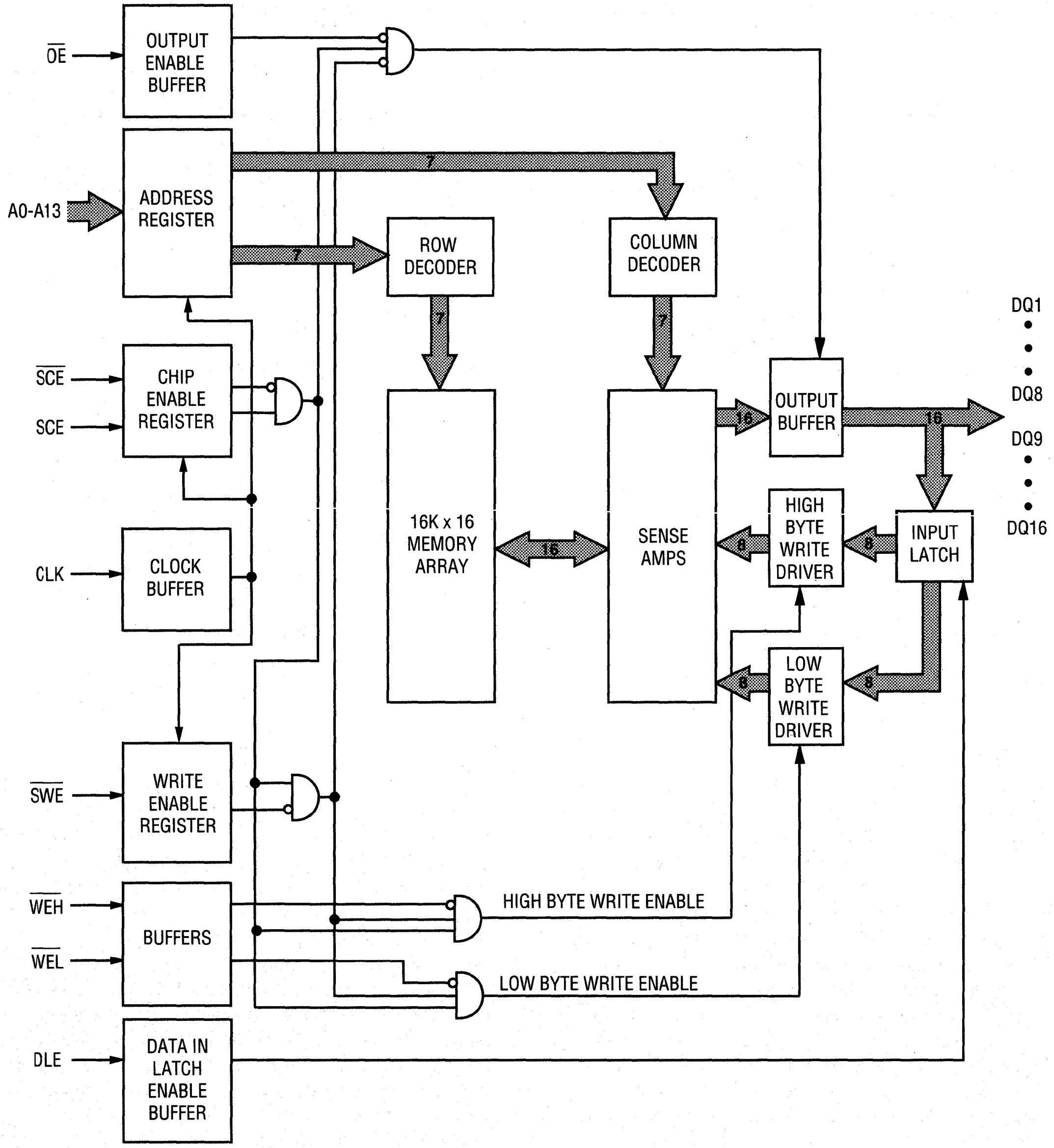


Address and write control are registered on-chip to simplify WRITE cycles. Dual write enables allow individual bytes to be written. $\overline{\text{WEL}}$ controls DQ1-DQ8 while $\overline{\text{WEH}}$ controls DQ9-DQ16. $\overline{\text{WEL}}$/$\overline{\text{WEH}}$ allow LATE WRITE cycles to be aborted if they are both HIGH during the LOW period of the clock. Dual chip enables (SCE, $\overline{\text{SCE}}$) allow on-chip address decoding to be accomplished when the devices are used in a dual-bank mode.

A data input latch is provided. When DLE is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present at the inputs is held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT58C1616 operates from a +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided to allow either +3.3V or +5V TTL operation of the output drivers.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC AND PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
52	$\overline{\text{SWE}}$	Input	Synchronous Write Enable: This input is a synchronous write enable and must meet the setup and hold times around the rising edge of CLK. $\overline{\text{SWE}}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
51	CLK	Input	Clock: This signal registers the address, SCE, $\overline{\text{SCE}}$, and $\overline{\text{SWE}}$ inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.
3, 4	$\overline{\text{WEL}}$, $\overline{\text{WEH}}$	Input	Asynchronous Write Enables: These asynchronous, active LOW inputs allow individual bytes to be written. When $\overline{\text{WEL}}$ is LOW, data is written to the lower byte, D1-D8. When $\overline{\text{WEH}}$ is LOW, data is written to the upper byte, D9-D16. A late WRITE cycle can be aborted if both $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ are HIGH during the LOW period of CLK.
5, 47	$\overline{\text{SCE}}$,SCE	Input	Synchronous Chip Selects: These synchronous signals are used to enable the device. Both active HIGH (SCE) and active LOW ($\overline{\text{SCE}}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual-bank configuration.
50	$\overline{\text{OE}}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH the latch is transparent. Input data is latched asynchronously into the on-chip data latch on the falling edge of DLE. DLE must meet the setup and hold times around CLK if data is latched.
20, 46	NC NC	Input/ Output	These pins are no connects (NC). No connects are not internally bonded.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. Input data must meet the setup and hold time around DLE when being latched.
2, 28	Vcc	Supply	Power Supply: +5V ±10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ±10% or 3.3V ±10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	SCE	$\overline{SCE}$	$\overline{SWE}$	$\overline{WEL}$	$\overline{WEH}$	DLE	$\overline{OE}$	DQ
Deselected Cycle	L	X	X	X	X	X	X	High-Z
Deselected Cycle	X	H	X	X	X	X	X	High-Z
Read Cycle	H	L	H	X	X	X	H	High-Z
Read Cycle	H	L	H	X	X	X	L	Q1-Q16
Word Write Cycle DQ1-DQ16 Transparent Data-In	H	L	L	L	L	H	X	D1-D16
Word Write Cycle DQ1-DQ16 Latched Data-In	H	L	L	L	L	L	X	D1-D16
Aborted Write Cycle	H	L	L	H	H	X	X	High-Z
Byte Write Cycle DQ1-DQ8 Transparent Data-In	H	L	L	L	H	H	X	D1-D8
Byte Write Cycle DQ9-DQ16 Transparent Data-In	H	L	L	H	L	H	X	D9-D16
Byte Write Cycle DQ1-DQ8 Latched Data-In	H	L	L	L	H	L	X	D1-D8
Byte Write Cycle DQ9-DQ16 Latched Data-In	H	L	L	H	L	L	X	D9-D16

NOTE:
1. Registered inputs (addresses, $\overline{SWE}$, SCE and $\overline{SCE}$) must satisfy the specified setup and hold times around the rising edge of clock (CLK). Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the WRITE cycle.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold times.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative
to V_{SS}/V_{SSQ} .... -1.0V to +7.0V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1.5W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%; $V_{SS} = V_{SSQ}$, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1
Output Buffer Supply Voltage	5V TTL Compatible	V_{CCQ}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{SCE} \le V_{IL}$; $SCE \ge V_{IH}$; f = MAX V_{CC} = MAX; Outputs Open	I_{CC}	150	250	mA	3
Power Supply Current: Standby	f = MAX; $SCE \le V_{IL}$; $\overline{SCE} \ge V_{IH}$ V_{CC} = MAX	I_{SB1}	50	80	mA	
	$\overline{SCE} \ge V_{CC}$ -0.2; $SCE \le V_{SS}$ +0.2 V_{CC} = MAX; $V_{IL} \le V_{SS}$ +0.2 $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}	5	15	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$	9	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = VccQ = 5V ±10%)

		-15		-17		-20		-25			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	^{t}KC	15		17		20		25		ns	
Clock HIGH time	^{t}KH	4		4		4		4		ns	
Clock LOW time	^{t}KL	8		8		8		8		ns	
Chip Enable											
SCE/$\overline{\text{SCE}}$ setup time	^{t}SCES	3		3		3		3		ns	10
SCE/$\overline{\text{SCE}}$ hold time	^{t}SCEH	2		2		2		2		ns	10
Address											
Address setup time	^{t}SAS	3		3		3		3		ns	10
Address hold time	^{t}SAH	2		2		2		2		ns	10
READ Cycle											
READ cycle time	^{t}RC	15		17		20		25		ns	11
Clock to output valid	^{t}KQ		15		17		20		25	ns	
Clock to output invalid	^{t}KQX	6		6		6		6		ns	10
Clock to output in Low-Z	^{t}KQLZ	10		10		10		10		ns	6, 7, 4
Clock to output in High-Z	^{t}KQHZ	3	8	3	8	3	8	3	12	ns	6, 7, 4
$\overline{\text{SWE}}$ setup time	^{t}SWNS	3		3		3		3		ns	10
$\overline{\text{SWE}}$ hold time	^{t}SWNH	2		2		2		2		ns	10
$\overline{\text{OE}}$ to output valid	^{t}OEQ		6		7		8		10	ns	
$\overline{\text{OE}}$ to output in Low-Z	^{t}OELZ	0		0		0		0		ns	6, 7, 4
$\overline{\text{OE}}$ to output in High-Z	^{t}OEHZ		8		8		8		8	ns	6, 7, 4
WRITE Cycle											
WRITE cycle time	^{t}WC	15		17		20		25		ns	11
$\overline{\text{SWE}}$ setup time	^{t}SWES	3		3		3		3		ns	10
$\overline{\text{SWE}}$ hold time	^{t}SWEH	2		2		2		2		ns	10
Data setup time	^{t}DS	5		6		6		7		ns	8, 10
Data hold time	^{t}DH	2		2		2		2		ns	8, 10
Data to DLE not setup time	^{t}DLNS	1		1		1		1		ns	9, 10
Data to DLE not hold time	^{t}DLNH	3		3		3		3		ns	9, 10
DLE setup time	^{t}DLS	6		6		6		7		ns	9, 10
DLE hold time	^{t}DLH	2		2		2		2		ns	9, 10
$\overline{\text{WEL}}$ / $\overline{\text{WEH}}$ setup time	^{t}WES	6		6		6		7		ns	10
$\overline{\text{WEL}}$ / $\overline{\text{WEH}}$ hold time	^{t}WEH	2		2		2		2		ns	10
$\overline{\text{WEL}}$ / $\overline{\text{WEH}}$ not setup time (aborted WRITE)	^{t}WNS		0		0		0		0	ns	10
$\overline{\text{WEL}}$ / $\overline{\text{WEH}}$ not hold time (aborted WRITE)	^{t}WNH	2		2		2		2		ns	10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

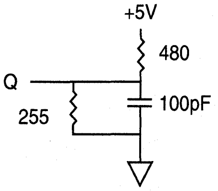


Fig. 1 OUTPUT LOAD EQUIVALENT

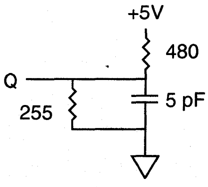
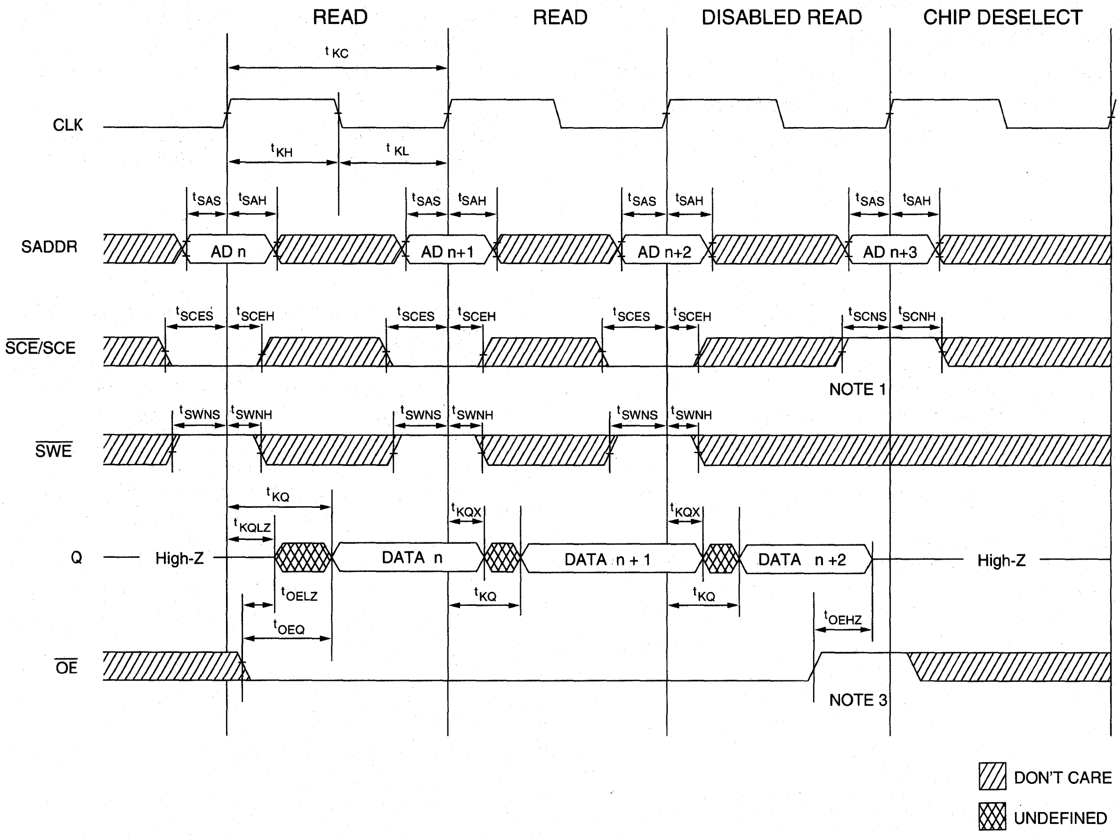


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

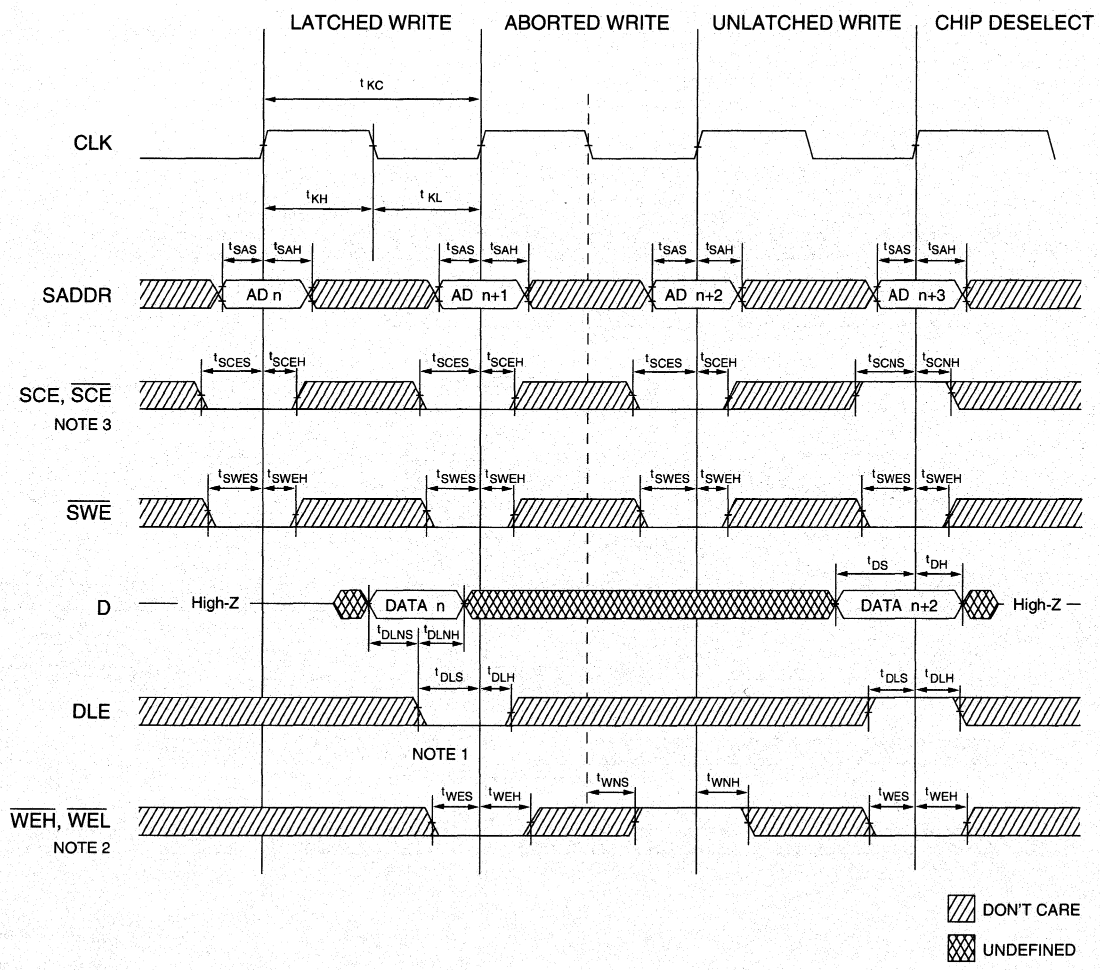
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}KQHZ is less than ^{t}KQLZ and ^{t}OEHZ is less than ^{t}OELZ.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold time with respect to the rising edge of clock (CLK).
10. This is a synchronous device. All synchronous inputs must meet the setup and hold times with stable logic levels for all falling edges of address latch enable (ALE) and data latch enable (DLE).
11. ^{t}RC = ^{t}WC = ^{t}KC

READ TIMING[2]



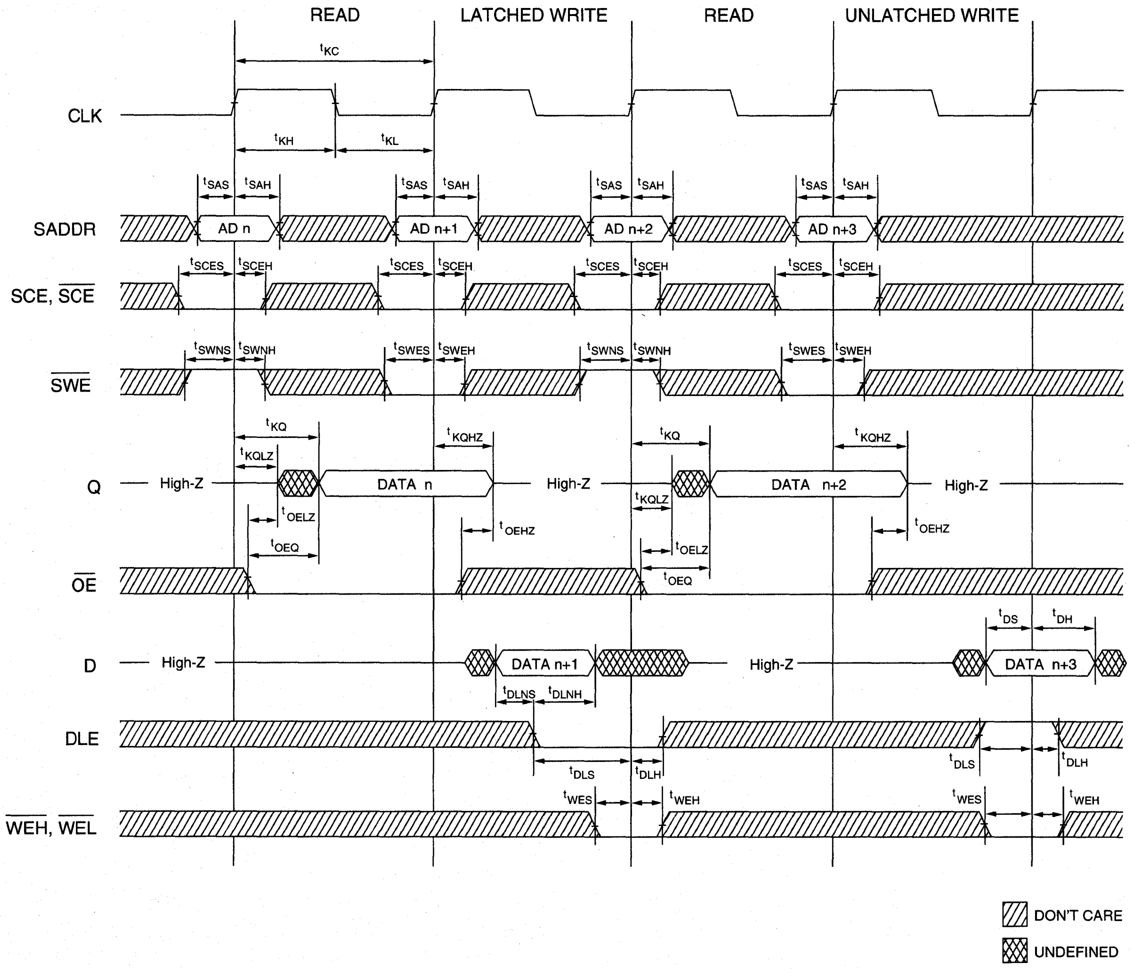
NOTE:
1. When synchronous chip enables (SCE, $\overline{\text{SCE}}$) are inactive, the part is deselected.
2. $\overline{\text{WEL}}$ / $\overline{\text{WEH}}$ are "don't care" signals during a READ cycle.
3. Data out (Q) is disabled whenever asynchronous output enable ($\overline{\text{OE}}$) is inactive, during a READ cycle.

WRITE TIMING



NOTE:
1. Data is latched when DLE transitions from HIGH to LOW. When DLE is HIGH, the latch is transparent and data flows through the latch.
2. Asynchronous write enables ($\overline{\text{WEH}}$, $\overline{\text{WEL}}$) are available for use as byte write enables at the system level. They are also available to perform a LATE WRITE cycle abort.
3. When synchronous chip enables (SCE, $\overline{\text{SCE}}$) are inactive, the part is deselected.

READ/WRITE TIMING



SYNCHRONOUS SRAM

16K x 18 SRAM

WITH CLOCKED, REGISTERED INPUTS

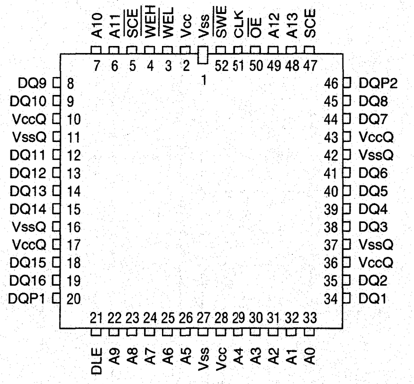
FEATURES

- Fast access times: 15, 17, 20 and 25ns
- Fast Output Enable: 6, 7, 8 and 10ns
- Single +5V ±10% power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Optional +3.3V ±10% output buffer operation
- Data input latch
- Common data inputs and data outputs
- BYTE WRITE capability via dual write strobes
- Parity bits
- Clock controlled registered address, write control and dual Chip Enables

OPTIONS	MARKING
• Timing	
15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG
• Density	
16K x 18	MT58C1618

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-5)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

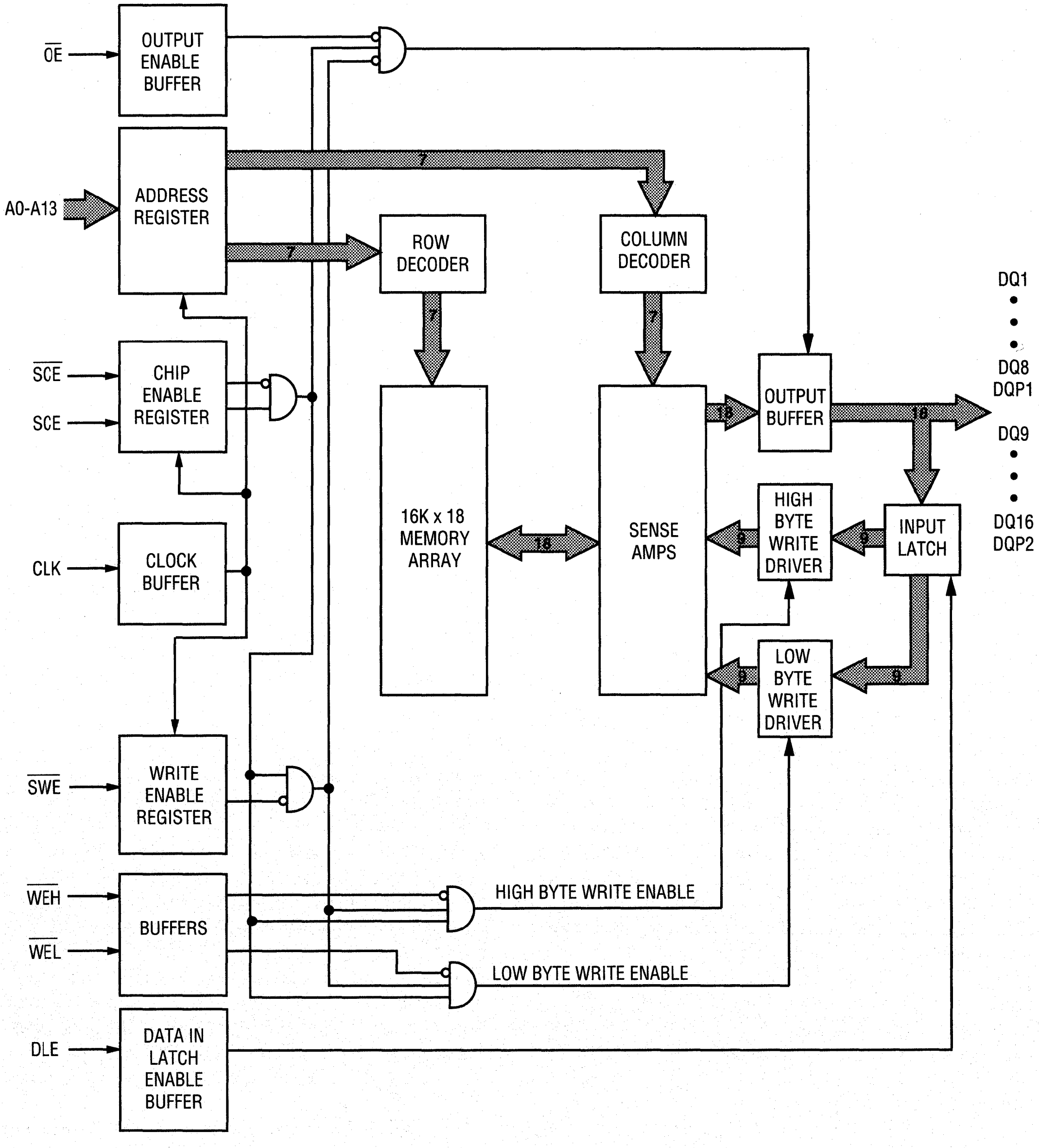
The MT58C1618 SRAM integrates a 16K x 18 SRAM core with advanced synchronous peripheral circuitry. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, the two chip selects ($\overline{\text{SCE}}$, SCE) and the synchronous write enable ($\overline{\text{SWE}}$). Asynchronous inputs include the byte write enables ($\overline{\text{WEL}}$, $\overline{\text{WEH}}$), output enable ($\overline{\text{OE}}$), data latch enable (DLE) and the clock. Input data can be asynchronously latched by DLE to provide simplified data-in (D) timing during WRITE cycles. Data-out (Q), enabled by $\overline{\text{OE}}$ during READ cycles, is asynchronous. The entire data word (DQ1-DQ16, DQP1/2) is output during each READ cycle. The devices are ideally suited for "pipelined" systems and those systems which benefit from a wide data bus.

Address and write control are registered on-chip to simplify WRITE cycles. Dual write enables allow individual bytes to be written. $\overline{\text{WEL}}$ controls DQ1-DQ8 and DQP1 while $\overline{\text{WEH}}$ controls DQ9-DQ16 and DQP2. $\overline{\text{WEL}}$/$\overline{\text{WEH}}$ allow LATE WRITE cycles to be aborted if they are both HIGH during the LOW period of the clock. Dual chip enables (SCE, $\overline{\text{SCE}}$) allow on-chip address decoding to be accomplished when the devices are used in a dual-bank mode.

A data input latch is provided. When DLE is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present at the input is held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT58C1618 operates from a +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided to allow either +3.3V or +5V TTL operation of the output drivers.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC AND PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
52	$\overline{\text{SWE}}$	Input	Synchronous Write Enable: This input is a synchronous write enable and must meet the setup and hold times around the rising edge of CLK. $\overline{\text{SWE}}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
51	CLK	Input	Clock: This signal latches the address, SCE, $\overline{\text{SCE}}$, and $\overline{\text{SWE}}$ inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
3, 4	$\overline{\text{WEL}}$, $\overline{\text{WEH}}$	Input	Asynchronous Write Enables: These asynchronous, active LOW inputs allow individual bytes to be written. When $\overline{\text{WEL}}$ is LOW, data is written to the lower byte, D1-D8, DQP1. When $\overline{\text{WEH}}$ is LOW, data is written to the upper byte, D9-D16, DQP2. A late WRITE cycle can be aborted if both $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ are HIGH during the LOW period of CLK.
5, 47	$\overline{\text{SCE}}$,SCE	Input	Synchronous Chip Selects: These synchronous signals are used to enable the device. Both active HIGH (SCE) and active LOW ($\overline{\text{SCE}}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual-bank configuration.
50	$\overline{\text{OE}}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH the latch is transparent. Input data is latched asynchronously into the on-chip data latch on the falling edge of DLE. DLE must meet the setup and hold times around DLE if data is latched.
20, 46	DQP1 DQP2	Input/ Output	Parity Data I/O: These signals are data parity bits. The DQP1 is the parity bit for the lower byte, DQ1-DQ8. DQP2 is the parity bit for the upper byte, DQ9-DQ16. Parity data must meet the setup and hold time around DLE when being latched.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. Input data must meet the setup and hold time around DLE when being latched.
2, 28	Vcc	Supply	Power Supply: +5V ±10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ±10% or 3.3V ±10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	SCE	$\overline{\text{SCE}}$	$\overline{\text{SWE}}$	$\overline{\text{WEL}}$	$\overline{\text{WEH}}$	DLE	$\overline{\text{OE}}$	DQ
Deselected Cycle	L	X	X	X	X	X	X	High-Z
Deselected Cycle	X	H	X	X	X	X	X	High-Z
Read Cycle	H	L	H	X	X	X	H	High-Z
Read Cycle	H	L	H	X	X	X	L	Q1-Q16, QP1, QP2
Word Write Cycle DQ1-DQ16, DQP1, DQP2, Transparent Data-In	H	L	L	L	L	H	X	D1-D16, DP1, DP2
Word Write Cycle DQ1-DQ16, DQP1, DQP2, Latched Data-In	H	L	L	L	L	L	X	D1-D16, DP1, DP2
Aborted Write Cycle	H	L	L	H	H	X	X	High-Z
Byte Write Cycle DQ1-DQ8, DQP1 Transparent Data-In	H	L	L	L	H	H	X	D1-D8, DP1
Byte Write Cycle DQ9-DQ16, DQP2 Transparent Data-In	H	L	L	H	L	H	X	D9-D16, DP2
Byte Write Cycle DQ1-DQ8, DQP1 Latched Data-In	H	L	L	L	H	L	X	D1-D8, DP1
Byte Write Cycle DQ9-DQ16, DQP2 Latched Data-In	H	L	L	H	L	L	X	D9-D16, DP2

NOTE:

1. Registered inputs (addresses, $\overline{\text{SWE}}$, SCE, and $\overline{\text{SCE}}$) must satisfy the specified setup and hold times around the rising edge of clock (CLK). Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the WRITE cycle.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold times.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative
to V_{SS}/V_{SSQ} .... -1.0V to +7.0V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1.5W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = V_{SSQ}$, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	$I_{OH} = -4.0mA$	V_{OH}	2.4		V	1
Output Low Voltage	$I_{OL} = 8.0mA$	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1
Output Buffer Supply Voltage	5V TTL Compatible	V_{CCQ}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{SCE} \le V_{IL}$; $SCE \ge V_{IH}$; f = MAX V_{CC} = MAX; Outputs Open	I_{CC}	150	250	mA	3
Power Supply Current: Standby	$SCE \le V_{IL}$; $\overline{SCE} \ge V_{IH}$ V_{CC} = MAX; f = MAX	I_{SB1}	50	80	mA	
	$\overline{SCE} \ge V_{CC} - 0.2$; $SCE \le V_{SS} + 0.2$ V_{CC} = MAX; $V_{IL} \le V_{SS} + 0.2$ $V_{IH} \ge V_{CC} - 0.2$; f = 0	I_{SB2}	5	15	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25°C$, f = 1 MHz $V_{CC} = 5V$	C_I	5	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$	9	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = VccQ = 5V ±10%)

		-15		-17		-20		-25			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	^{t}KC	15		17		20		25		ns	
Clock HIGH time	^{t}KH	4		4		4		4		ns	
Clock LOW time	^{t}KL	8		8		8		8		ns	
Chip Enable											
SCE/$\overline{\text{SCE}}$ setup time	^{t}SCES	3		3		3		3		ns	10
SCE/$\overline{\text{SCE}}$ hold time	^{t}SCEH	2		2		2		2		ns	10
Address											
Address setup time	^{t}SAS	3		3		3		3		ns	10
Address hold time	^{t}SAH	2		2		2		2		ns	10
READ Cycle											
READ cycle time	^{t}RC	15		17		20		25		ns	11
Clock to output valid	^{t}KQ		15		17		20		25	ns	
Clock to output invalid	^{t}KQX	6		6		6		6		ns	10
Clock to output in Low-Z	^{t}KQLZ	10		10		10		10		ns	6, 7, 4
Clock to output in High-Z	^{t}KQHZ	3	8	3	8	3	8	3	12	ns	6, 7, 4
$\overline{\text{SWE}}$ setup time	^{t}SWNS	3		3		3		3		ns	10
$\overline{\text{SWE}}$ hold time	^{t}SWNH	2		2		2		2		ns	10
$\overline{\text{OE}}$ to output valid	^{t}OEQ		6		7		8		10	ns	
$\overline{\text{OE}}$ to output in Low-Z	^{t}OELZ	0		0		0		0		ns	6, 7,4
$\overline{\text{OE}}$ to output in High-Z	^{t}OEHZ		8		8		8		8	ns	6, 7, 4
WRITE Cycle											
WRITE cycle time	^{t}WC	15		17		20		25		ns	11
$\overline{\text{SWE}}$ setup time	^{t}SWES	3		3		3		3		ns	10
$\overline{\text{SWE}}$ hold time	^{t}SWEH	2		2		2		2		ns	10
Data setup time	^{t}DS	5		6		6		7		ns	8, 10
Data hold time	^{t}DH	2		2		2		2		ns	8, 10
Data to DLE not setup time	^{t}DLNS	1		1		1		1		ns	9, 10
Data to DLE not hold time	^{t}DLNH	3		3		3		3		ns	9, 10
DLE setup time	^{t}DLS	6		6		6		7		ns	9, 10
DLE hold time	^{t}DLH	2		2		2		2		ns	9, 10
$\overline{\text{WEL}}$ / $\overline{\text{WEH}}$ setup time	^{t}WES	6		6		6		7		ns	10
$\overline{\text{WEL}}$ / $\overline{\text{WEH}}$ hold time	^{t}WEH	2		2		2		2		ns	10
$\overline{\text{WEL}}$ / $\overline{\text{WEH}}$ not setup time (aborted WRITE)	^{t}WNS		0		0		0		0	ns	10
$\overline{\text{WEL}}$ / $\overline{\text{WEH}}$ not hold time (aborted WRITE)	^{t}WNH	2		2		2		2		ns	10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

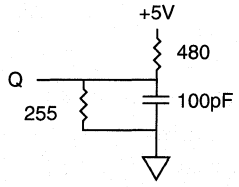


Fig. 1 OUTPUT LOAD EQUIVALENT

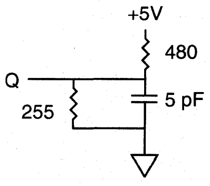
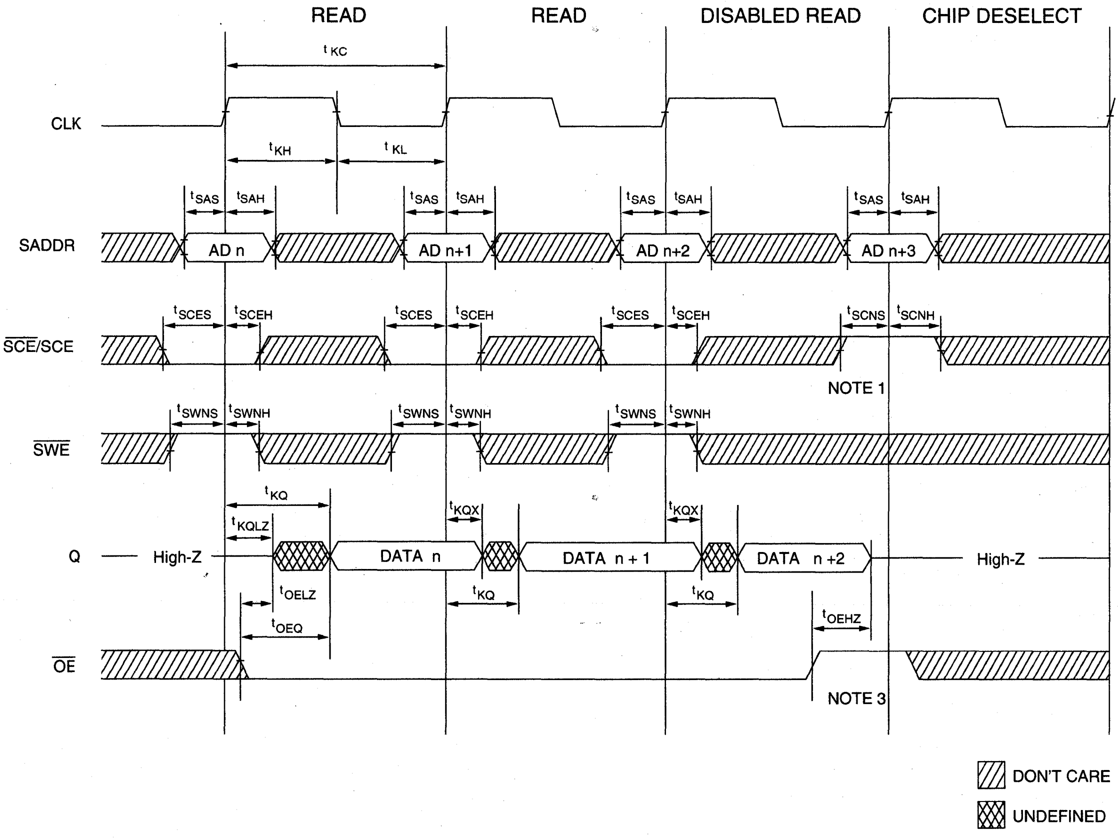


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

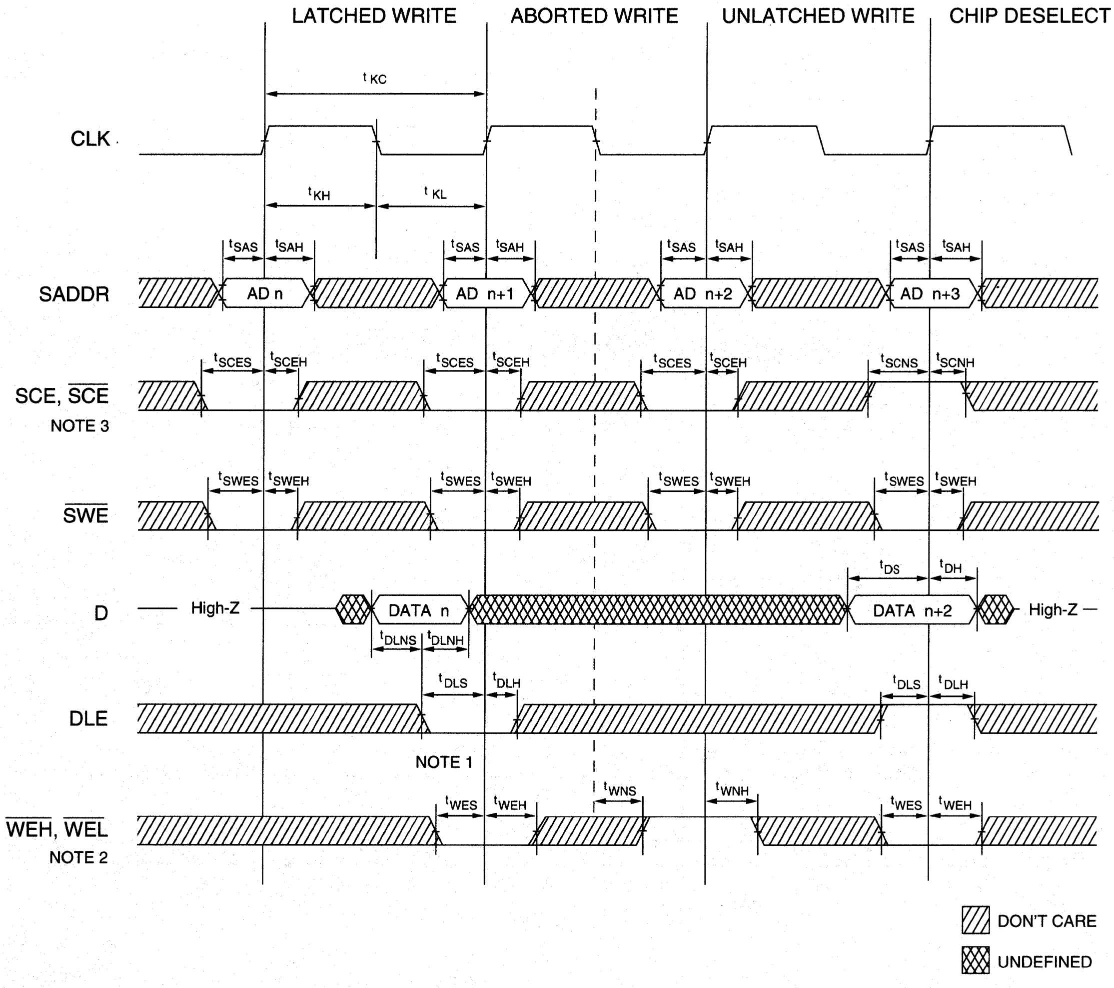
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}KQHZ is less than ^{t}KQLZ and ^{t}OEHZ is less than ^{t}OELZ.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold time with respect to the rising edge of clock (CLK).
10. This is a synchronous device. All synchronous inputs must meet the setup and hold times with stable logic levels for all falling edges of address latch enable (ALE) and data latch enable (DLE).
11. ^{t}RC = ^{t}WC = ^{t}KC

READ TIMING[2]



NOTE:
1. When synchronous chip enables (SCE, $\overline{\text{SCE}}$) are inactive, the part is deselected.
2. $\overline{\text{WEL}}$ / $\overline{\text{WEH}}$ are “don't care” signals during a READ cycle.
3. Data out (Q) is disabled whenever asynchronous output enable ($\overline{\text{OE}}$) is inactive, during a READ cycle.

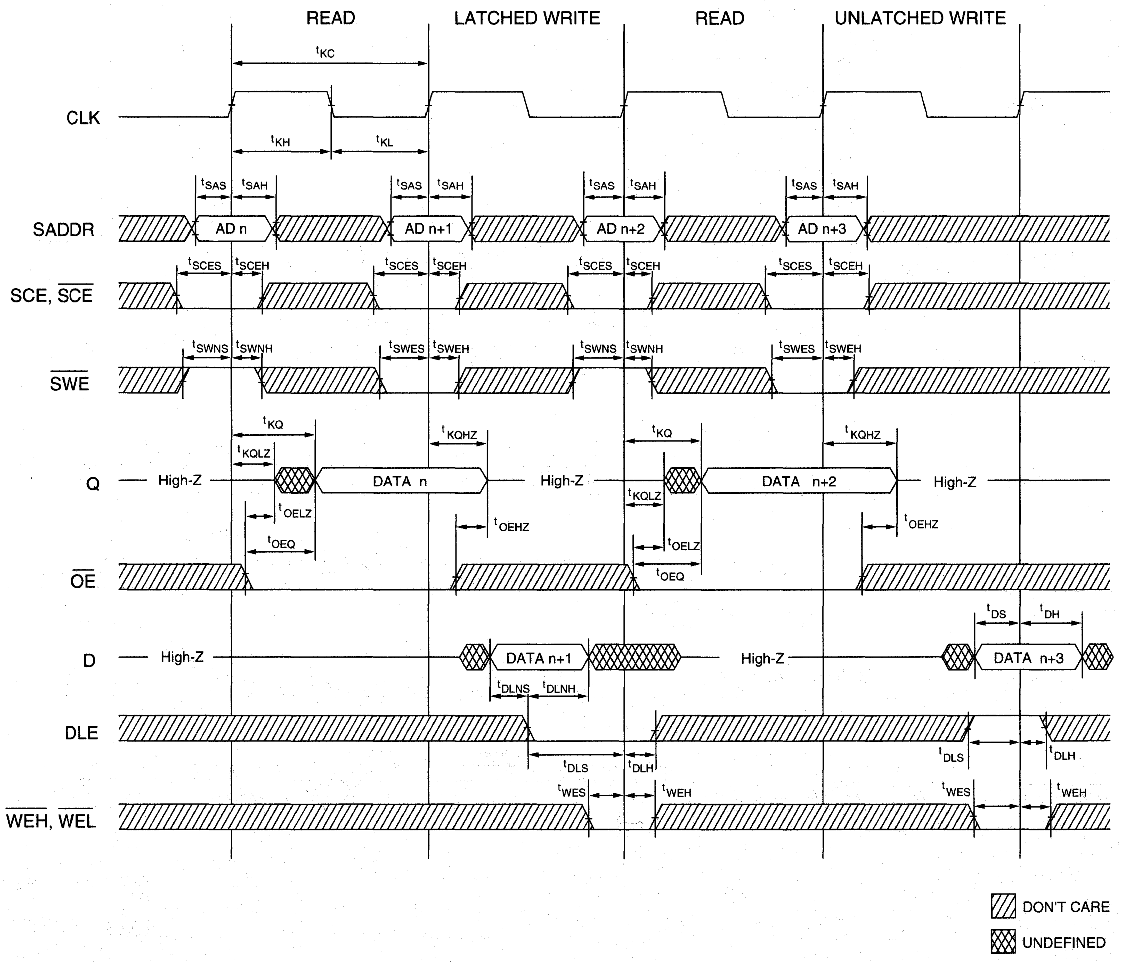
WRITE TIMING



NOTE:

1. Data is latched when DLE transitions from HIGH to LOW. When DLE is HIGH, the latch is transparent and data flows through the latch.
2. Asynchronous write enables ($\overline{\text{WEH}}$, $\overline{\text{WEL}}$) are available for use as byte write enables at the system level. They are also available to perform a LATE WRITE cycle abort.
3. When synchronous chip enables (SCE, $\overline{\text{SCE}}$) are inactive, the part is deselected.

READ/WRITE TIMING



SRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Package and No. of Pins			Process	Page
				DIP	ZIP	SIMM		
128K x 8	$\overline{CE}$ & $\overline{OE}$	MT4S1288	30, 35, 45	32	-	-	CMOS	3-1
32K x 16	$\overline{CE}$ & $\overline{OE}$	MT2S3216	30, 35, 45	40	-	-	CMOS	3-9
64K x 16	$\overline{CE}$ & $\overline{OE}$	MT4S6416	30, 35, 45	40	-	-	CMOS	3-17
16K x 32	$\overline{CE}$ & $\overline{OE}$	MT8S1632	15, 20, 25, 30, 35, 45	-	64	64	CMOS	3-25
64K x 32	$\overline{CE}$ & $\overline{OE}$	MT8S6432	20, 25, 30, 35, 45	-	64	64	CMOS	3-33
128K x 32	$\overline{CE}$ & $\overline{OE}$	MT4S12832	20, 25, 35, 45	-	64	64	CMOS	3-41
256K x 32	$\overline{CE}$ & $\overline{OE}$	MT8S25632	20, 25, 35, 45	-	64	64	CMOS	3-49

SRAM MODULE

128K x 8 SRAM

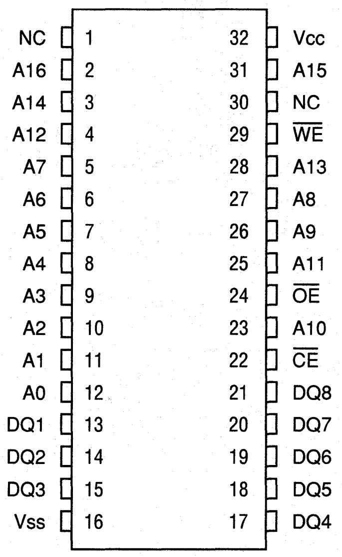
FEATURES

- High speed: 30, 35 and 45ns
- High-performance, low-power CMOS process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{\text{CE}}$ function
- All inputs and outputs are TTL compatible
- Pin compatible with monolithic 1 Meg SRAM

OPTIONS	MARKING
• Timing	
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
32-pin DIP (600 mil)	D
• 2V data retention (Available in 45ns, CMOS decoder version only)	L

PIN ASSIGNMENT (Top View)

32-Pin DIP
(K-1)



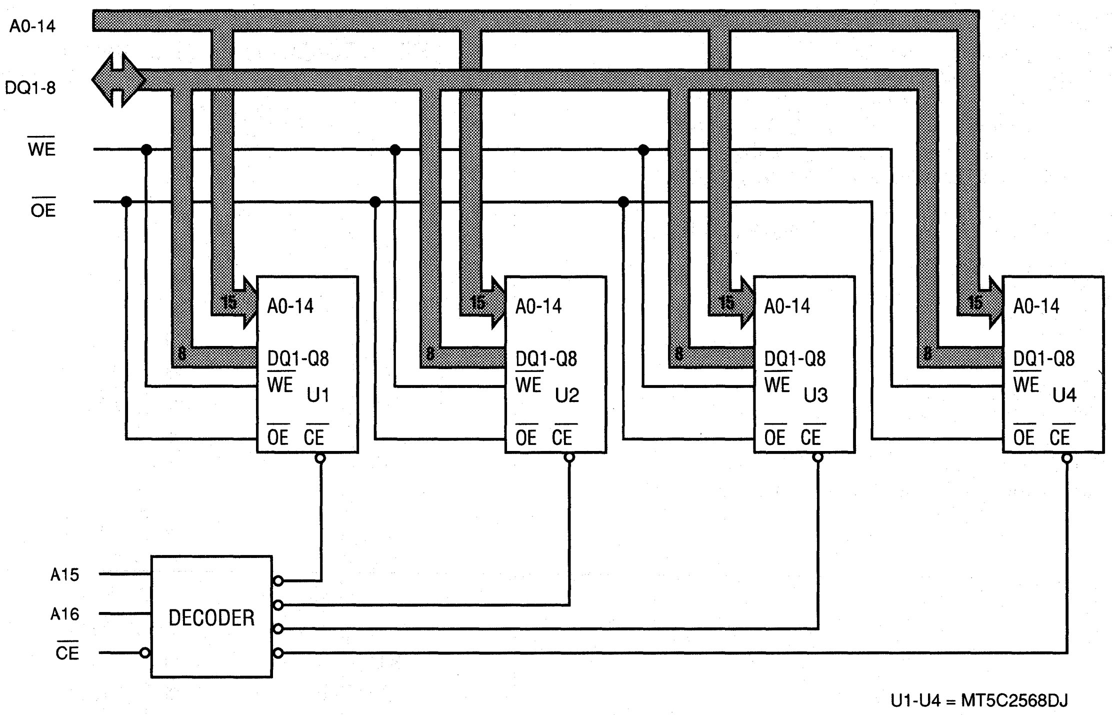
GENERAL DESCRIPTION

The MT4S1288 is a high-speed SRAM memory module containing 131,072 words organized in a x8-bit configuration. The module consists of four 32K x 8 fast static RAMs and a single decoder mounted on a 32-pin DIP, FR4 printed circuit board. Depending upon the speed of the module, the decoder will be either TTL (30ns and 35ns) or CMOS (45ns).

The decoder interprets the higher order address bits (A15 and A16) to select one of the four fast static RAMs. Data is written into the SRAM memory when both write enable ($\overline{\text{WE}}$) and chip enable ($\overline{\text{CE}}$) inputs are LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH, and $\overline{\text{CE}}$ and output enable ($\overline{\text{OE}}$) are LOW. $\overline{\text{CE}}$ sets the output in High-Z for additional system design flexibility and memory expansion may be achieved through use of the $\overline{\text{OE}}$ and $\overline{\text{CE}}$ functions.

The Micron SRAM family uses high-speed, low-power CMOS designs featuring a four-transistor memory cell and double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V DC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature .... -55°C to +125°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

					MAX				
DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**-30**	**-35**	**-45**	**UNITS**	**NOTES**
Input High (Logic 1) Voltage			V_{IH}	2.2	Vcc+1	Vcc+1	Vcc+1	V	
Input Low (Logic 0) Voltage			V_{IL}	-0.5	0.8	0.8	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	A0-A14, $\overline{WE}$, $\overline{OE}$	I_{LI}	-20	20	20	20	µA	
		A15, A16, $\overline{CE}$			600	600	1.0	µA	
Input/Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	DQ1-DQ8	I_{LO}	-20	20	20	20	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4			V	1	
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}	0.4	0.4	0.4	0.4	V	1

				MAX				
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-30**	**-35**	**-45**	**UNITS**	**NOTES**
Operating Current: TTL Input Levels	$\overline{CE} \le V_{IL}$; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	170	210	200	250	mA	3, 13
Standby Current: TTL Input Levels	$\overline{CE} \ge V_{IH}$, Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	60	120	120	100	mA	13
Standby Current: CMOS Input Levels	$\overline{CE} \ge V_{CC} -0.2$; Vcc = MAX $V_{IL} \le V_{SS} +0.2$ $V_{IH} \ge V_{CC} -0.2$; f = 0	I_{SB2}	5	40	40	20	mA	13

CAPACITANCE

			MAX				
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-30**	**-35**	**-45**	**UNITS**	**NOTES**
Input Capacitance: A0-A14 $\overline{WE}$,& $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_{I1}	28	28	28	pF	4
Input Capacitance: A15, A16 & $\overline{CE}$		C_{I2}	5	5	4.5	pF	4
Input/Output Capacitance: DQ1-DQ8		C_{IO}	28	28	28	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C $\leq T_A \leq$ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-30		-35		-45			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle									
READ cycle time	^{t}RC	30		35		45		ns	
Address access time	^{t}AA		30		35		45	ns	
Chip Enable access time	^{t}ACE		30		35		45	ns	
Output hold from address change	^{t}OH	5		5		5		ns	
Chip Enable LOW to output in Low-Z	^{t}LZCE	5		5		5		ns	7
Chip Enable to output in High-Z	^{t}HZCE		20		20		25	ns	6, 7
Chip Enable LOW to power-up time	^{t}PU	0		0		0		ns	
Chip Enable HIGH to power-down time	^{t}PD		30		35		45	ns	
Output Enable access time	^{t}AOE		10		12		15	ns	
Output Enable LOW to output in Low-Z	^{t}LZOE	0		0		0		ns	
Output Enable HIGH to output in High-Z	^{t}HZOE		10		12		15	ns	6
WRITE Cycle									
WRITE cycle time	^{t}WC	25		30		35		ns	
Chip Enable to end of write	^{t}CW	25		30		30		ns	
Address valid to end of write	^{t}AW	18		20		25		ns	
Address setup time	^{t}AS	0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		ns	
WRITE pulse width	^{t}WP	25		25		30		ns	
Data setup time	^{t}DS	15		15		20		ns	
Data hold time	^{t}DH	0		0		0		ns	
Write Enable LOW to output in Low-Z	^{t}LZWE	0		0		0		ns	7
Write Enable HIGH to output in High-Z	^{t}HZWE		12		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

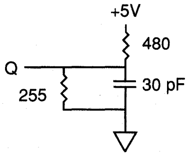


Fig. 1 OUTPUT LOAD EQUIVALENT

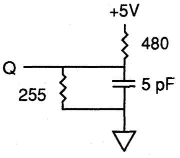


Fig. 2 OUTPUT LOAD EQUIVALENT

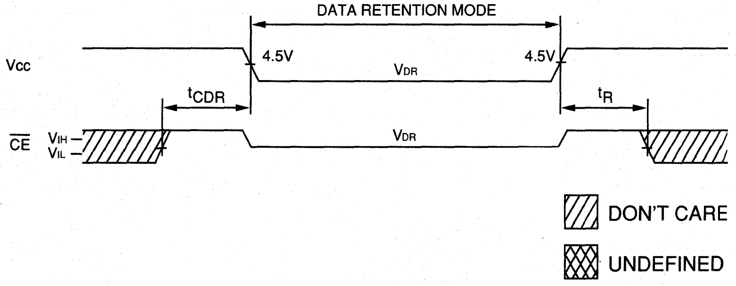
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. All $\overline{\text{CE}}$s are held in their active state.
10. Address valid prior to or coincident with latest occurring $\overline{\text{CE}}$.
11. The output will be in the High-Z state if $\overline{\text{OE}}$ is HIGH.
12. The first falling edge of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.

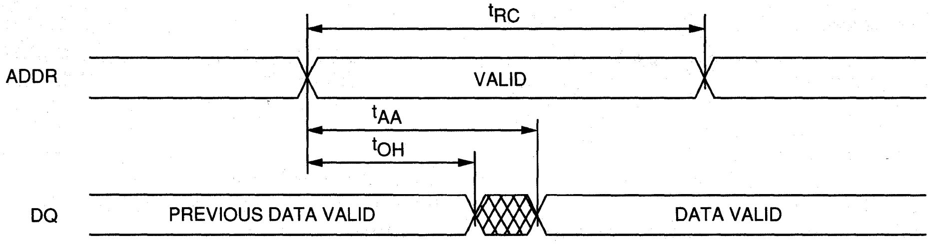
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{\text{CE}} \geq$ (Vcc -0.2V) $V_{IN} \geq$ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		0.5	1.5	mA	
		Vcc = 3V			1.5	2.0	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

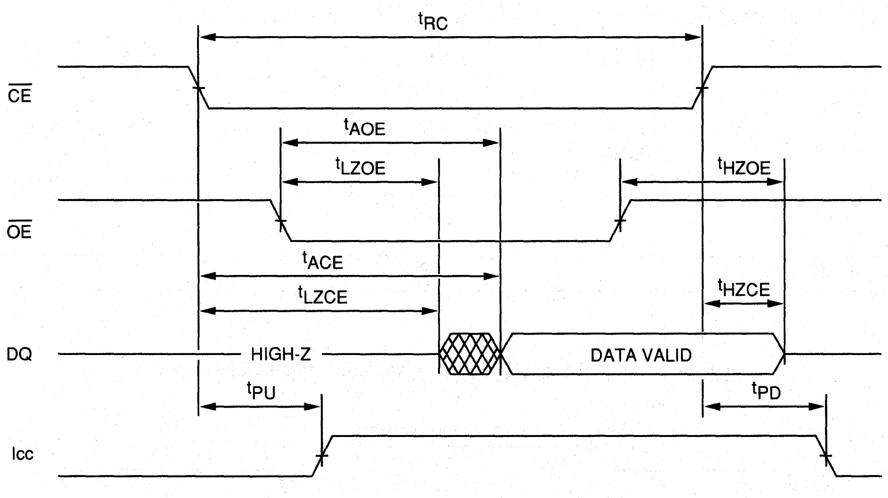
LOW Vcc DATA-RETENTION WAVEFORM



READ CYCLE NO. 1[8, 9]



READ CYCLE NO. 2[7, 8, 10]

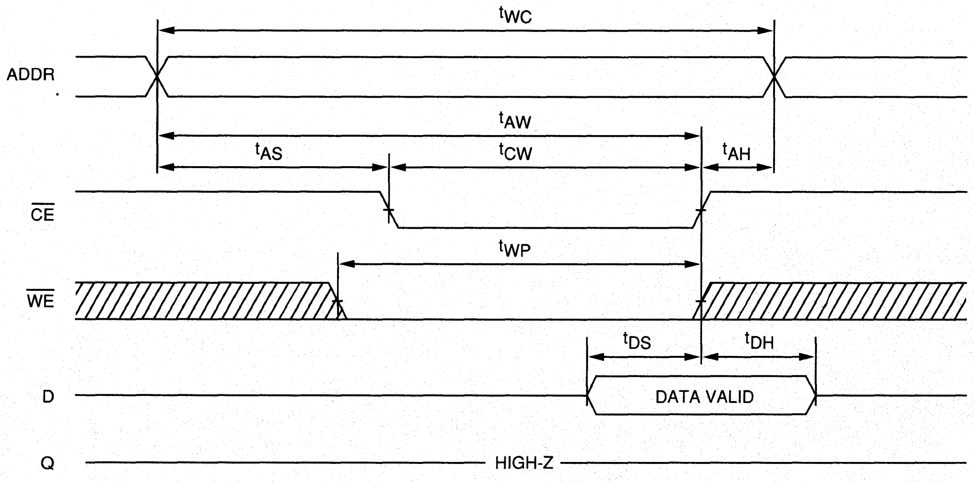


▨ DON'T CARE

▩ UNDEFINED

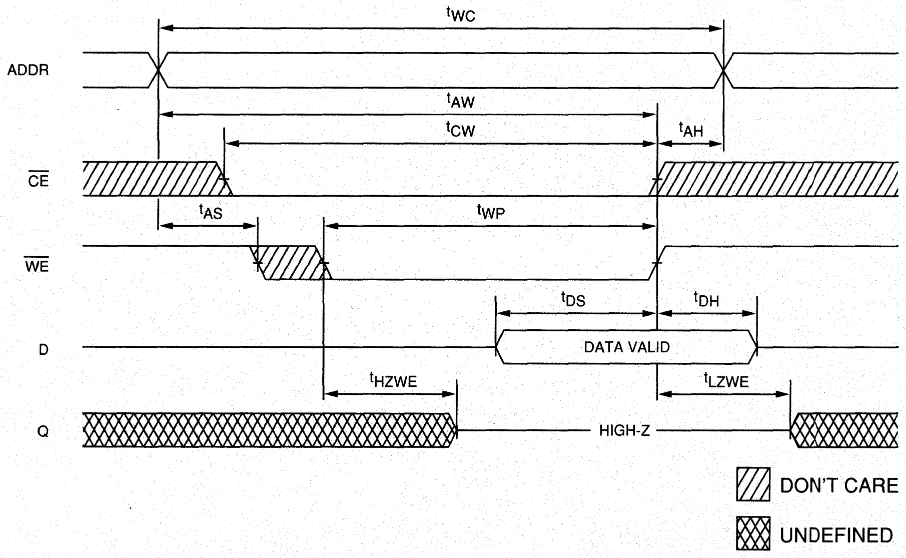
WRITE CYCLE NO. 1

(Chip Enable Controlled) [11, 12]



WRITE CYCLE NO. 2

(Write Enable Controlled) [11, 12]



SRAM MODULE

32K x 16 SRAM

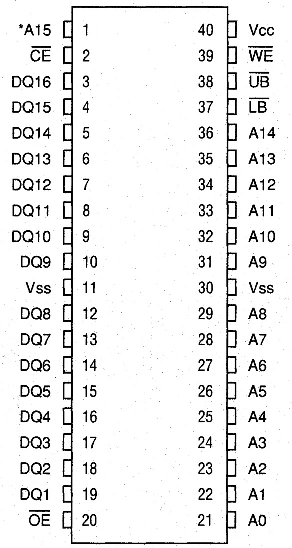
FEATURES

- High speed: 30, 35 and 45ns
- High-performance, low-power CMOS process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ function
- Upper and lower byte select
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
• Timing	
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
40-pin DIP (600 mil)	D
• 2V data retention (Available in 45ns, CMOS decoder versions only)	L

PIN ASSIGNMENT (Top View)

40-Pin DIP
(K-2)



*Address A15 must be connected to Vss.

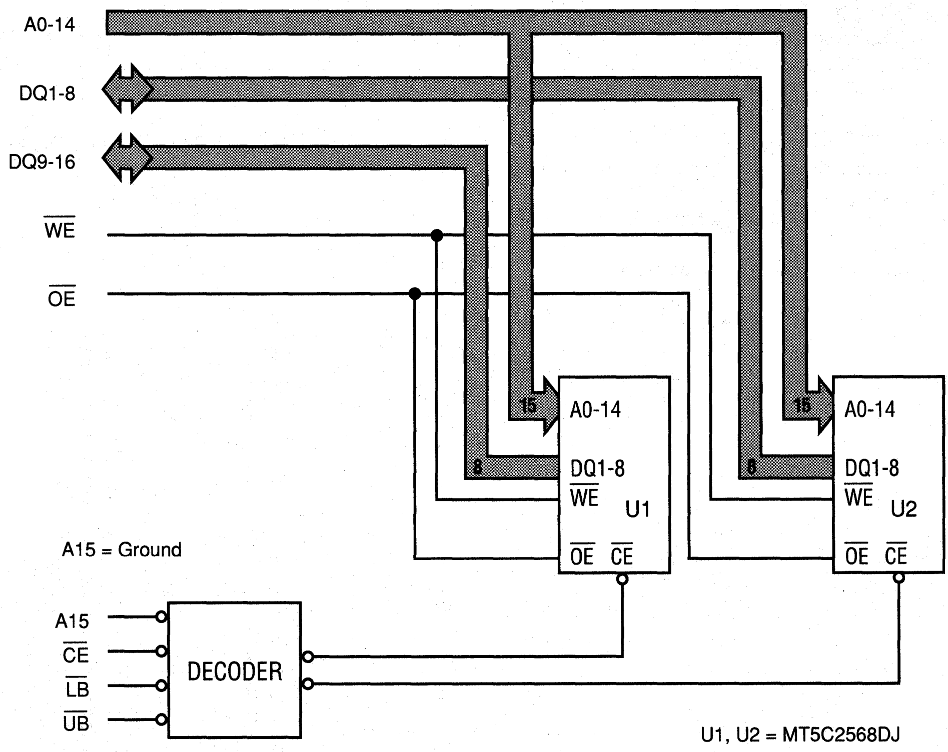
GENERAL DESCRIPTION

The MT2S3216 is a high-speed SRAM memory module containing 32,768 words organized in a x16-bit configuration. The module consists of two 32K x 8 fast static RAMs and a single decoder mounted on a 40-pin DIP, FR4 printed circuit board. Depending upon the speed of the module, the decoder will be either TTL (30ns and 35ns) or CMOS (45ns).

Data is written into the SRAM memory when both write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are LOW. Reading occurs when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{LB}$ and $\overline{UB}$ control the lower and upper byte selection. $\overline{CE}$ sets the output in High-Z for additional system design flexibility, and memory expansion may be achieved through use of the $\overline{CE}$ functions.

The Micron SRAM family uses high-speed, low-power CMOS designs featuring a four-transistor memory cell and double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V DC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



A15 = Ground

U1, U2 = MT5C2568DJ

TRUTH TABLE

MODE	$\overline{\text{CE}}$	$\overline{\text{UB}}$	$\overline{\text{LB}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A15	DQ OPERATION	POWER
STANDBY	H	X	X	X	X	L	HIGH-Z	STANDBY
STANDBY	L	H	H	X	X	L	HIGH-Z	STANDBY
READ: WORD	L	L	L	L	H	L	Q1-16	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	L	H	L	Q1-8	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	L	H	L	Q9-16	ACTIVE (x8)
READ: WORD	L	L	L	H	H	L	HIGH-Z	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	H	H	L	HIGH-Z	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	H	H	L	HIGH-Z	ACTIVE (x8)
WRITE: WORD	L	L	L	X	L	L	D1-16	ACTIVE (x16)
WRITE: LOWER BYTE	L	H	L	X	L	L	D1-8	ACTIVE (x8)
WRITE: UPPER BYTE	L	L	H	X	L	L	D9-16	ACTIVE (x8)

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature .... -55°C to +125°C
Power Dissipation 2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX -30	MAX -35	MAX -45	UNITS	NOTES
Input High (Logic 1) Voltage	A0-A14, $\overline{WE}$, $\overline{OE}$		V_{IH}	2.2	Vcc+1	Vcc+1	Vcc+1	V	
	A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$		V_{IH}	2.0	Vcc+1	Vcc+1	Vcc+1	V	
Input Low (Logic 0) Voltage	A0-A14, $\overline{WE}$, $\overline{OE}$		V_{IL}	-0.5	0.8	0.8	0.8	V	1, 2
	A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$		V_{IL}	-0.5	0.8	0.8	0.9	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	A0-A14, $\overline{WE}$, $\overline{OE}$	I_{LI}	-10	10	10	10	µA	
		A15, $\overline{CE}$			1,200	1,200	2.0	µA	
		$\overline{UB}$, $\overline{LB}$			600	600	1.0	µA	
Input/Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	DQ1-DQ16	I_{LO}	-5	5	5	5	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4			V	1	
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	0.4	0.4	V	1

DESCRIPTION		CONDITIONS	SYMBOL	TYP	MAX -30	MAX -35	MAX -45	UNITS	NOTES
Operating Current: TTL Input Levels	(x16)	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ${}^tRC$ Outputs Open	I_{CC}	170	210	200	200	mA	3, 13
	(x8)			85	140	140	130	mA	3, 13
Standby Current: TTL Input Levels		$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX =1/ ${}^tRC$ Outputs Open	I_{SB1}	30	70	70	50	mA	13
Standby Current: CMOS Input Levels		$\overline{CE}$ ≥ Vcc -0.2; Vcc = MAX V_{IL} ≤ Vss +0.2 V_{IH} ≥ Vcc -0.2; f = 0	I_{SB2}	5	35	35	15	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX -30	MAX -35	MAX -45	UNITS	NOTES
Input Capacitance: A0-A14, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_{I1}	14	14	14	pF	4
Input Capacitance: A15, $\overline{CE}$		C_{I2}	10	10	9	pF	4
Input Capacitance: $\overline{UB}$, $\overline{LB}$		C_{I3}	5	5	4.5	pF	4
Input/Output Capacitance: DQ		C_{IO}	7	7	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-30		-35		-45			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle									
READ cycle time	^{t}RC	30		35		45		ns	
Address access time	^{t}AA		30		35		45	ns	
Chip Enable access time	^{t}ACE		30		35		45	ns	
Output hold from address change	^{t}OH	5		5		5		ns	
Chip Enable LOW to output in Low-Z	^{t}LZCE	5		5		5		ns	7
Chip Enable to output in High-Z	^{t}HZCE		20		20		25	ns	6, 7
Chip Enable LOW to power-up time	^{t}PU	0		0		0		ns	
Chip Enable HIGH to power-down time	^{t}PD		30		35		45	ns	
Output Enable access time	^{t}AOE		10		12		15	ns	
Output Enable LOW to output in Low-Z	^{t}LZOE	0		0		0		ns	
Output Enable HIGH to output in High-Z	^{t}HZOE		10		12		15	ns	6
WRITE Cycle									
WRITE cycle time	^{t}WC	25		30		35		ns	
Chip Enable to end of write	^{t}CW	25		30		30		ns	
Address valid to end of write	^{t}AW	18		20		25		ns	
Address setup time	^{t}AS	0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		ns	
WRITE pulse width	^{t}WP	25		25		30		ns	
Data setup time	^{t}DS	15		15		20		ns	
Data hold time	^{t}DH	0		0		0		ns	
Write Enable LOW to output in Low-Z	^{t}LZWE	0		0		0		ns	7
Write Enable HIGH to output in High-Z	^{t}HZWE		12		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

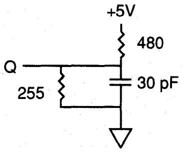


Fig. 1 OUTPUT LOAD EQUIVALENT

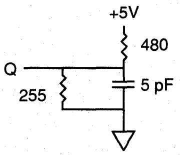


Fig. 2 OUTPUT LOAD EQUIVALENT

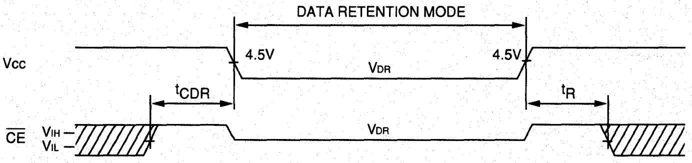
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. The output will be in the High-Z state if $\overline{OE}$ is HIGH.
12. The first falling edge of either $\overline{CE}$ or $\overline{WE}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{CE}$ or $\overline{WE}$ will terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		0.3	1.0	mA	
		Vcc = 3V			0.8	1.2	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

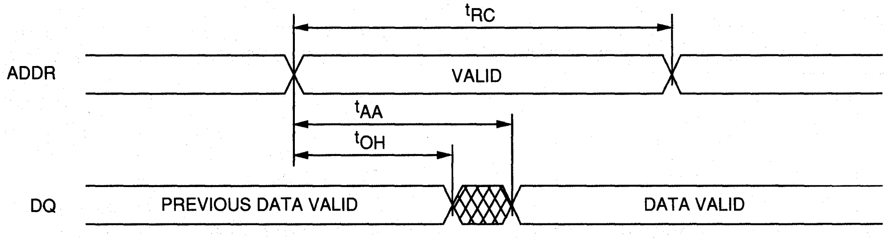
LOW Vcc DATA-RETENTION WAVEFORM



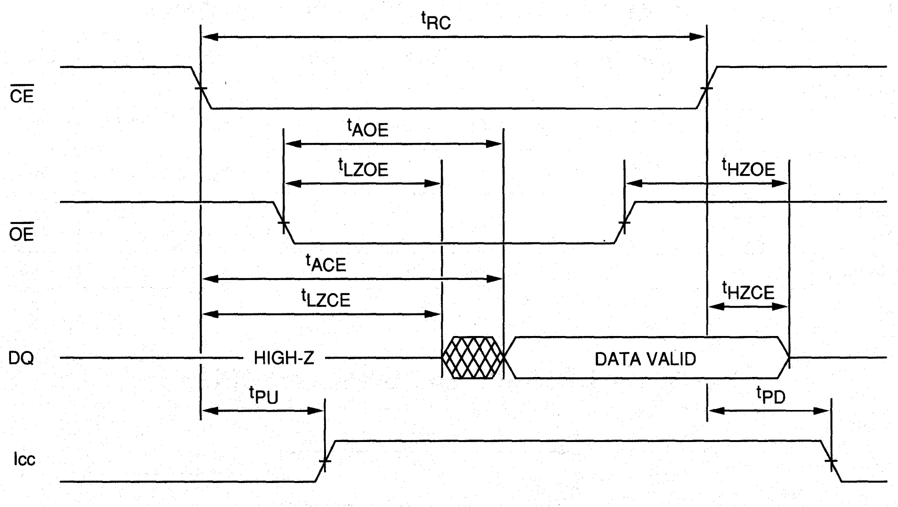
▨ DON'T CARE

▩ UNDEFINED

READ CYCLE NO. 1 [8, 9]



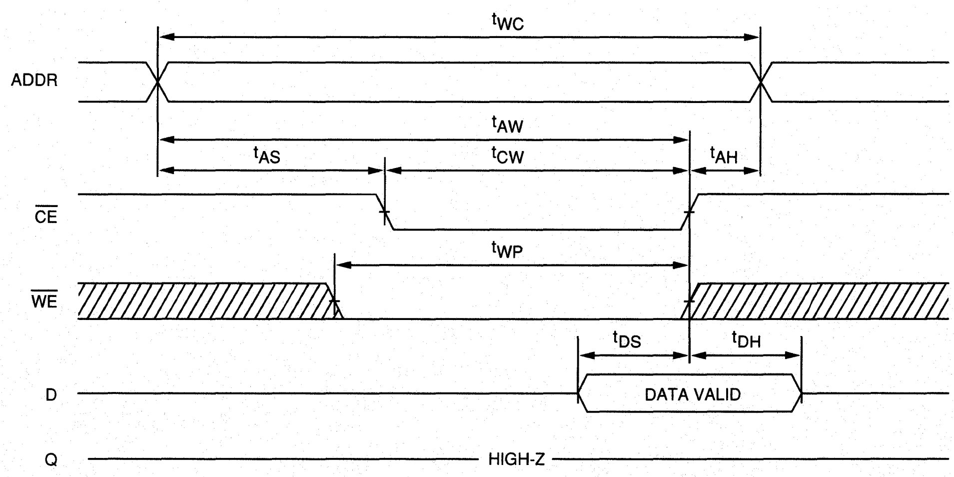
READ CYCLE NO. 2 [7, 8, 10]



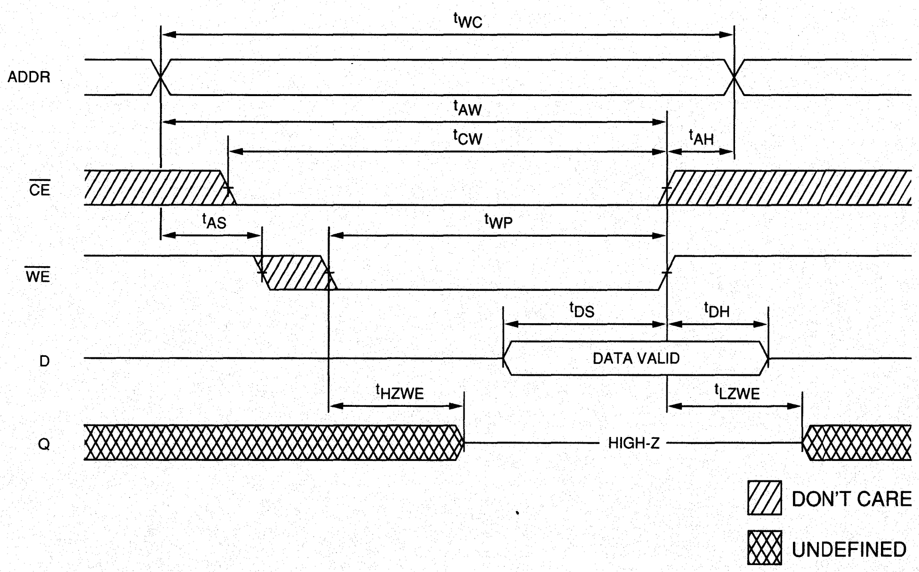
▨ DON'T CARE

☒ UNDEFINED

WRITE CYCLE NO. 1
(Chip Enable Controlled)[11, 12]



WRITE CYCLE NO. 2
(Write Enable Controlled)[11, 12]



MICRON
TECHNOLOGY, INC.

MT4S6416

SRAM MODULE

64K x 16 SRAM

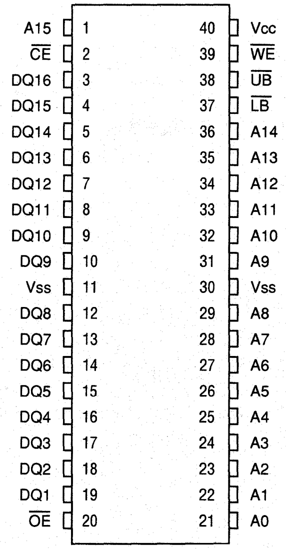
FEATURES

- High speed: 30, 35 and 45ns
- High-performance, low-power, CMOS process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ function
- Upper and lower byte select
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
• Timing	
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
40-pin DIP (600 mil)	D
• 2V data retention	L
(Available in the 45ns, CMOS decoder version only)	

PIN ASSIGNMENT (Top View)

40-Pin DIP
(K-3)



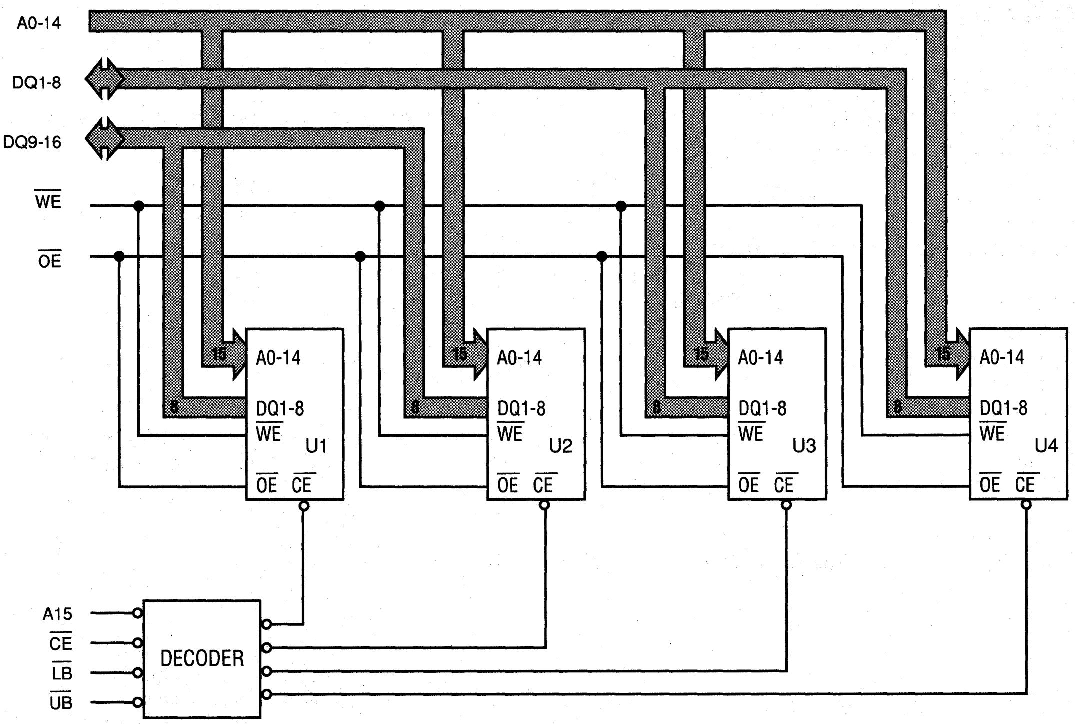
GENERAL DESCRIPTION

The MT4S6416 is a high-speed SRAM memory module containing 65,536 words organized in a x16-bit configuration. The module consists of four 32K x 8 fast static RAMs and a single decoder mounted on a 40-pin DIP, double-sided FR4 printed circuit board. Depending upon the speed of the module, the decoder will be either TTL (30ns and 35ns) or CMOS (45ns).

The decoder interprets the higher order address bit (A15) to select two of the four fast static RAMs. Data is written into the SRAM memory when both write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are LOW. Reading occurs when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{LB}$ and $\overline{UB}$ control the lower and upper byte selection. $\overline{CE}$ sets the output in High-Z for additional system design flexibility and memory expansion may be achieved through use of the $\overline{OE}$ function.

The Micron SRAM family uses high-speed, low-power CMOS designs featuring a four-transistor memory cell and double-layer metal, double-layer polysilicon technology. All module components can be powered from a single +5V DC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT5C2568DJ

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	DQ OPERATION	POWER
STANDBY	H	X	X	X	X	HIGH-Z	STANDBY
STANDBY	L	H	H	X	X	HIGH-Z	STANDBY
READ: WORD	L	L	L	L	H	Q1-16	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	L	H	Q1-8	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	L	H	Q9-16	ACTIVE (x8)
READ: WORD	L	L	L	H	H	HIGH-Z	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	H	H	HIGH-Z	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	H	H	HIGH-Z	ACTIVE (x8)
WRITE: WORD	L	L	L	X	L	D1-16	ACTIVE (x16)
WRITE: LOWER BYTE	L	H	L	X	L	D1-8	ACTIVE (x8)
WRITE: UPPER BYTE	L	L	H	X	L	D9-16	ACTIVE (x8)

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +7V
Storage Temperature .... -55°C to +125°C
Power Dissipation 4W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

					MAX				
DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**-30**	**-35**	**-45**	**UNITS**	**NOTES**
Input High (Logic 1) Voltage	A0-A14, $\overline{WE}$, $\overline{OE}$		V_{IH}	2.2	Vcc+1	Vcc+1	Vcc+1	V	
	A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$		V_{IH}	2.0	Vcc+1	Vcc+1	Vcc+1	V	
Input Low (Logic 0) Voltage	A0-A14, $\overline{WE}$, $\overline{OE}$		V_{IL}	-0.5	0.8	0.8	0.8	V	1, 2
	A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$		V_{IL}	-0.5	0.8	0.8	1.3	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	A0-A14	I_{LI}	-40	40	40	40	µA	
		A15, $\overline{CE}$			1,200	1,200	1.0	µA	
		$\overline{UB}$, $\overline{LB}$			600	600	1.0	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$		I_{LO}	-20	20	20	20	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4				V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	0.4	0.4	V	1

					MAX				
DESCRIPTION		**CONDITIONS**	**SYMBOL**	**TYP**	**-30**	**-35**	**-45**	**UNITS**	**NOTES**
Operating Current: TTL Input Levels	(x16)	$\overline{CE} \le V_{IL}$, V_{CC} = MAX f = MAX = $1/{}^tRC$ Outputs Open	I_{CC}	170	250	250	290	mA	3, 13
	(x8)			85	140	140	180	mA	13
Standby Current: TTL Input Levels		$\overline{CE} \ge V_{IH}$, V_{CC} = MAX f = MAX = $1/{}^tRC$ Outputs Open	I_{SB1}	60	120	120	100	mA	13
Standby Current: CMOS Input Levels		$\overline{CE} \ge V_{CC}$ -0.2, V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2 $V_{IH} \ge V_{CC}$ -0.2, f = 0	I_{SB2}	5	40	40	20	mA	13

CAPACITANCE

			MAX				
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-30**	**-35**	**-45**	**UNITS**	**NOTES**
Input Capacitance: A0-A14, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz V_{CC} = 5V	C_{I1}	32	32	16	pF	4
Input Capacitance: A15, $\overline{CE}$		C_{I2}	10	10	9	pF	4
Input Capacitance: $\overline{UB}$, $\overline{LB}$		C_{I3}	5	5	4.5	pF	4
Input/Output Capacitance: DQ		C_{IO}	16	16	16	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^{t}RC	30		35		45		ns	
Address access time	^{t}AA		30		35		45	ns	
Chip Enable access time	^{t}ACE		30		35		45	ns	
Output hold from address change	^{t}OH	5		5		5		ns	
Chip Enable LOW to output in Low-Z	^{t}LZCE	5		5		5		ns	7
Chip Enable to output in High-Z	^{t}HZCE		20		20		25	ns	6, 7
Chip Enable LOW to power-up time	^{t}PU	0		0		0		ns	
Chip Enable HIGH to power-down time	^{t}PD		30		35		45	ns	
Output Enable access time	^{t}AOE		20		20		25	ns	
Output Enable LOW to output in Low-Z	^{t}LZOE	0		0		0		ns	
Output Enable HIGH to output in High-Z	^{t}HZOE		20		20		30	ns	6
WRITE Cycle									
WRITE cycle time	^{t}WC	30		35		45		ns	
Chip Enable to end of write	^{t}CW	25		30		30		ns	
Address valid to end of write	^{t}AW	25		25		30		ns	
Address setup time	^{t}AS	0		0		0		ns	
Address hold from end of write	^{t}AH	2		2		2		ns	
WRITE pulse width	^{t}WP	25		25		30		ns	
Data setup time	^{t}DS	15		15		18		ns	
Data hold time	^{t}DH	0		0		0		ns	
Write Enable LOW to output in Low-Z	^{t}LZWE	0		0		0		ns	7
Write Enable HIGH to output in High-Z	^{t}HZWE		20		15		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

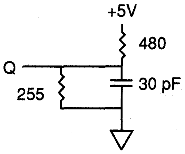


Fig. 1 OUTPUT LOAD EQUIVALENT

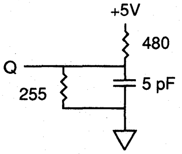


Fig. 2 OUTPUT LOAD EQUIVALENT

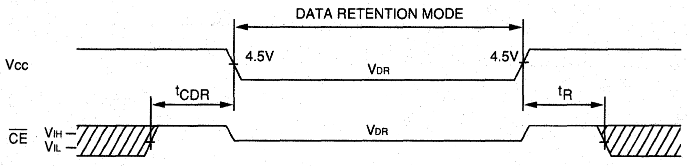
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE and ^{t}HZWE are less than ^{t}LZCE and ^{t}LZWE respectively.
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. The output will be in the High-Z state if $\overline{\text{OE}}$ is HIGH.
12. The first falling edge of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{\text{CE}}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		0.5	1.5	mA	
		Vcc = 3V			1.5	2.0	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

LOW Vcc DATA-RETENTION WAVEFORM

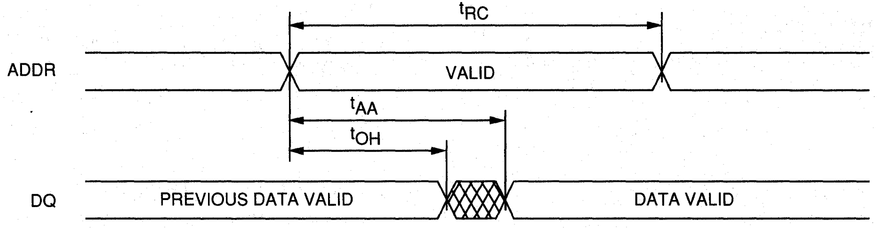


▨ DON'T CARE

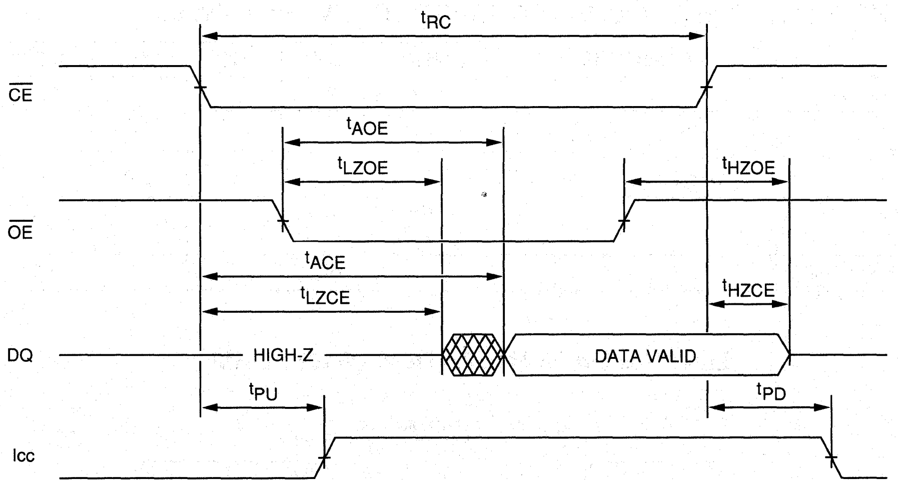
⊠ UNDEFINED

SRAM MODULE

READ CYCLE NO. 1[8, 9]



READ CYCLE NO. 2[7, 8, 10]

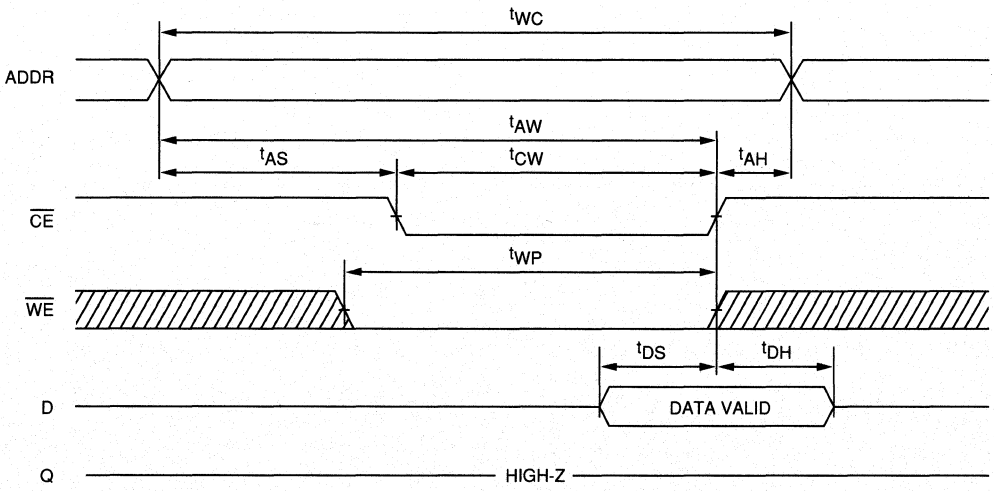


▨ DON'T CARE

▩ UNDEFINED

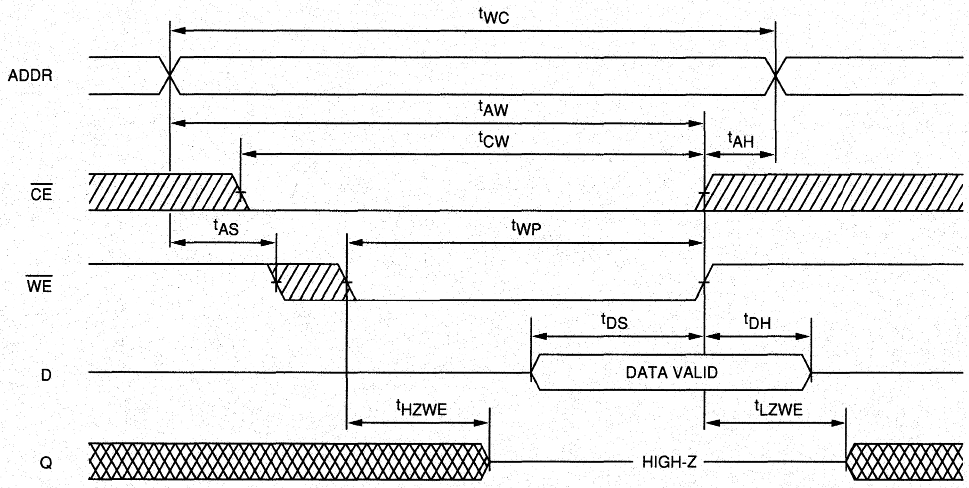
WRITE CYCLE NO. 1

(Chip Enable Controlled)[11, 12]



WRITE CYCLE NO. 2

(Write Enable Controlled)[11, 12]



▨ DON'T CARE

▩ UNDEFINED

MICRON TECHNOLOGY, INC.

MT8S1632

SRAM MODULE

16K x 32 SRAM

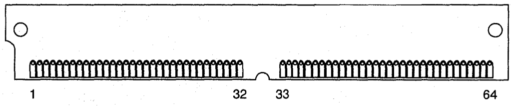
FEATURES

- High speed: 15, 20, 25, 30, 35 and 45ns
- High-performance, low-power, CMOS process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ functions
- Low profile (.50 inches maximum height)
- All inputs and outputs are TTL compatible
- Industry standard pinout
- Upgradable with 64K x 32, 128K x 32 and 256K x 32 modules

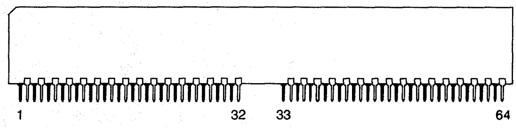
OPTIONS	MARKING
• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
64-pin SIMM	M
64-pin ZIP	Z
• 2V data retention	L

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(I-11)



64-Pin ZIP
(J-1)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{\text{CE4}}$	49	A4
2	PD0	18	A9	34	$\overline{\text{CE3}}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	$\overline{\text{OE}}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{\text{WE}}$	44	DQ19	60	DQ23
13	A0	29	NC	45	DQ28	61	DQ31
14	A7	30	NC	46	DQ20	62	DQ24
15	A1	31	$\overline{\text{CE2}}$	47	A3	63	DQ32
16	A8	32	$\overline{\text{CE1}}$	48	A10	64	Vss

GENERAL DESCRIPTION

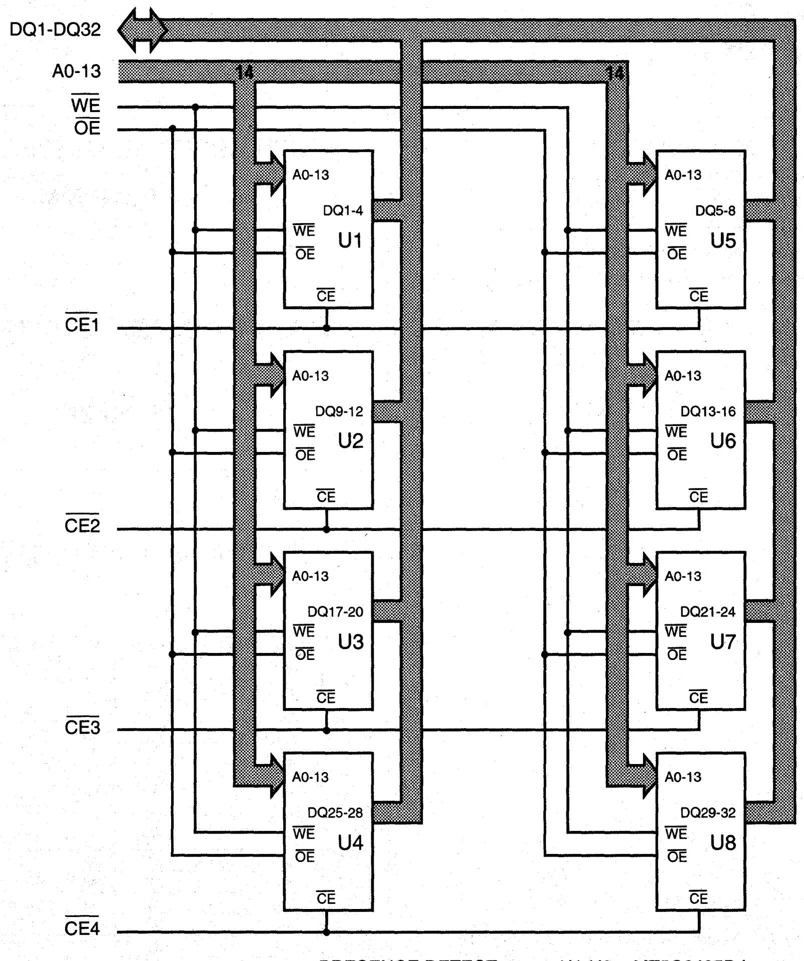
The MT8S1632 is a high-speed SRAM memory module containing 16,384 words organized in a x32-bit configuration. The module consists of eight 16K x 4 fast static RAMs mounted on a 64-pin, double-sided, FR4-printed circuit board.

Data is written into to the SRAM memory when write enable ($\overline{\text{WE}}$) and chip enable ($\overline{\text{CE}}$) inputs are both LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH and $\overline{\text{CE}}$ and output enable ($\overline{\text{OE}}$) are LOW. $\overline{\text{CE}}$ can set the output in High-Z for additional flexibility in system design, and memory expansion is accomplished by use of the $\overline{\text{OE}}$ function.

PD0 and PD1 identify the module's density, allowing interchangeable use of alternate-density, industry standard modules. Four chip enable inputs, ($\overline{\text{CE1}}$, $\overline{\text{CE2}}$, $\overline{\text{CE3}}$ and $\overline{\text{CE4}}$), are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5VDC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT
PD0 = Vss
PD1 = No Connect

U1-U8 = MT5C6405DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-40	40	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-15	-20	-25	-30	-35	-45	UNITS	NOTES
Operating Current: TTL Input Levels	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^{t}RC Outputs Open	Icc	520	960	880	800	800	720	720	mA	3, 13
Standby Current: TTL Input Levels	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^{t}RC Outputs Open	I_{SB1}	160	320	280	240	240	200	200	mA	13
Power Supply Current: Standby	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IL} ≤ Vss +0.2V V_{IH} ≥ Vcc -0.2V; f = 0	I_{SB2}	3.2	24	24	24	24	24	24	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A13, $\overline{WE}$, $\overline{CE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_I	70	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	15	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-15		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	15		20		25		30		35		45		ns	
Address access time	^tAA		15		20		25		30		35		45	ns	
Chip Enable access time	^tACE		12		15		20		25		30		40	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip disable to output in Low-Z	^tLZCE	3		5		5		5		5		5		ns	7
Chip Enable to output in High-Z	^tHZCE		7		8		8		8		8		8	ns	6, 7
Chip disable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip Enable to power-down time	^tPD		15		20		25		30		35		45	ns	
Output Enable access time	^tAOE		6		7		8		15		15		15	ns	
Output disable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output Enable to output in High-Z	^tHZOE		6		7		8		8		8		8	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	15		20		25		30		35		45		ns	
Chip Enable to end of write	^tCW	12		15		20		25		25		30		ns	
Address valid to end of write	^tAW	12		15		20		25		25		30		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	12		15		18		20		20		30		ns	
WRITE pulse width	$^tWP2$	14		18		20		25		25		30		ns	
Data setup time	^tDS	8		10		10		12		12		12		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		6		8		8		8		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

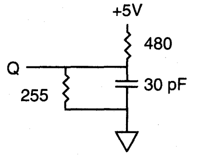


Fig. 1 OUTPUT LOAD EQUIVALENT

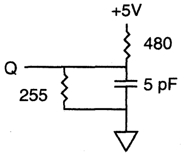


Fig. 2 OUTPUT LOAD EQUIVALENT

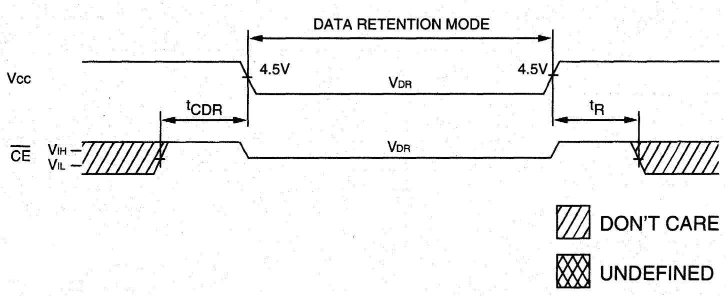
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. The output will be in the High-Z if $\overline{\text{OE}}$ is HIGH.
12. The first falling edge of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.

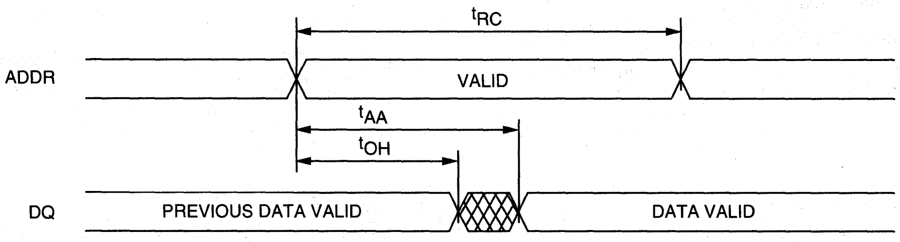
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{\text{CE}} \geq$ (Vcc -0.2V) $V_{IN} \geq$ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		760	2,000	µA	
		Vcc = 3V			1,000	3,200	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

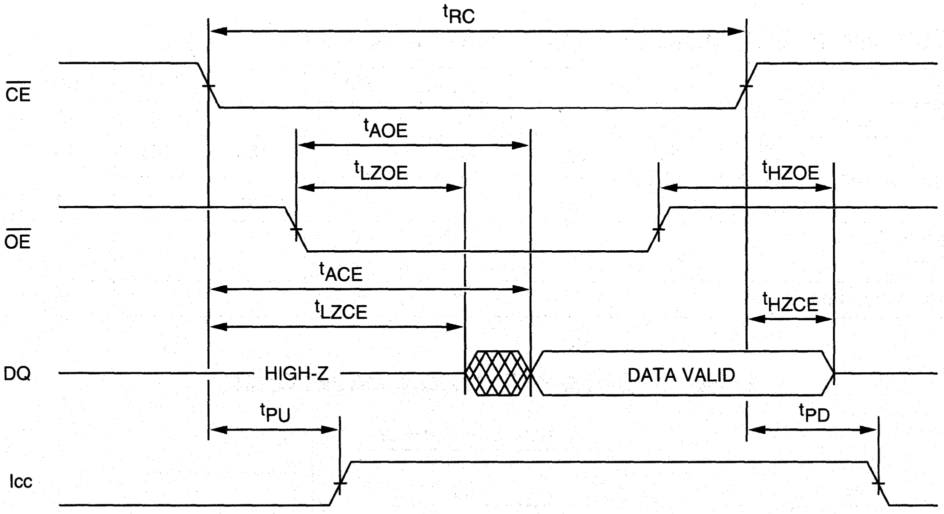
LOW Vcc DATA-RETENTION WAVEFORM



READ CYCLE NO. 1[8, 9]



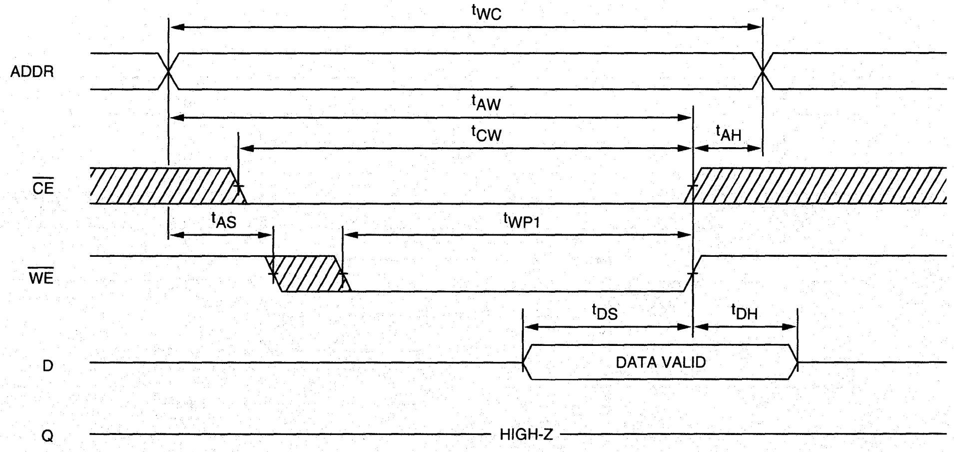
READ CYCLE NO. 2[7, 8, 10]



▨ DON'T CARE

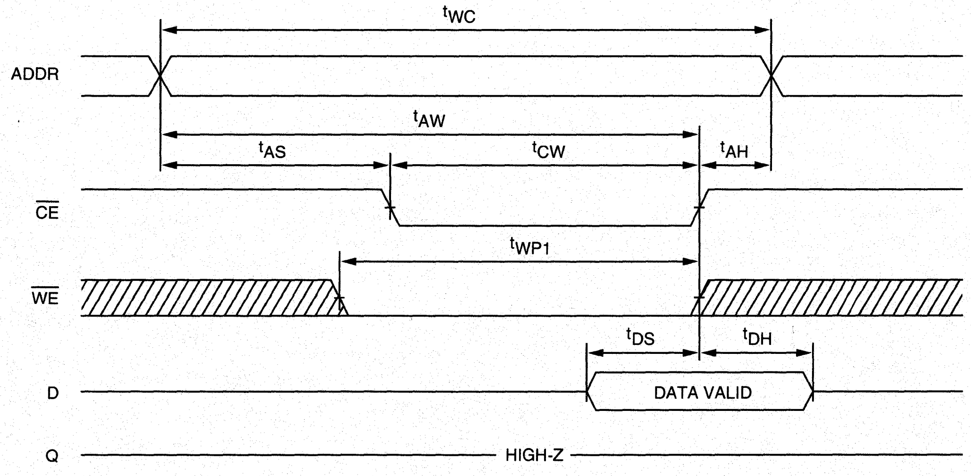
▩ UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

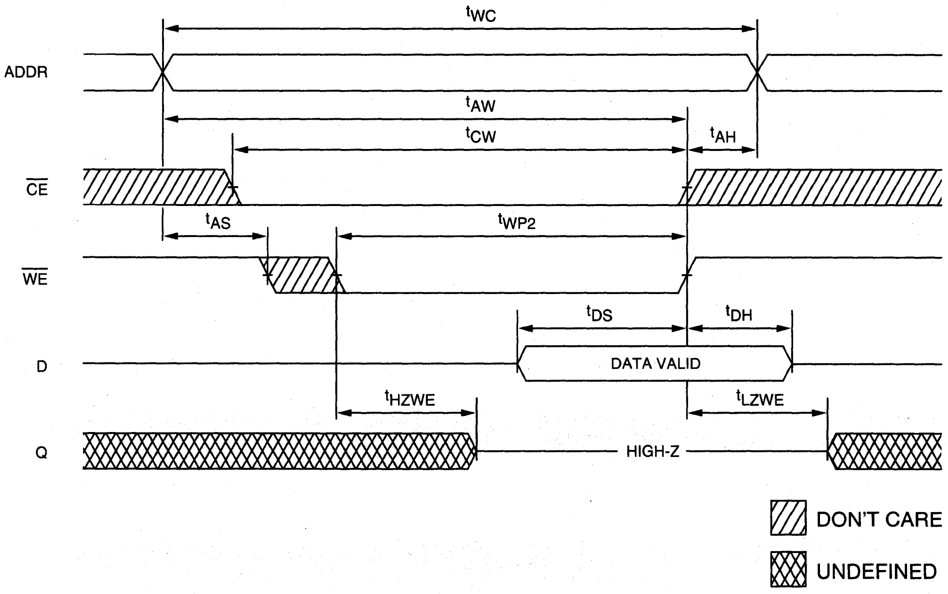
WRITE CYCLE NO. 2
(Chip Enable Controlled)



▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 3
(Write Enable Controlled)[11, 12]



SRAM MODULE

64K x 32 SRAM

FEATURES

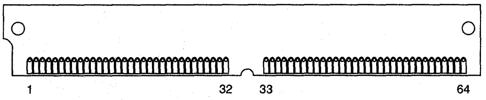
- Industry compatible pinout
- High speed: 20, 25, 30, 35 and 45ns
- High-performance, low-power CMOS process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ function
- Low profile (.50 inches maximum height)
- All inputs and outputs are TTL compatible

OPTIONS / MARKING

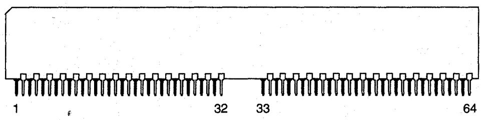
OPTIONS	MARKING
• Timing	
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
64-pin SIMM	M
64-pin ZIP	Z
• 2V data retention	L

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(I-11)



64-Pin ZIP
(J-1)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

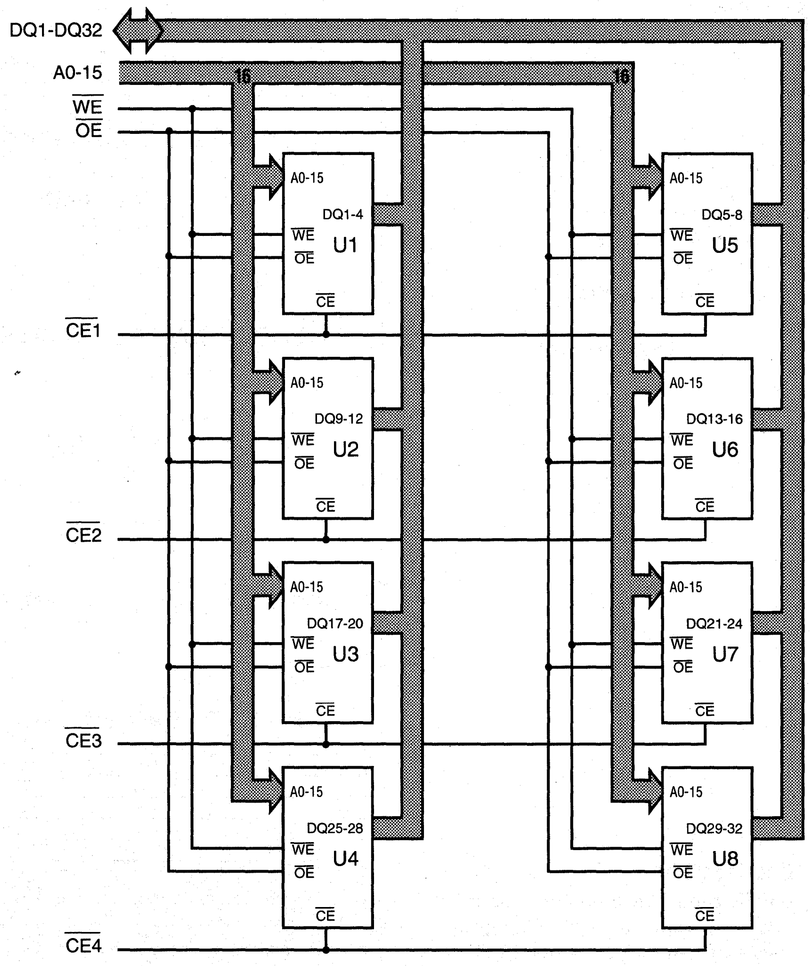
The MT8S6432 is a high-speed SRAM memory module containing 65,536 words organized in a x32-bit configuration. The module consists of eight 64K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4 printed circuit board.

Data is written into to the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density, allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5VDC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT
PD0 = No Connect
PD1 = Vss

U1-U8 = MT5C2565DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-40	40	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX						
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-20	-25	-30	-35	-45	UNITS	NOTES
Operating Current: TTL Input Levels	$\overline{CE} \le V_{IL}$; Vcc = MAX f = MAX = 1/ ᵗRC Outputs Open	I_{CC}	600	960	880	760	720	720	mA	3, 13
Standby Current: TTL Input Levels	$\overline{CE} \ge V_{IH}$; Vcc = MAX f = MAX = 1/ ᵗRC Outputs Open	I_{SB1}	88	240	200	200	200	200	mA	13
Power Supply Current: Standby	$\overline{CE} \ge V_{CC}$ -0.2V; Vcc = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	3.2	40	40	40	56	56	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A13, $\overline{WE}$, $\overline{CE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_I	72	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	15	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^{t}RC	20		25		30		35		45		ns	
Address access time	^{t}AA		20		25		30		35		45	ns	
Chip Enable access time	^{t}ACE		20		25		30		35		45	ns	
Output hold from address change	^{t}OH	3		5		5		5		5		ns	
Chip Enable LOW to output in Low-Z	^{t}LZCE	6		6		6		6		6		ns	7
Chip Enable to output in High-Z	^{t}HZCE		9		9		12		15		18	ns	6, 7
Chip Enable LOW to power-up time	^{t}PU	0		0		0		0		0		ns	
Chip Enable HIGH to power-down time	^{t}PD		20		25		30		35		45	ns	
Output Enable access time	^{t}AOE		8		8		10		12		15	ns	
Output Enable LOW to output in Low-Z	^{t}LZOE	0		0		0		0		0		ns	
Output Enable HIGH to output in High-Z	^{t}HZOE		7		7		10		12		15	ns	6
WRITE Cycle													
WRITE cycle time	^{t}WC	20		20		25		30		35		ns	
Chip Enable to end of write	^{t}CW	15		15		18		20		25		ns	
Address valid to end of write	^{t}AW	15		15		18		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		0		ns	
WRITE pulse width	^{t}WP	15		15		18		20		25		ns	
Data setup time	^{t}DS	10		10		12		15		20		ns	
Data hold time	^{t}DH	0		0		0		0		0		ns	
Write Enable LOW to output in Low-Z	^{t}LZWE	5		5		5		5		5		ns	7
Write Enable HIGH to output in High-Z	^{t}HZWE	0	10	0	10	0	12	0	15	0	18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

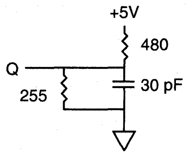


Fig. 1 OUTPUT LOAD EQUIVALENT

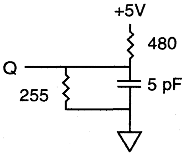


Fig. 2 OUTPUT LOAD EQUIVALENT

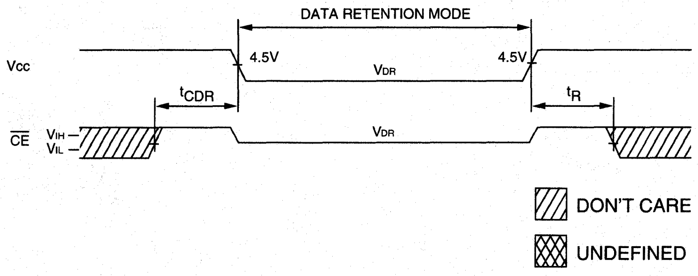
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. The output will be in the High-Z state if $\overline{OE}$ is HIGH.
12. The first falling edge of either $\overline{CE}$ or $\overline{WE}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{CE}$ or $\overline{WE}$ will terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.

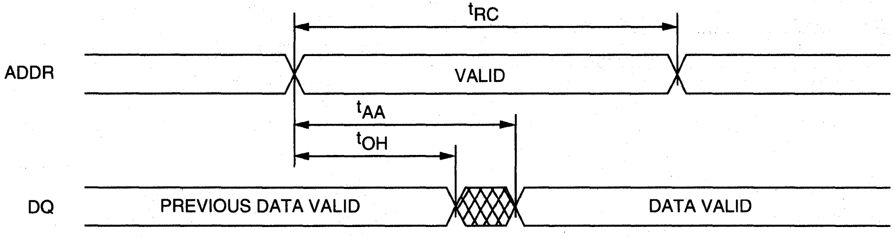
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		760	2,400	µA	
		Vcc = 3V			1,400	3,200	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

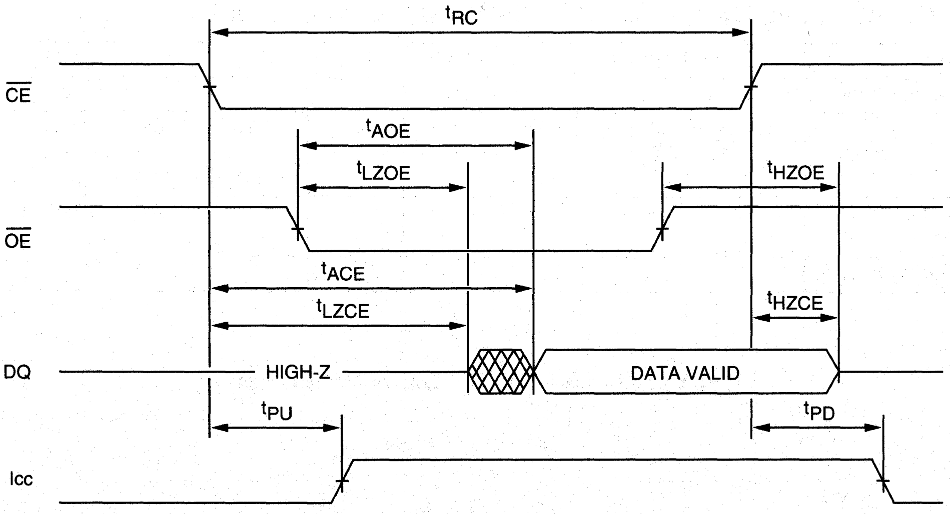
LOW Vcc DATA-RETENTION WAVEFORM



READ CYCLE NO. 1[8, 9]



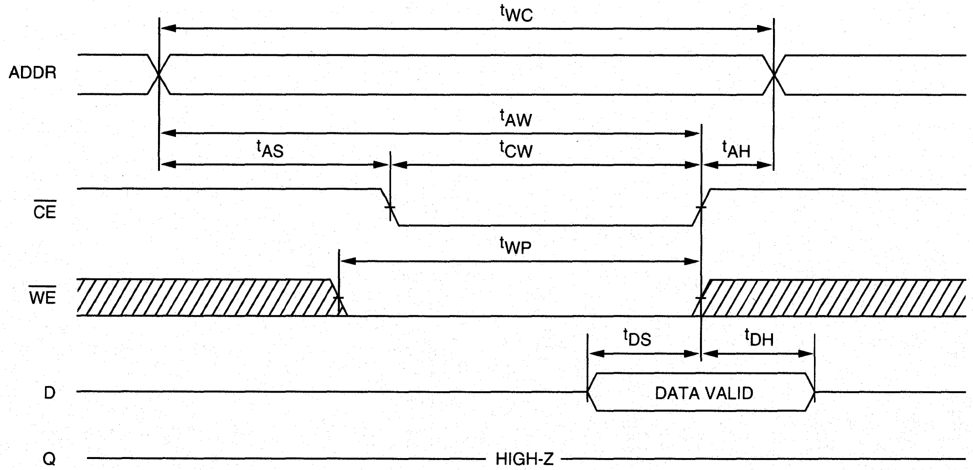
READ CYCLE NO. 2[7, 8, 10]



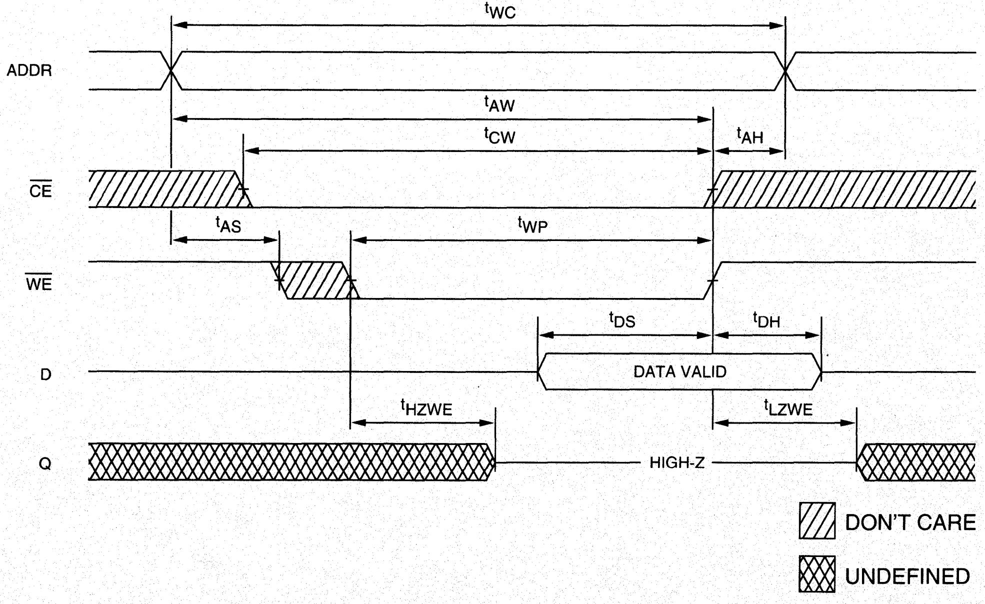
▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 1
(Chip Enable Controlled)[11, 12]



WRITE CYCLE NO. 2
(Write Enable Controlled)[11, 12]



SRAM MODULE

128K x 32 SRAM

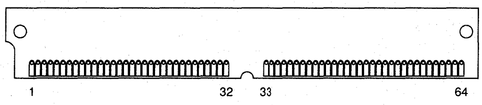
FEATURES

- Industry compatible pinout
- High speed: 20, 25, 35 and 45ns
- High-density 512KB design
- High-performance, low-power, CMOS process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{\text{CE}}$ function
- All inputs and outputs are TTL compatible
- Low profile (.600 inches maximum height)

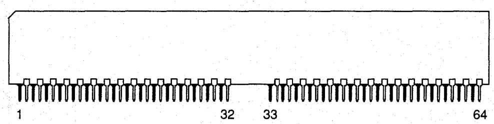
OPTIONS	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
64-pin SIMM	M
64-pin ZIP	Z
• Optional, 2V data retention	L

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(I-11)



64-Pin ZIP
(J-2)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{\text{CE4}}$	49	A4
2	PD0	18	A9	34	$\overline{\text{CE3}}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{\text{OE}}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{\text{WE}}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{\text{CE2}}$	47	A3	63	DQ32
16	A8	32	$\overline{\text{CE1}}$	48	A10	64	Vss

GENERAL DESCRIPTION

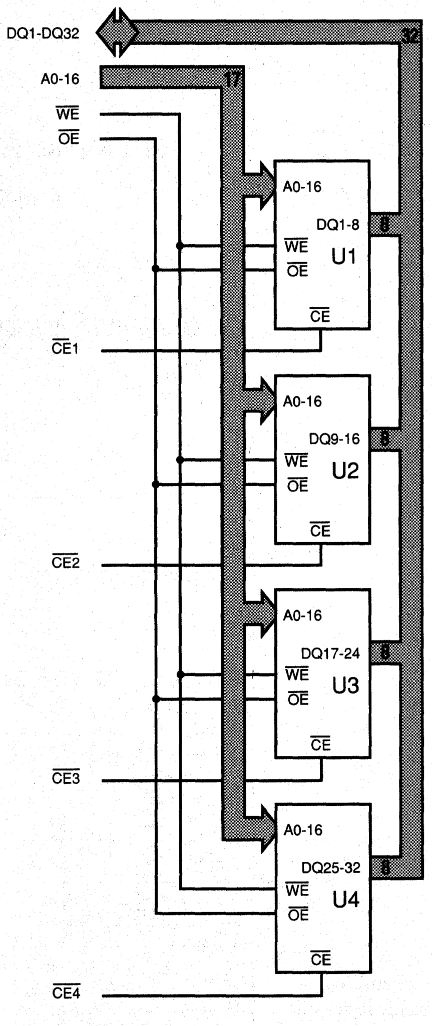
The MT4S12832 is a high-speed SRAM memory module containing 131,072 words organized in a x32-bit configuration. The module consists of four 128K x 8 fast static RAMs mounted on a 64-pin, single-sided, FR4-printed circuit board.

Data is written into the SRAM memory when write enable ($\overline{\text{WE}}$) and chip enable ($\overline{\text{CE}}$) inputs are both LOW. Reading is accomplished when $\overline{\text{WE}}$ remains HIGH and $\overline{\text{CE}}$ and output enable ($\overline{\text{OE}}$) are LOW. $\overline{\text{CE}}$ and/or $\overline{\text{OE}}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{\text{CE1}}$, $\overline{\text{CE2}}$, $\overline{\text{CE3}}$ and $\overline{\text{CE4}}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5VDC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT5C1008DJ

PRESENCE DETECT
PD0 = No Connect
PD1 = No Connect

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature .... -55°C to +125°C
Power Dissipation 4W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-20	20	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-20	20	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Operating Current: TTL Input Levels	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ${}^tRC$ Outputs Open	I_{CC}	380	560	500	460	440	mA	3, 13
Standby Current: TTL Input Levels	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ${}^tRC$ Outputs Open	I_{SB1}	68	140	120	100	100	mA	13
Standby Current: CMOS Input Levels	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	1.6	20	20	20	20	mA	13
"L" version only	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	1.2	6	6	6	6	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A13, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_I	35	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$; Vcc = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
READ cycle time	^{t}RC	20		25		35		45		ns	
Address access time	^{t}AA		20		25		35		45	ns	
Chip Enable access time	^{t}ACE		20		25		35		45	ns	
Output hold from address change	^{t}OH	5		5		5		5		ns	
Chip disable to output in Low-Z	^{t}LZCE	5		5		5		5		ns	7
Chip Enable to output in High-Z	^{t}HZCE		8		10		15		18	ns	6, 7
Chip disable to power-up time	^{t}PU	0		0		0		0		ns	
Chip Enable to power-down time	^{t}PD		20		25		35		45	ns	
Output Enable access time	^{t}AOE		6		8		12		15	ns	
Output disable to output in Low-Z	^{t}LZOE	0		0		0		0		ns	
Output Enable to output in High-Z	^{t}HZOE		6		10		12		15	ns	6
WRITE Cycle											
WRITE cycle time	^{t}WC	20		25		35		45		ns	
Chip Enable to end of write	^{t}CW	12		15		20		25		ns	
Address valid to end of write	^{t}AW	12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		ns	
WRITE pulse width	^{t}WP1	12		15		20		25		ns	
WRITE pulse width	^{t}WP2	15		15		20		25		ns	
Data setup time	^{t}DS	8		10		15		20		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	5		0		0		0		ns	7
Write Enable to output in High-Z	^{t}HZWE		8		10		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

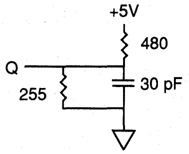


Fig. 1 OUTPUT LOAD EQUIVALENT

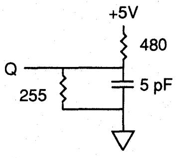


Fig. 2 OUTPUT LOAD EQUIVALENT

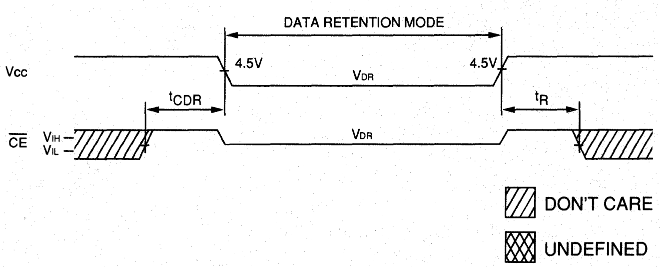
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1, unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{\text{WE}}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. The output will be in the High-Z state if $\overline{\text{OE}}$ is HIGH.
12. The first falling edge of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 25ns cycle time.

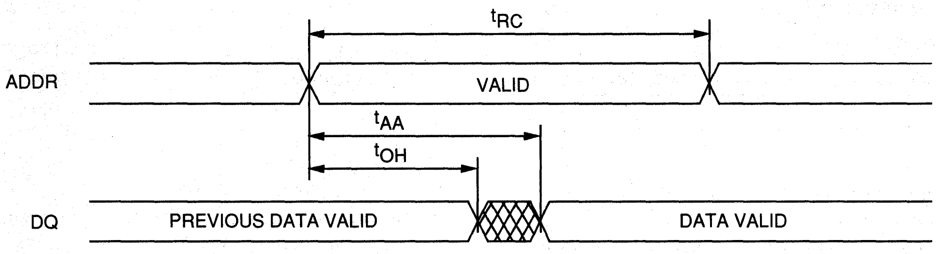
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{\text{CE}}$ ≥ (Vcc -0.2V)	Vcc = 2V	I_{CCDR}		140	800	µA	
	V_{IN} ≥ (Vcc -0.2V)	Vcc = 3V			280	1,600	µA	
	or ≤ 0.2V	Vcc = 5V			1,000	5,200	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

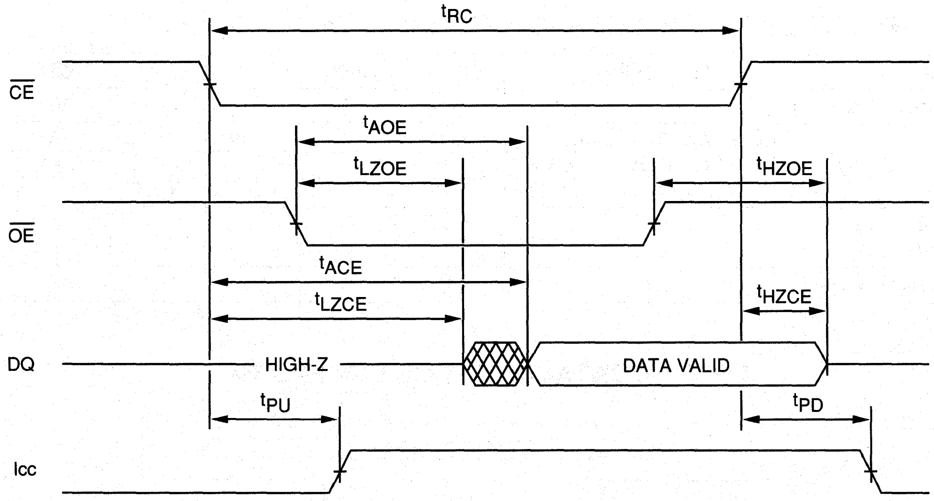
LOW Vcc DATA-RETENTION WAVEFORM



READ CYCLE NO. 1[8, 9]



READ CYCLE NO. 2[7, 8, 10]

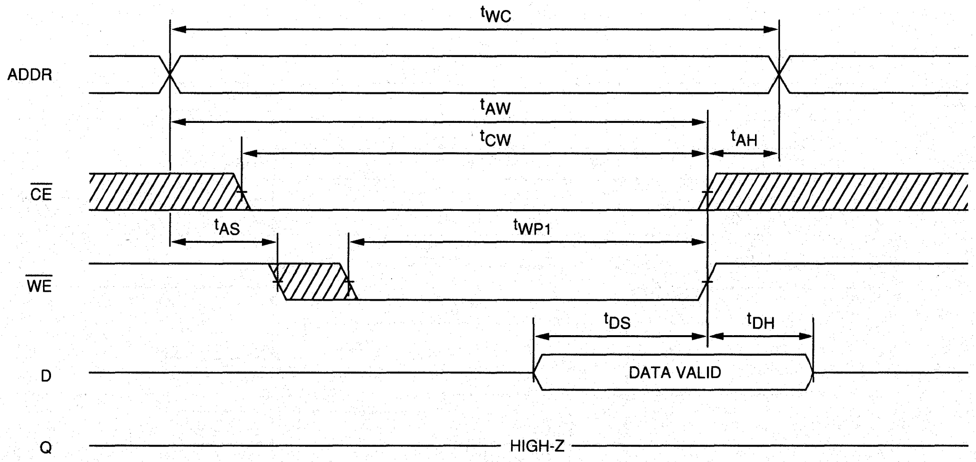


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 1

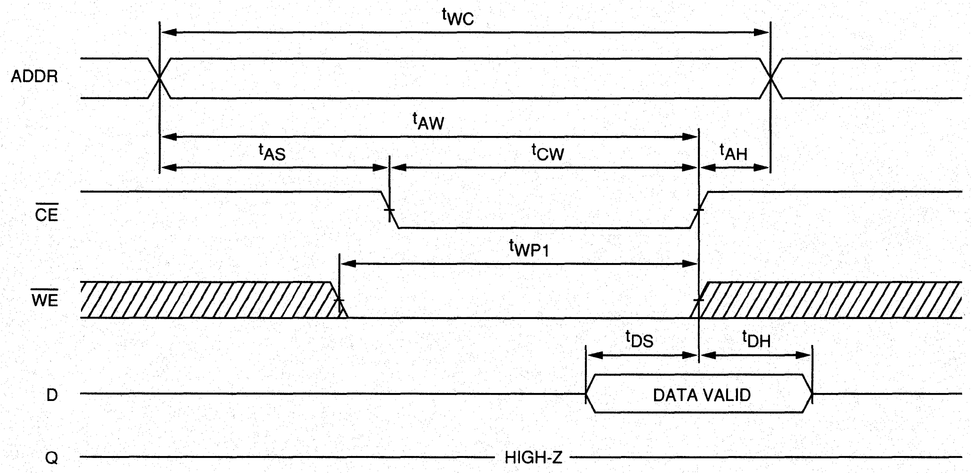
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 2

(Chip Enable Controlled)

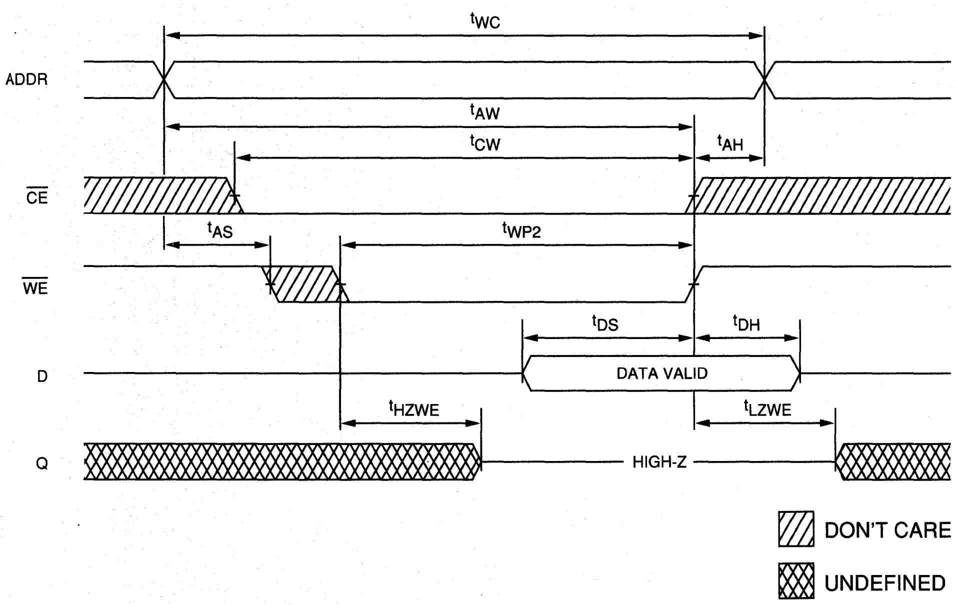


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 3

(Write Enable Controlled)[11, 12]



SRAM MODULE

256K x 32 SRAM

FEATURES

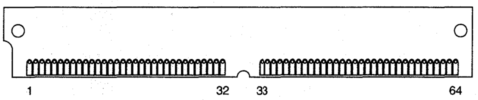
- Industry compatible pinout
- High speed: 20, 25, 35 and 45ns
- High-density 1MB design
- High-performance, low-power, CMOS process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ function
- All inputs and outputs are TTL compatible
- Low profile (.600 inches maximum height)

OPTIONS

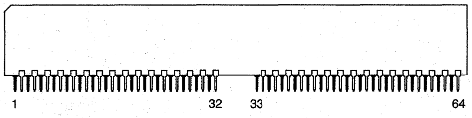
OPTIONS	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
64-pin SIMM	M
64-pin ZIP	Z
• Optional, 2V data retention	L

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(I-11)



64-Pin ZIP
(J-1)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	A17	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

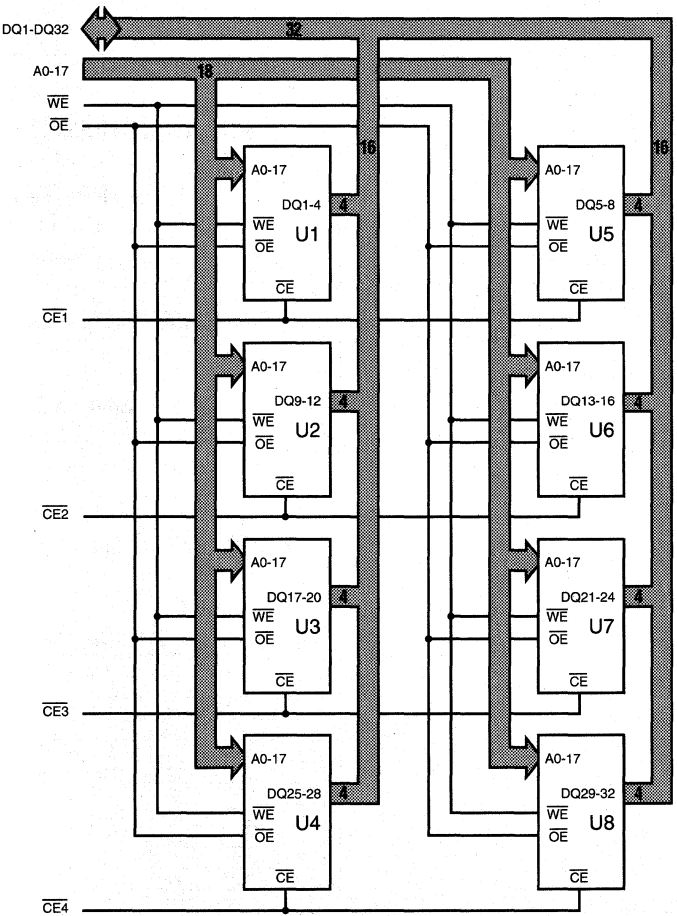
The MT8S25632 is a high-speed SRAM memory module containing 262,144 words organized in a x32-bit configuration. The module consists of eight 256K x 4 fast static RAMs mounted on a 64-pin, double-sided, FR4-printed circuit board.

Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in High-Z for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5VDC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT
PD0 = Vss
PD1 = Vss

U1-U8 = MT5C1005DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage			V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq Vcc$		I_{LI}	-5	5	µA	
Input/Output Leakage Current	Output(s) Disabled $0V \leq V_{OUT} \leq Vcc$	DQ1-DQ32	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Operating Current: TTL Input Levels	$\overline{CE} \leq V_{IL}$; Vcc = MAX f = MAX = 1/ ${}^tRC$ Outputs Open	Icc	760	1,120	1,000	920	880	mA	3, 13
Standby Current: TTL Input Levels	$\overline{CE} \geq V_{IH}$; Vcc = MAX f = MAX = 1/ ${}^tRC$ Outputs Open	I_{SB1}	560	280	240	200	200	mA	13
Standby Current: TTL Input Levels	$\overline{CE} \geq$ Vcc -0.2V; Vcc = MAX $V_{IL} \leq$ Vss +0.2V $V_{IH} \geq$ Vcc -0.2V; f = 0	I_{SB2}	3.2	40	40	40	40	mA	13
"L" version only	$\overline{CE} \geq$ Vcc -0.2V; Vcc = MAX $V_{IL} \leq$ Vss +0.2V $V_{IH} \geq$ Vcc -0.2V; f = 0	I_{SB2}	2.4	12	12	12	12	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance; A0-A17, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_{I1}	70	pF	4
Input Capacitance; $\overline{CE1}$-$\overline{CE4}$		C_{I2}	18	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^{t}RC	20		25		35		45		ns	
Address access time	^{t}AA		20		25		35		45	ns	
Chip Enable access time	^{t}ACE		20		25		35		45	ns	
Output hold from address change	^{t}OH	5		5		5		5		ns	
Chip disable to output in Low-Z	^{t}LZCE	5		5		5		5		ns	7
Chip Enable to output in High-Z	^{t}HZCE		8		10		15		18	ns	6, 7
Chip disable to power-up time	^{t}PU	0		0		0		0		ns	
Chip Enable to power-down time	^{t}PD		20		25		35		45	ns	
Output Enable access time	^{t}AOE		6		8		12		15	ns	
Output disable to output in Low-Z	^{t}LZOE	0		0		0		0		ns	
Output Enable to output in High-Z	^{t}HZOE		6		10		12		15	ns	6
WRITE Cycle											
WRITE cycle time	^{t}WC	20		25		35		45		ns	
Chip Enable to end of write	^{t}CW	12		15		20		25		ns	
Address valid to end of write	^{t}AW	12		15		20		25		ns	
Address setup time	^{t}AS	0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		ns	
WRITE pulse width	^{t}WP1	12		15		20		25		ns	
WRITE pulse width	^{t}WP2	15		15		20		25		ns	
Data setup time	^{t}DS	8		10		15		20		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	5		5		5		5		ns	7
Write Enable to output in High-Z	^{t}HZWE		8		10		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

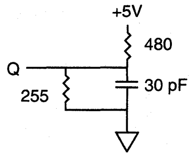


Fig. 1 OUTPUT LOAD EQUIVALENT

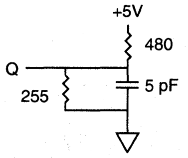


Fig. 2 OUTPUT LOAD EQUIVALENT

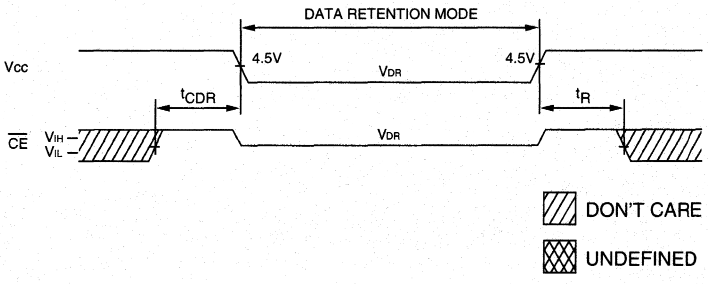
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. The output will be in the High-Z state if $\overline{OE}$ is HIGH.
12. The first falling edge of either $\overline{CE}$ or $\overline{WE}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{CE}$ or $\overline{WE}$ will terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 25ns cycle time.

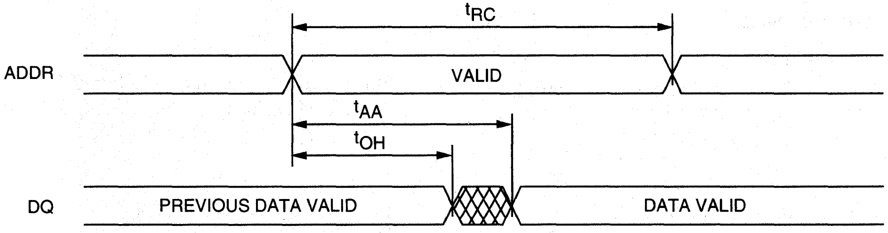
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		280	1,600	µA	
	VIN ≥ (Vcc -0.2V)	Vcc = 3V			560	3,200	µA	
	or ≤ 0.2V	Vcc = 5V			2,000	10,400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

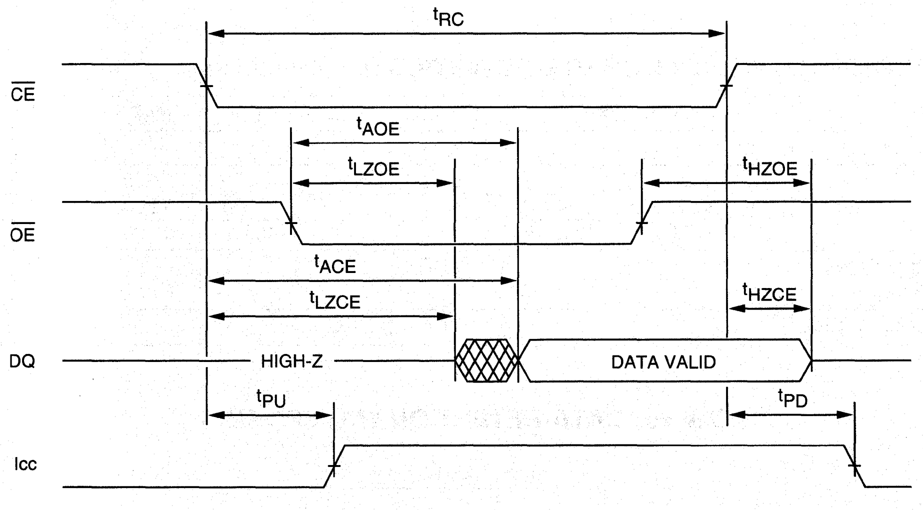
LOW Vcc DATA-RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



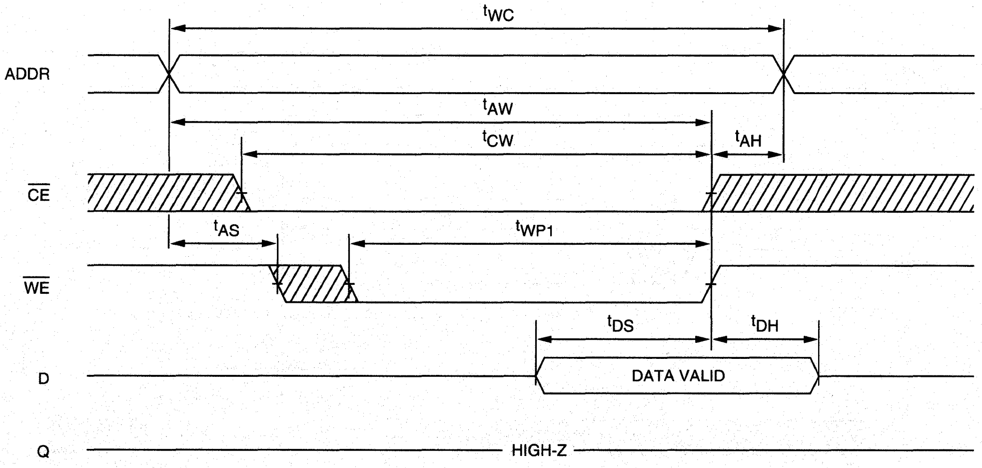
READ CYCLE NO. 2 [7, 8, 10]



▨ DON'T CARE

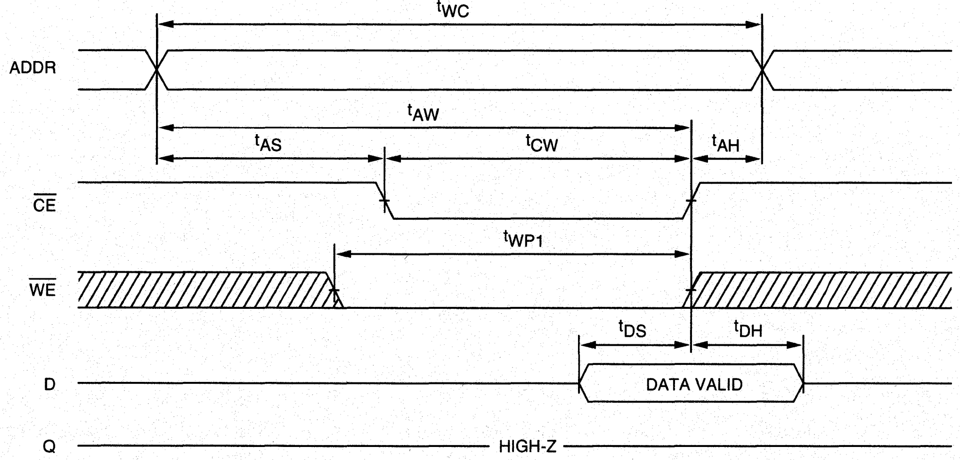
▩ UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 2
(Chip Enable Controlled)

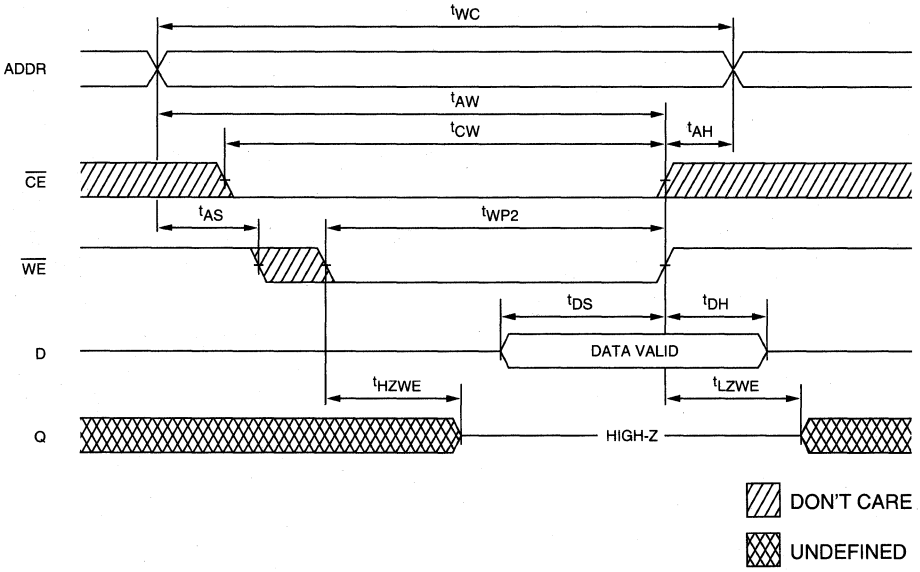


▨ DON'T CARE

▩ UNDEFINED

WRITE CYCLE NO. 3

(Write Enable Controlled) [11, 12]



CACHE DATA/LATCHED SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package		Process	Page
				PLCC	PQFP		
Dual 4K x 16 or Single 8K x 16	Mode, Byte Select, CE, OE Address Latch (A0-A11)	MT56C0816	20, 25, 35	52	52	CMOS	4-1
Dual 4K x 16 or Single 8K x 16	Mode, Byte Select, CE, OE Address Latch (A0-A12)	MT56C3816	20, 25, 35	52	52	CMOS	4-13
16K x 16	Latched Address and Data, Dual Chip Enables, Byte Write Controls	MT5C2516	15, 17, 20, 25	52	52	CMOS	4-25
Dual 4K x 18 or Single 8K x 18	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Address Latch (A0-A11)	MT56C0818	20, 25, 35	52	52	CMOS	4-39
Dual 4K x 18 or Single 8K x 18	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Synchronous Write Enable	MT56C2818	24, 28	52	52	CMOS	4-51
Dual 4K x 18 or Single 8K x 18	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Address Latch (A0-A12)	MT56C3818	20, 25, 35	52	52	CMOS	4-61
16K x 18	Latched Address and Data, Dual Chip Enables, Byte Write Controls	MT5C2818	15, 17, 20, 25	52	52	CMOS	4-73

NOTE: Many Micron components are available in bare die form. Contact Micron Technology, Inc., for more information.

CACHE DATA SRAM

DUAL 4K x 16 SRAM, SINGLE 8K x 16 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

- Operates as two 4K x 16 SRAMs with common addresses and data; also configurable as a single 8K x 16 SRAM
- Built-in input address latches
- Separate upper and lower Byte Select
- Fast access times: 20, 25 and 35ns allow operation with 40, 33 and 25 MHz microprocessor systems
- Fast Output Enable: 8ns
- Directly interfaces with the Intel 82385 cache controller as well as other 80386 cache memory controllers

OPTIONS	MARKING
• Timing	
20ns access (40 MHz)	-20
25ns access (33 MHz)	-25
35ns access (25 MHz)	-35
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

GENERAL DESCRIPTION

The MT56C0816 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

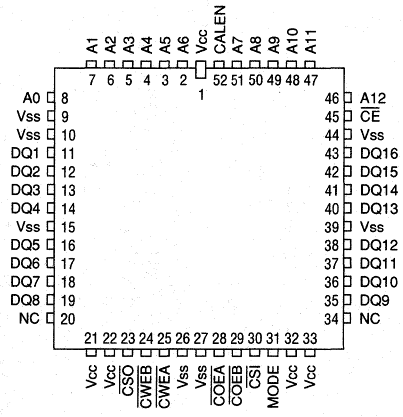
The MT56C0816 is a highly integrated cache data memory building block. It easily interfaces with cache controllers for the Intel 80386 in either the DIRECT MAPPED or TWO-WAY SET ASSOCIATIVE MODE. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 16-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 16-bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{\text{CE}}$, $\overline{\text{CS0}}$ and $\overline{\text{CS1}}$), output enable ($\overline{\text{COEA}}$ and $\overline{\text{COEB}}$) and write enable ($\overline{\text{CWEA}}$ and $\overline{\text{CWEB}}$) signals.

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-4)



In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{\text{CE}}$ is a global chip enable, while $\overline{\text{CS0}}$ and $\overline{\text{CS1}}$ control lower and upper byte selection for READ and WRITE operations.

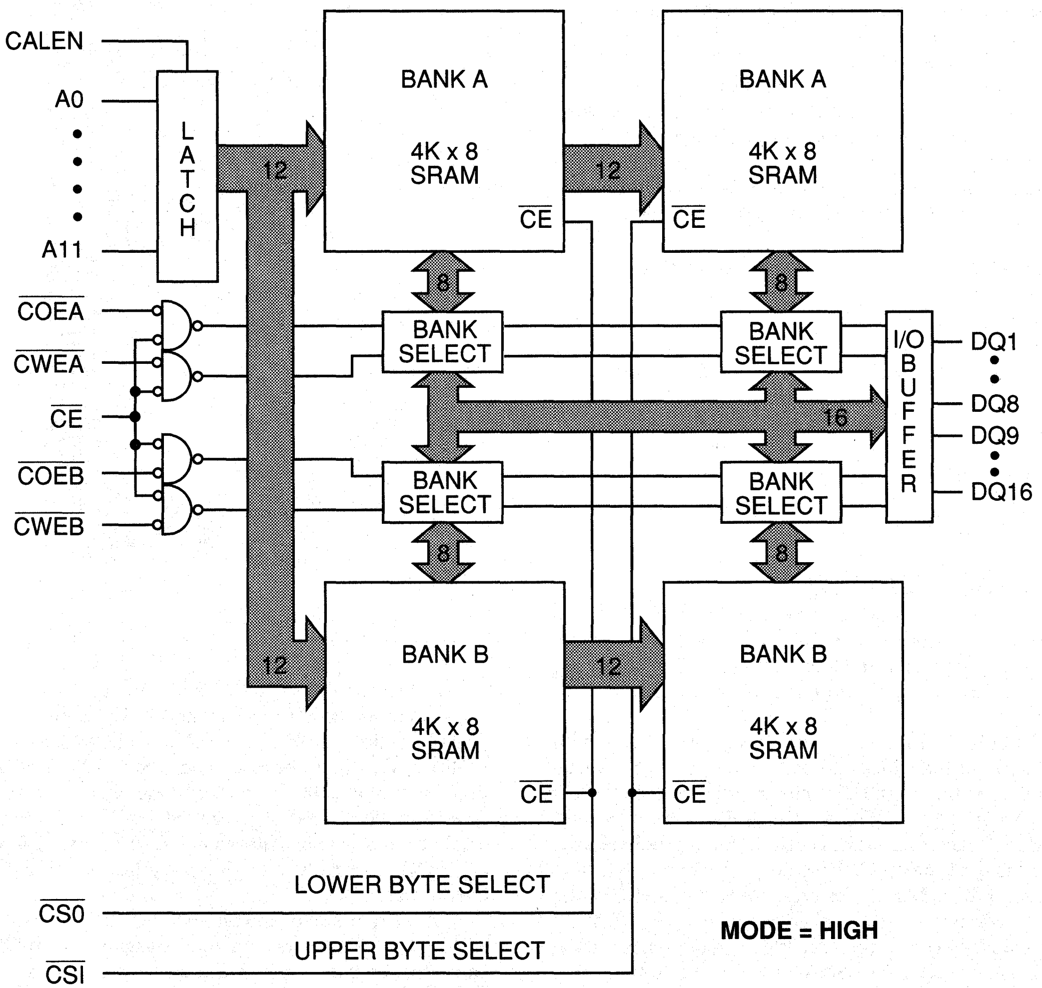
Outputs are enabled on a HIGH to LOW transition of $\overline{\text{COEA}}$ or $\overline{\text{COEB}}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{\text{COEA}}$ and $\overline{\text{COEB}}$ should be connected together externally and used as a single output enable. Alternately, $\overline{\text{COEA}}$ or $\overline{\text{COEB}}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH to LOW transition of $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{\text{CWEA}}$ and $\overline{\text{CWEB}}$ should be connected together externally and used as a single write enable. Alternately, $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C0816 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM

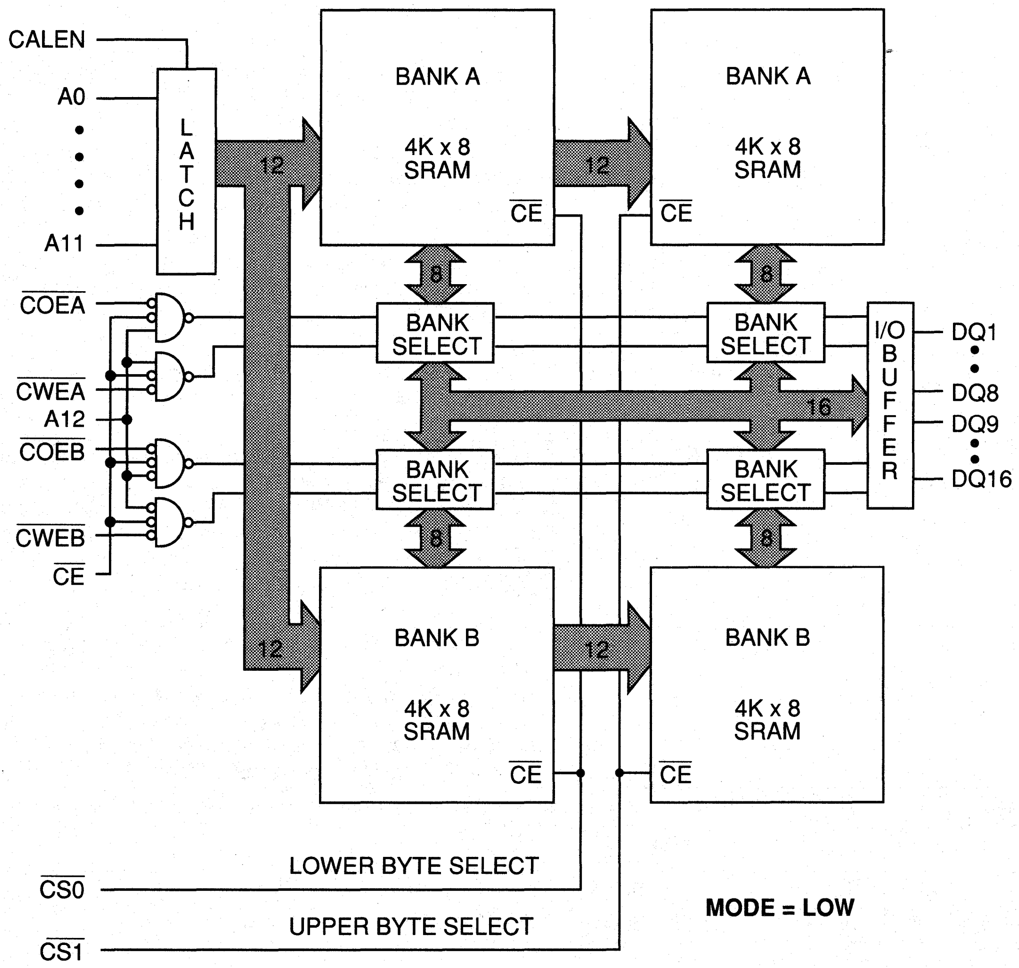
DUAL 4K x 16
(TWO-WAY SET ASSOCIATIVE)



MODE = HIGH

FUNCTIONAL BLOCK DIAGRAM

8K x 16
(DIRECT MAP)



MODE = LOW

PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K x 16 configuration. It is not used in the dual 4K x 16 configuration.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A11).
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 16 configuration. When the pin is tied LOW, the device is configured as an 8K x 16 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 are enabled.
45	$\overline{CE}$	Input	Chip Enable: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	Output Enable: In the dual configuration, the signal that is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the DIRECT mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the output.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	Write Enable: In the dual configuration, the signal that is LOW enables a data WRITE to the addressed memory location. In the DIRECT mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ±5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 16 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1-DQ8 bank A	L	L	H	L	H	H	H
READ DQ1-DQ8 bank B	L	L	H	H	L	H	H
READ DQ9-DQ16 bank A	L	H	L	L	H	H	H
READ DQ9- DQ16 bank B	L	H	L	H	L	H	H
READ DQ1- DQ16 bank A	L	L	L	L	H	H	H
READ DQ1- DQ16 bank B	L	L	L	H	L	H	H
WRITE DQ1-DQ8 bank A	L	L	H	X	X	L	H
WRITE DQ1-DQ8 bank B	L	L	H	X	X	H	L
WRITE DQ9-DQ16 bank A	L	H	L	X	X	L	H
WRITE DQ9-DQ16 bank B	L	H	L	X	X	H	L
WRITE DQ1-DQ16 bank A	L	L	L	X	X	L	H
WRITE DQ1-DQ16 bank B	L	L	L	X	X	H	L
WRITE DQ1-DQ8 banks A & B	L	L	H	X	X	L	L
WRITE DQ9-DQ16 banks A & B	L	H	L	X	X	L	L
WRITE DQ1-DQ16 banks A & B	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ or $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

TRUTH TABLE

8K x 16 (MODE PIN = LOW)

OPERATION	$\overline{\text{CE}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	$\overline{\text{COEA}}$	$\overline{\text{COEB}}$	$\overline{\text{CWEA}}$	$\overline{\text{CWEB}}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1-DQ8	L	L	H	L	L	H	H
READ DQ9-DQ16	L	H	L	L	L	H	H
READ DQ1-DQ16	L	L	L	L	L	H	H
WRITE DQ1-DQ8	L	L	H	X	X	L	L
WRITE DQ9-DQ16	L	H	L	X	X	L	L
WRITE DQ1-DQ16	L	L	L	X	X	L	L

NOTE:

1. $\overline{\text{CE}}$, when taken inactive while $\overline{\text{CWEA}}$ and $\overline{\text{CWEB}}$ remain active, allows a chip-enable-controlled WRITE to be performed.
2. $\overline{\text{COEA}}$ and $\overline{\text{COEB}}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{\text{CWEA}}$ and $\overline{\text{CWEB}}$ must both be LOW to enable a WRITE cycle. Either $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ....-1.0V to +7.0V
Storage Temperature ....-55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$; V_{CC} = 5V ±5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		V_{CC}	4.75	5.25	V	
Input High Voltage		V_{IH}	2.2	V_{CC} +0.3	V	1
Input Low Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	V_{IN} = GND to V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	$V_{I/O}$ = GND to V_{CC} Output(s) Disabled	I_{LO}	-5	5	µA	
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty Cycle V_{IN} = GND to V_{CC}	I_{CC1}	120	220	mA	
Power Supply Current: Average Operating Current	50% Duty Cycle V_{IN} = GND to V_{CC}	I_{CC2}	65	120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0} = \overline{CS1} \geq V_{CC} - 0.2V$ V_{CC} = MAX $V_{IL} \leq V_{SS} + 0.2V$ $V_{IH} \geq V_{CC} - 0.2V$	I_{SB}	20	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_{IN}	6	pF	3
Output Capacitance		$C_{I/O}$	6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient	Still Air	θ_{JA}	100	°C/W	
Thermal resistance – Junction to Case		θ_{JC}	45	°C/W	
Maximum Case Temperature		T_C	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$; Vcc = 5V ±5%)

DESCRIPTION		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^{t}RC	20		25		35		ns	4, 5
Address access time (A0-A11)	^{t}AA		20		25		35	ns	
A12 address access time	^{t}A12A		15		17		25	ns	
Chip Enable access time	^{t}ACE		20		20		25	ns	
Chip Select access time	^{t}ACS		20		25		35	ns	
Output Enable access time	^{t}AOE		8		10		13	ns	
Output hold from address change	^{t}OH	3		3		3		ns	
Chip Select to output Low-Z	^{t}LZCS	3		3		3		ns	
Output Enable to output Low-Z	^{t}LZOE	2		2		2		ns	
Chip deselect to output High-Z	^{t}HZCS		15		15		25	ns	6
Output disable to output High-Z	^{t}HZOE		10		10		14	ns	6
Address Latch Enable pulse width	^{t}CALEN	8		8		10		ns	
Address setup to latch LOW	^{t}ASL	4		4		6		ns	
Address hold from latch LOW	^{t}AHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	^{t}WC	20		25		35		ns	
Address valid to end of write	^{t}AW	15		18		25		ns	
A12 address valid to end of write	^{t}A12W	15		18		25		ns	
Chip Select to end of write	^{t}CW	15		18		25		ns	
Data valid to end of write	^{t}DW	10		10		10		ns	
Data hold from end of write	^{t}DH	0		0		0		ns	
Write Enable output in High-Z	^{t}HZWE		12		15		15	ns	6
Write disable to output in Low-Z	^{t}LZWE	3		3		3		ns	
WRITE pulse width	^{t}WP	15		18		25		ns	
$\overline{\text{CE}}$ pulse width (during Chip Enable controlled write)	^{t}CP	15		18		25		ns	
Address setup time	^{t}AS	0		0		0		ns	
WRITE recovery time	^{t}WR	0		0		0		ns	
Address Latch Enable pulse width	^{t}CALEN	8		8		10		ns	
Address setup to latch LOW	^{t}ASL	4		4		6		ns	
Address hold from latch LOW	^{t}AHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

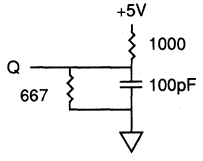


Fig. 1 OUTPUT LOAD EQUIVALENT

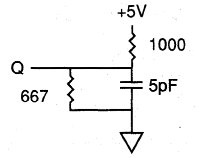
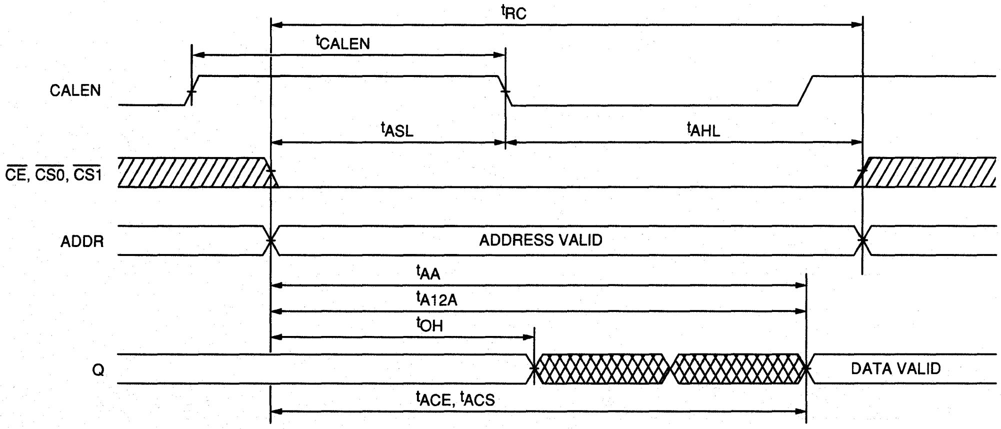


Fig. 2 OUTPUT LOAD EQUIVALENT

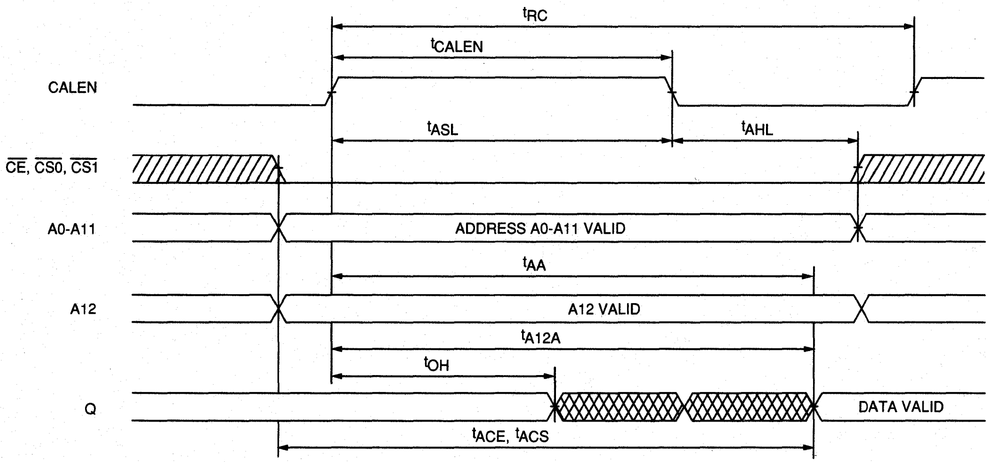
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{\text{CWE}}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. ^{t}HZCS, ^{t}HZOE, and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.

READ CYCLE NO. 1
(Address Controlled)
$\overline{\text{CWEA}} = \overline{\text{CWEB}} = V_{IH}$; $\overline{\text{COEA}}$ and/or $\overline{\text{COEB}} = V_{IL}$



READ CYCLE NO. 2
(CALEN Controlled)
$\overline{\text{CWEA}} = \overline{\text{CWEB}} = V_{IH}$; $\overline{\text{COEA}}$ and/or $\overline{\text{COEB}} = V_{IL}$

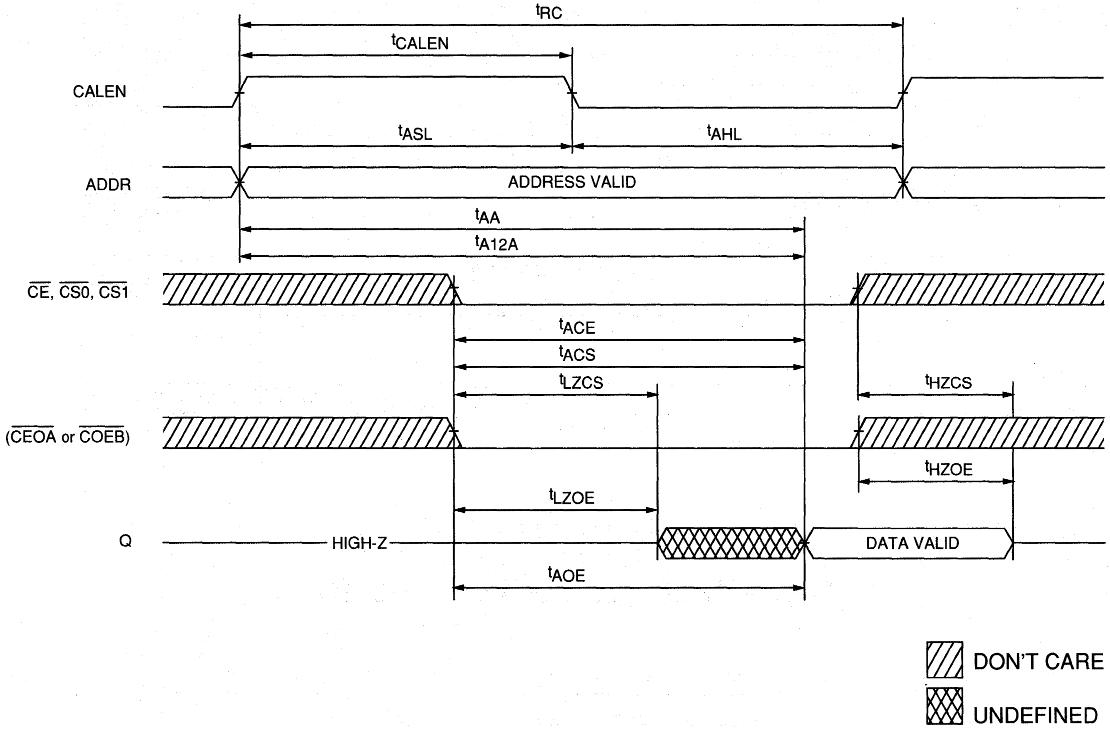


▨ DON'T CARE

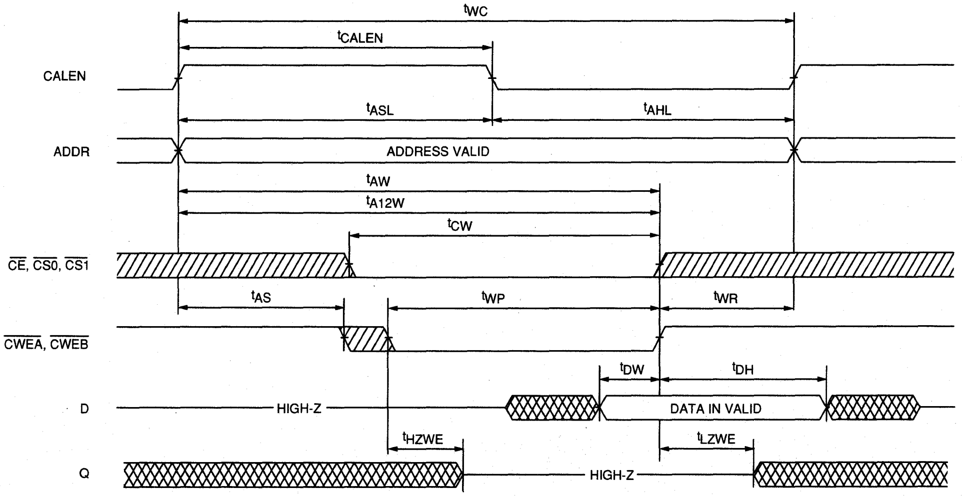
▩ UNDEFINED

READ CYCLE NO. 3

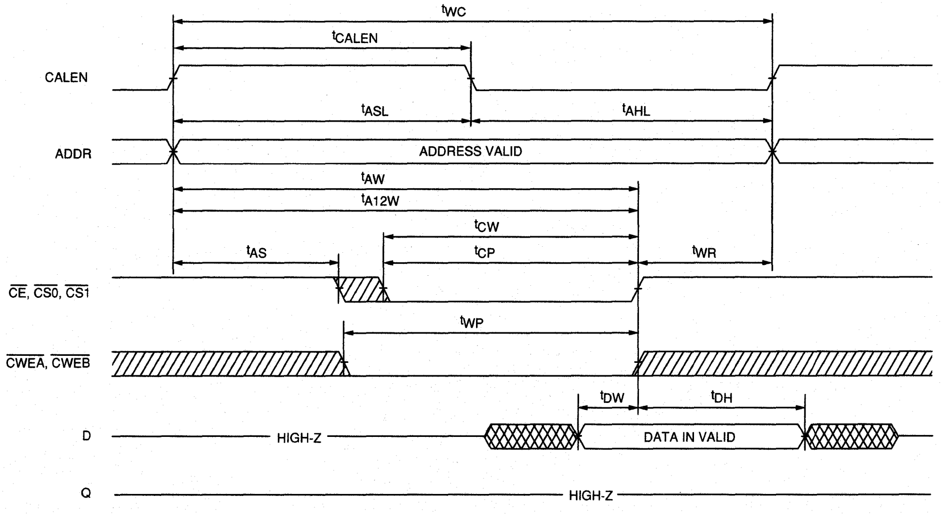
$\overline{CWEA} = \overline{CWEB} = V_{IH}$



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



▨ DON'T CARE

▩ UNDEFINED

CACHE DATA SRAM

DUAL 4K x 16 SRAM, SINGLE 8K x 16 SRAM

CONFIGURABLE CACHE DATA SRAM

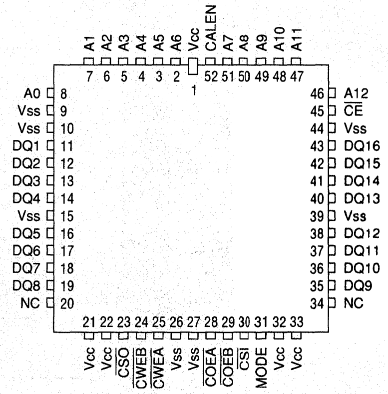
FEATURES

- Operates as two 4K x 16 SRAMs with common addresses and data; also configurable as a single 8K x 16 SRAM
- Built-in input address latches (A0-A12)
- Separate upper and lower Byte Select
- Fast access times: 20, 25 and 35ns allow operation with 40, 33 and 25 MHz microprocessor systems
- Fast Output Enable: 8ns
- Directly interfaces with the Intel 82385 cache controller as well as other 80386 and 80486 cache memory controllers

OPTIONS	MARKING
• Timing	
20ns access (40 MHz)	-20
25ns access (33 MHz)	-25
35ns access (25 MHz)	-35
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-4)



GENERAL DESCRIPTION

The MT56C3816 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C3816 is a highly integrated cache data memory building block. It easily interfaces with cache controllers for the Intel 80386 in either the DIRECT MAPPED or TWO-WAY SET ASSOCIATIVE MODE. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 16-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 16-bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations.

Outputs are enabled on a HIGH to LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

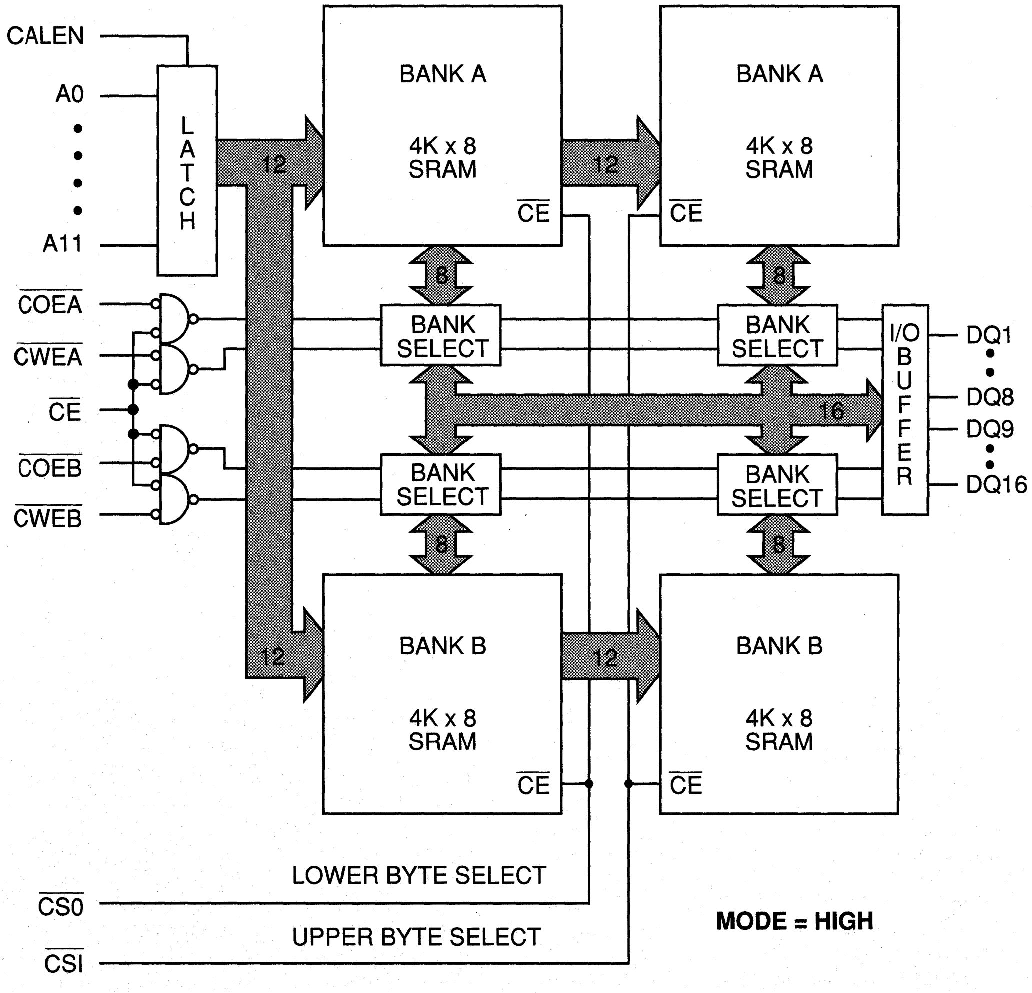
Write enable is activated on a HIGH to LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C3816 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 16

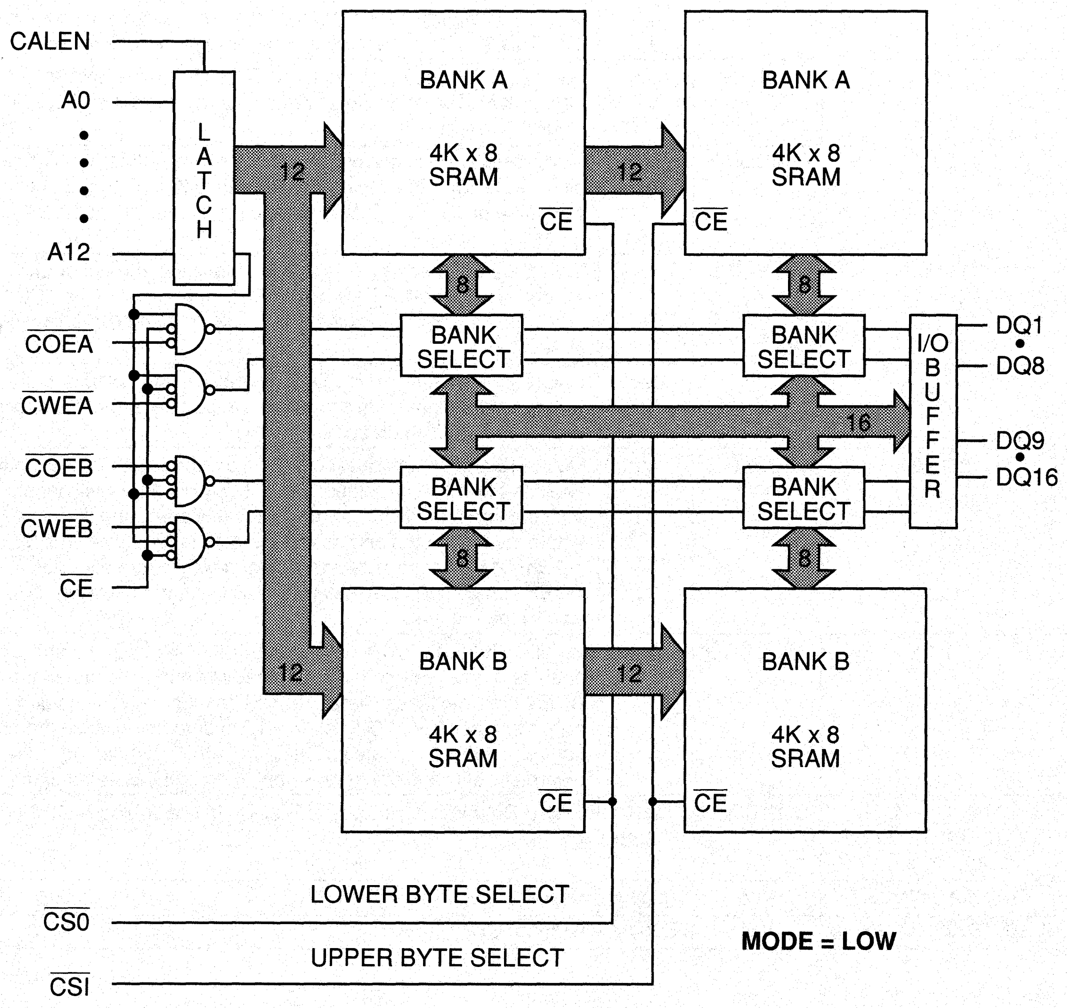
(TWO-WAY SET ASSOCIATIVE)



MODE = HIGH

FUNCTIONAL BLOCK DIAGRAM

8K x 16
(DIRECT MAP)



MODE = LOW

PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K x 16 configuration. It is not used in the dual 4K x 16 configuration. This input is latched by the negative edge of CALEN.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A12).
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 16 configuration. When the pin is tied LOW, the device is configured as an 8K x 16 SRAM.
23, 30	$\overline{\text{CS0}}$, $\overline{\text{CS1}}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{\text{CS0}}$ is LOW, DQ1-DQ8 are enabled. When $\overline{\text{CS1}}$ is LOW, DQ9-DQ16 are enabled.
45	$\overline{\text{CE}}$	Input	Chip Enable: When $\overline{\text{CE}}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{\text{COEA}}$, $\overline{\text{COEB}}$	Input	Output Enable: In the dual configuration, the signal that is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the DIRECT mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{\text{COEA}}$ or $\overline{\text{COEB}}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{\text{CWEA}}$, $\overline{\text{CWEB}}$	Input	WRITE ENABLE: In the dual configuration, the signal that is LOW enables a data write to the addressed memory location. In the DIRECT mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$ can be tied LOW externally, allowing the other signal to control the write function.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ±5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 16 (MODE PIN = HIGH)

OPERATION	$\overline{\text{CE}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	$\overline{\text{COEA}}$	$\overline{\text{COEB}}$	$\overline{\text{CWEA}}$	$\overline{\text{CWEB}}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1-DQ8 bank A	L	L	H	L	H	H	H
READ DQ1-DQ8 bank B	L	L	H	H	L	H	H
READ DQ9-DQ16 bank A	L	H	L	L	H	H	H
READ DQ9-DQ16 bank B	L	H	L	H	L	H	H
READ DQ1-DQ16 bank A	L	L	L	L	H	H	H
READ DQ1-DQ16 bank B	L	L	L	H	L	H	H
WRITE DQ1-DQ8 bank A	L	L	H	X	X	L	H
WRITE DQ1-DQ8 bank B	L	L	H	X	X	H	L
WRITE DQ9-DQ16 bank A	L	H	L	X	X	L	H
WRITE DQ9-DQ16 bank B	L	H	L	X	X	H	L
WRITE DQ1-DQ16 bank A	L	L	L	X	X	L	H
WRITE DQ1-DQ16 bank B	L	L	L	X	X	H	L
WRITE DQ1-DQ8 banks A & B	L	L	H	X	X	L	L
WRITE DQ9-DQ16 banks A & B	L	H	L	X	X	L	L
WRITE DQ1-DQ16 banks A & B	L	L	L	X	X	L	L

NOTE: $\overline{\text{CE}}$, when taken inactive while $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$ remain active, allows a chip-enable-controlled WRITE to be performed.

TRUTH TABLE

8K x 16 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1-DQ8	L	L	H	L	L	H	H
READ DQ9-DQ16	L	H	L	L	L	H	H
READ DQ1-DQ16	L	L	L	L	L	H	H
WRITE DQ1-DQ8	L	L	H	X	X	L	L
WRITE DQ9-DQ16	L	H	L	X	X	L	L
WRITE DQ1-DQ16	L	L	L	X	X	L	L

NOTE:

1. $\overline{CE}$, when taken inactive while $\overline{CWEA}$ and $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.
2. $\overline{COEA}$ and $\overline{COEB}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{CWEA}$ and $\overline{CWEB}$ must both be LOW to enable a WRITE cycle. Either $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ....-1.0V to +7.0V
Storage Temperature ....-55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		Vcc	4.75	5.25	V	
Input High Voltage		VIH	2.2	Vcc+0.3	V	1
Input Low Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	VIN = GND to Vcc	ILI	-5	5	µA	
Output Leakage Current	VI/O = GND to Vcc Output(s) Disabled	ILO	-5	5	µA	
Output Low Voltage	IOL = 4.0mA	VOL		0.4	V	1
Output High Voltage	IOH = -1.0mA	VOH	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty cycle VIN = GND to Vcc	ICC1	120	220	mA	
Power Supply Current: Average Operating Current	50% Duty cycle VIN = GND to Vcc	ICC2	65	120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0} = \overline{CS1} \ge$ Vcc -0.2V Vcc = MAX VIL ≤ Vss +0.2V VIH ≥ Vcc -0.2V	ISB	20	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	CIN	6	pF	3
Output Capacitance		CI/O	6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient	Still Air	θJA	100	°C/W	
Thermal resistance – Junction to Case		θJC	45	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$; Vcc = 5V ±5%)

DESCRIPTION		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^{t}RC	20		25		35		ns	4, 5
Address access time (A0-A12)	^{t}AA		20		25		35	ns	
Chip Enable access time	^{t}ACE		20		20		25	ns	
Chip Select access time	^{t}ACS		20		25		35	ns	
Output Enable access time	^{t}AOE		8		10		13	ns	
Output hold from address change	^{t}OH	3		3		3		ns	
Chip Select to output Low-Z	^{t}LZCS	3		3		3		ns	
Output Enable to output Low-Z	^{t}LZOE	2		2		2		ns	
Chip deselect to output High-Z	^{t}HZCS		15		15		25	ns	6
Output disable to output High-Z	^{t}HZOE		10		10		14	ns	6
Address Latch Enable pulse width	^{t}CALEN	8		8		10		ns	
Address setup to latch LOW	^{t}ASL	4		4		6		ns	
Address hold from latch LOW	^{t}AHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	^{t}WC	20		25		35		ns	
Address valid to end of write	^{t}AW	15		18		25		ns	
Chip Select to end of write	^{t}CW	15		18		25		ns	
Data valid to end of write	^{t}DW	10		10		10		ns	
Data hold from end of write	^{t}DH	0		0		0		ns	
Write Enable output in High-Z	^{t}HZWE		12		15		15	ns	6
Write disable to output in Low-Z	^{t}LZWE	3		3		3		ns	
WRITE pulse width	^{t}WP	15		18		25		ns	
$\overline{\text{CE}}$ pulse width (during Chip Enable controlled write)	^{t}CP	15		18		25		ns	
Address setup time	^{t}AS	0		0		0		ns	
WRITE recovery time	^{t}WR	0		0		0		ns	
Address Latch Enable pulse width	^{t}CALEN	8		8		10		ns	
Address setup to latch LOW	^{t}ASL	4		4		6		ns	
Address hold from latch LOW	^{t}AHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels .... Vss to 3.0V
Input rise and fall times 3ns
Input timing reference levels 1.5V
Output reference levels 1.5V
Output load .... See Figures 1 and 2

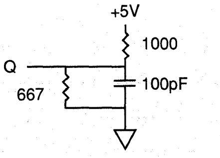


Fig. 1 OUTPUT LOAD EQUIVALENT

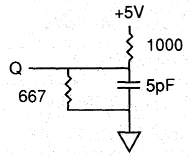


Fig. 2 OUTPUT LOAD EQUIVALENT

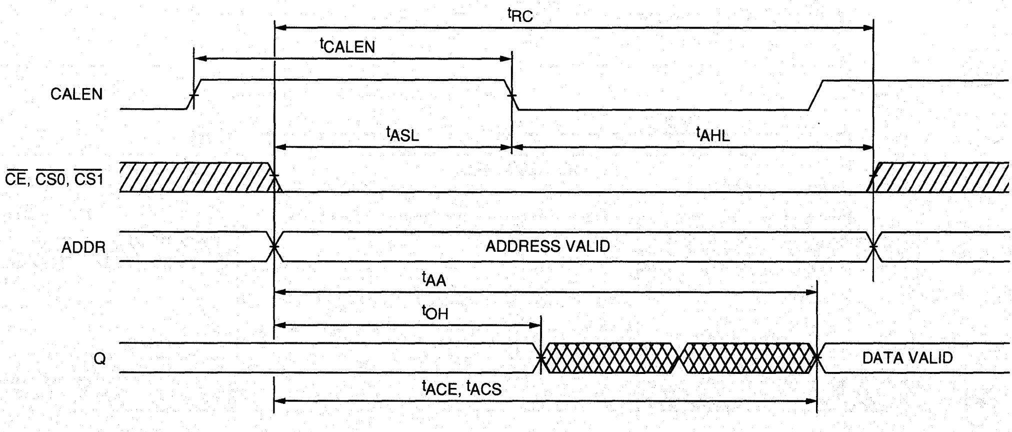
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{\text{CWE}}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. ^{t}HZCS, ^{t}HZOE, and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.

READ CYCLE NO. 1

(Address Controlled)

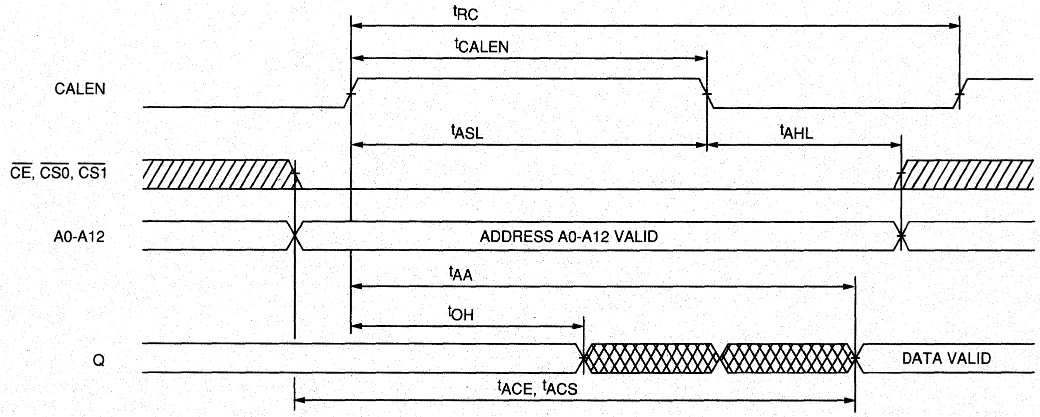
$\overline{\text{CWEA}} = \overline{\text{CWEB}} = V_{IH}$; $\overline{\text{COEA}}$ and/or $\overline{\text{COEB}} = V_{IL}$



READ CYCLE NO. 2

(CALEN Controlled)

$\overline{\text{CWEA}} = \overline{\text{CWEB}} = V_{IH}$; $\overline{\text{COEA}}$ and/or $\overline{\text{COEB}} = V_{IL}$

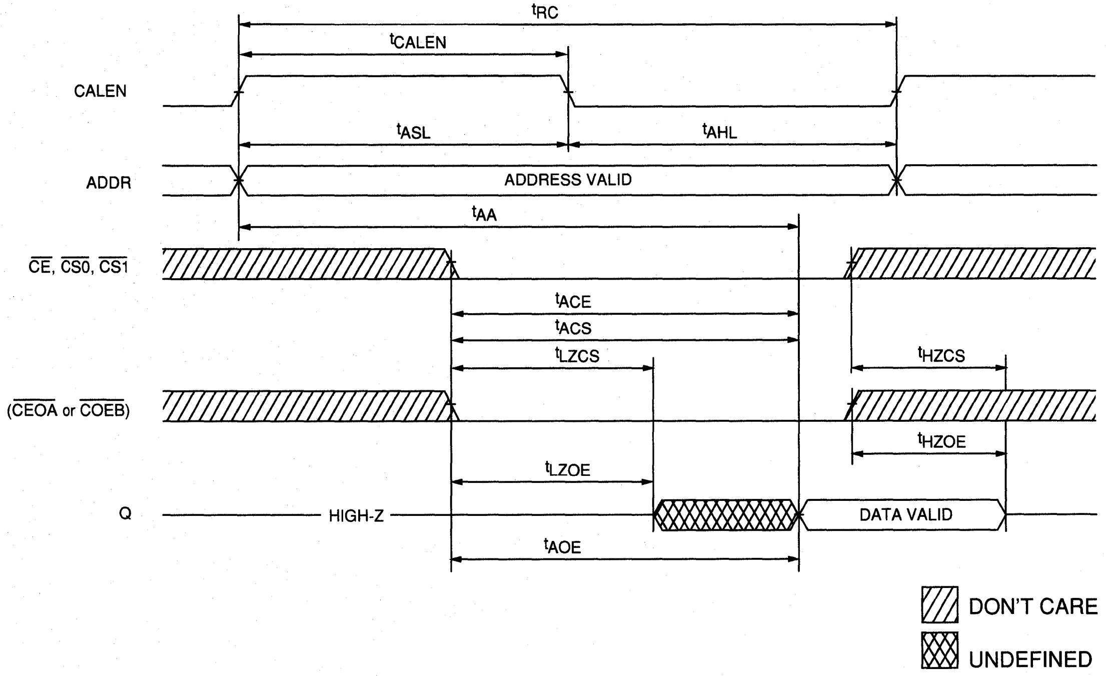


▨ DON'T CARE

▩ UNDEFINED

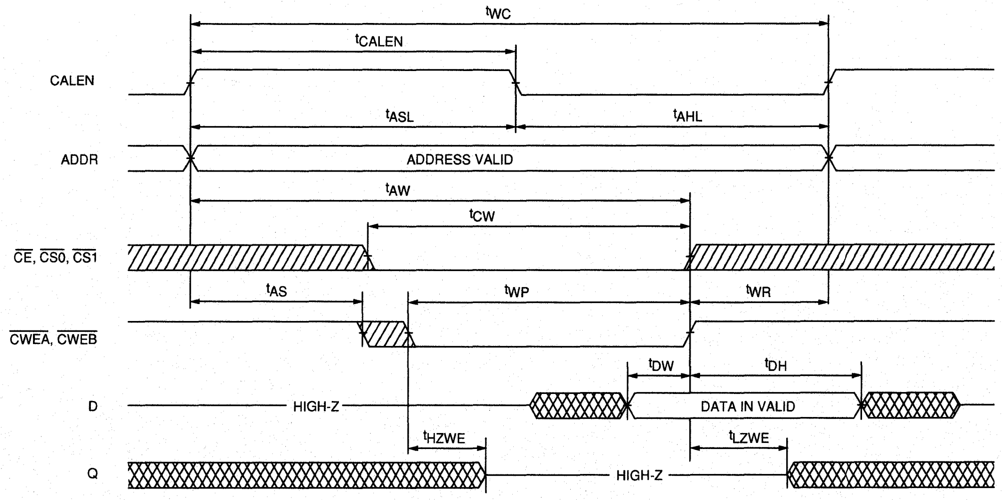
READ CYCLE NO. 3

$\overline{\text{CWEA}} = \overline{\text{CWEB}} = V_{IH}$



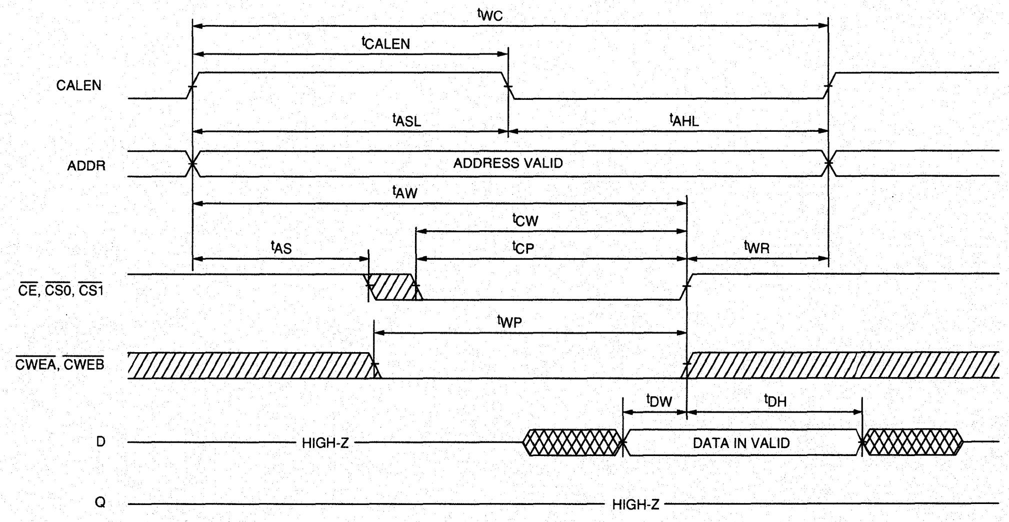
WRITE CYCLE NO. 1

(Write Enable Controlled)



WRITE CYCLE NO. 2

(Chip Select Controlled)



▨ DON'T CARE

▩ UNDEFINED

LATCHED SRAM

16K x 16 SRAM

WITH ADDRESS/ DATA INPUT LATCHES

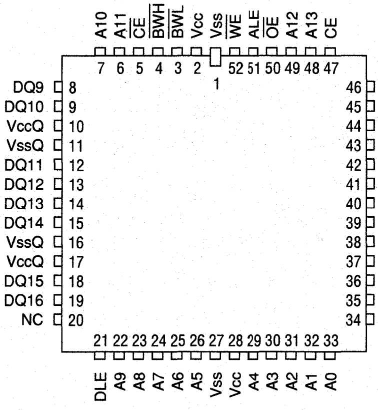
FEATURES

- Fast access times: 15, 17, 20 and 25ns
- Fast Output Enable: 6, 8 and 10ns
- Single +5V ±10% power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Optional +3.3V ±10% output buffer operation
- Separate data input latch
- Common data inputs and data outputs
- BYTE WRITE capability via dual write strobes
- Address and Chip Enable input latches

OPTIONS	MARKING
• Timing	
15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG
• Density	
16K x 16	MT5C2516

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT5C2516 SRAM integrates a 16K x 16 SRAM core with advanced peripheral circuitry consisting of address and data input latches, latched active HIGH and active LOW chip enables, separate upper and lower byte write strobes and a fast output enable. The device is ideally suited for "pipelined" systems and systems that benefit from a wide data bus.

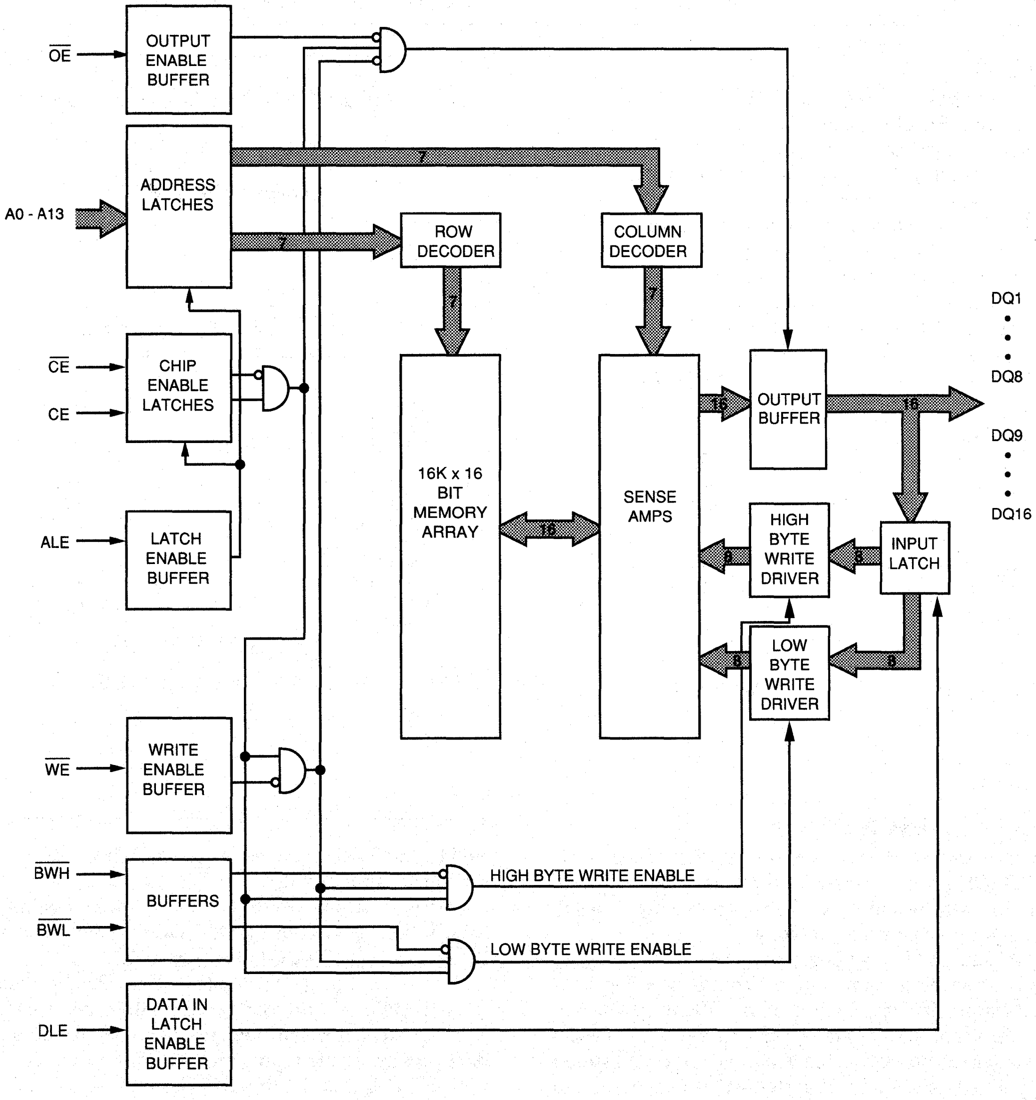
Address and chip enable latches are provided. When address latch enable (ALE) is HIGH, the address and chip enable latches are transparent, allowing the input to flow through the latch. If ALE is LOW, the address and chip enable latch inputs are disabled. This input latch simplifies READ and WRITE cycles by guaranteeing address hold time in a simple fashion.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) allow individual bytes to be written. $\overline{BWL}$ controls DQ1-DQ8 the lower bits. While $\overline{BWH}$ controls DQ9-DQ16 the upper bits.

A data input latch is provided. When data latch enable (DLE) is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present on the inputs are held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT5C2516 operates from a +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided to allow either +3.3V or +5V TTL operation of the output drivers.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC and PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are either latched or unlatched depending on the state of ALE.
52	$\overline{\text{WE}}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{\text{WE}}$ is LOW for a WRITE cycle and HIGH for a READ cycle
51	ALE	Input	Address Latch Enable: This signal latches the address, CE, and $\overline{\text{CE}}$ inputs on its falling edge. When ALE is HIGH, the latch is transparent.
3, 4	$\overline{\text{BWL}}$, $\overline{\text{BWH}}$	Input	Byte Write Enables: These active LOW inputs allow individual bytes to be written. When $\overline{\text{BWL}}$ is LOW, data is written to the lower byte, D1-D8. When $\overline{\text{BWH}}$ is LOW, data is written to the upper byte, D9-D16. When both $\overline{\text{BWH}}$ and $\overline{\text{BWL}}$ are HIGH and meet the required setup time to the falling edge of $\overline{\text{WE}}$, then the WRITE cycle is aborted.
5, 47	$\overline{\text{CE}}$,CE	Input	Chip Enables: These signals are used to enable the device. Both active HIGH (CE) and active LOW ($\overline{\text{CE}}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual bank configuration.
50	$\overline{\text{OE}}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH, the data latch is transparent. Input data is latched into the on-chip data latch on the falling edge of DLE.
20, 46	NC	Input/ Output	Parity Data I/O: These signals are no connects (NC). No connects are not internally bonded.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. When data is latched, DQ1-DQ16 must meet the required setup and hold times around DLE.
2, 28	Vcc	Supply	Power Supply: +5V ±10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ±10% or 3.3V ±10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	CE	$\overline{CE}$	$\overline{WE}$	$\overline{BWL}$	$\overline{BWH}$	ALE	DLE	$\overline{OE}$	DQ
Deselected cycle	L	X	X	X	X	X	X	X	High-Z
Deselected	X	H	X	X	X	X	X	X	High-Z
READ	H	L	H	X	X	H	X	H	High-Z
READ	H	L	H	X	X	H	X	L	Q1-Q16
LATCHED READ	H	L	H	X	X	L	X	L	Q1-Q16
WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	H	H	X	D1-D16
LATCHED WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	L	H	X	D1-D16
WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	H	L	X	D1-D16
LATCHED WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	L	L	X	D1-D16
ABORTED WRITE	H	L	L	H	H	X	X	X	High-Z
BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	H	H	X	D1-D8
LATCHED BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	L	H	X	D1-D8
BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	H	H	X	D9-D16
LATCHED BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	L	H	X	D9-D16
BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	H	L	X	D1-D8
LATCHED BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	L	L	X	D1-D8
BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	H	L	X	D9-D16
LATCHED BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	L	L	X	D9-D16

NOTE:

1. Latched inputs (Addresses, CE and $\overline{CE}$) must satisfy the specified setup and hold times around the falling edge of ALE. Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the ^{t}DLW time.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold times for DLE.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative
to V_{SS}/V_{SSQ} .... -1.0V to +7.0V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1.5W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$; V_{CC} = 5V ±10%; $V_{SS} = V_{SSQ}$, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \leq V_{OUT} \leq V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1
Output Buffer Supply Voltage	5V TTL Compatible	V_{CCQ}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}$, $CE \geq V_{IH}$ V_{CC} = MAX; Outputs Open f = MAX = 1/ ^tRC	I_{CC}	150	250	mA	3
Power Supply Current: Standby	$CE \leq V_{IL}$, $\overline{CE} \geq V_{IH}$; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{SB1}	50	80	mA	
	$\overline{CE} \geq V_{CC}$ -0.2; $CE \leq V_{SS}$ +0.2 V_{CC} = MAX; $V_{IL} \leq V_{SS}$ +0.2 $V_{IH} \geq V_{CC}$ -0.2; f = 0	I_{SB2}	5	15	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz	C_I	5	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 5V	$C_{I/O}$	9	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$; Vcc = VccQ = 5V ±10%)

		-15		-17		-20		-25			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
ADDRESS LATCH											
Latch cycle time	^{t}LC	15		17		20		25		ns	
Latch HIGH time	^{t}LEH	5		5		5		5		ns	
Address/Chip Enable setup to latch LOW	^{t}LS	2		2		2		2		ns	
Address/Chip Enable hold from latch LOW	^{t}LH	3		3		3		3		ns	
Address/Chip Enable setup to latch HIGH	^{t}LHS	0		0		0		0		ns	
Latch HIGH to output active (Low-Z)	^{t}LZL	2		2		2		2		ns	6, 7, 4
Latch HIGH to output in High-Z	^{t}HZL	2	7	2	7	2	7	2	10	ns	6, 7, 4
READ CYCLE											
READ cycle time	^{t}RC	15		17		20		25		ns	
Address access time	^{t}AA		15		17		20		25	ns	
Chip Enable access time	^{t}ACE		15		17		20		25	ns	
Output hold from address change	^{t}OH	4		4		4		4		ns	
Chip Enable to output in Low-Z	^{t}LZCE	2		2		2		2		ns	6, 7, 4
Chip disable to output in High-Z	^{t}HZCE	2	7	2	7	2	7	2	10	ns	6, 7, 4
Output Enable access time	^{t}AOE		6		7		8		10	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		ns	6, 7, 4
Output disable to output in High-Z	^{t}HZOE	2	6	2	7	2	8	2	10	ns	6, 7, 4
WRITE Cycle											
WRITE cycle time	^{t}WC	15		17		20		25		ns	
Chip Enable to end of write	^{t}CW	13		14		15		20		ns	
Address valid to end of write	^{t}AW	13		14		15		20		ns	
Address setup time	^{t}AS	0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		ns	
WRITE pulse width	^{t}WP	13		14		15		20		ns	
Data setup time	^{t}DS	6		7		8		10		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	5		5		5		5		ns	6, 7, 4
Write Enable to output in High-Z	^{t}HZWE	0	8	0	8	0	10	0	10	ns	6, 7, 4
Byte Write Enable setup time	^{t}BWS	6		7		8		10		ns	
Byte Write Enable hold time	^{t}BWH	2		2		2		2		ns	
Byte Write disable setup time	^{t}BWDS	0		0		0		0		ns	
Data setup to DLE LOW	^{t}DLS	1		1		1		1		ns	9
Data hold from DLE LOW	^{t}DLH	3		3		3		3		ns	9
DLE HIGH to end of write	^{t}DLW	6		7		8		10		ns	8
End of write to DLE HIGH	^{t}WDLH	0		0		0		0		ns	9
End of write to ALE HIGH	^{t}WLH	0		0		0		0		ns	
ALE HIGH setup time to write enable LOW	^{t}LWS	0		0		0		0		ns	
ALE HIGH to end of write	^{t}LW	13		14		15		20		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

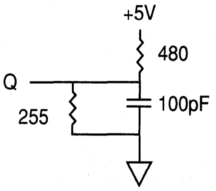


Fig. 1 OUTPUT LOAD EQUIVALENT

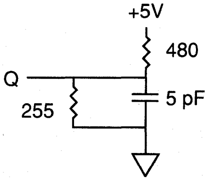
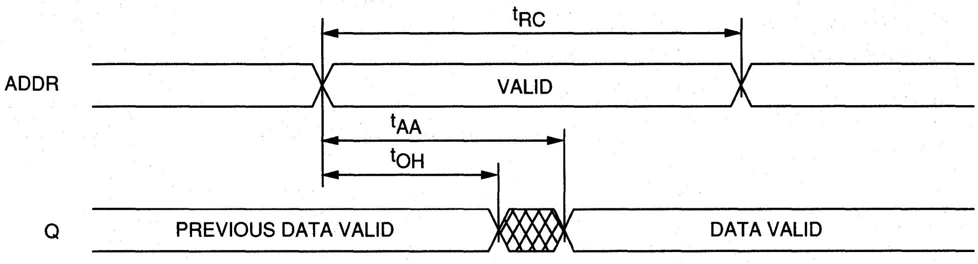


Fig. 2 OUTPUT LOAD EQUIVALENT

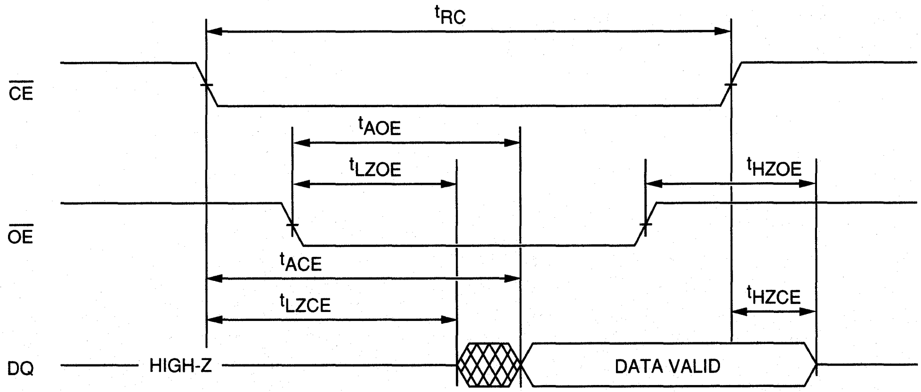
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZOE is less than ^{t}LZOE.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold time with respect to DLE.
10. Any combination of write enable ($\overline{\text{WE}}$) and chip enable ($\overline{\text{CE}}$) can initiate and terminate a WRITE cycle.
11. $\overline{\text{WE}}$ is HIGH for READ cycle.
12. Device is continuously selected. All chip enables are held in their active state.
13. Address valid prior to or coincident with the latest occurring chip enable.
14. CE timing is the same as $\overline{\text{CE}}$ timing. The wave form is inverted.
15. If output enable ($\overline{\text{OE}}$) is inactive (HIGH) the output will be in High-Z instead of undefined.

READ CYCLE NO. 1[11, 12]



READ CYCLE NO. 2[7, 11, 13, 14]

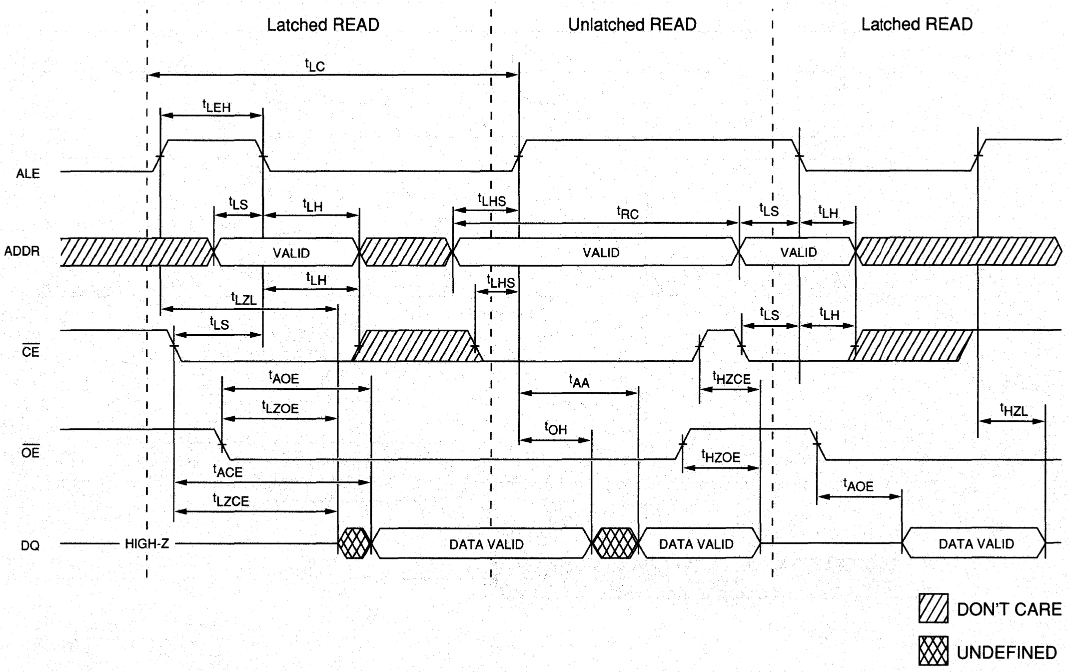


▨ DON'T CARE

▩ UNDEFINED

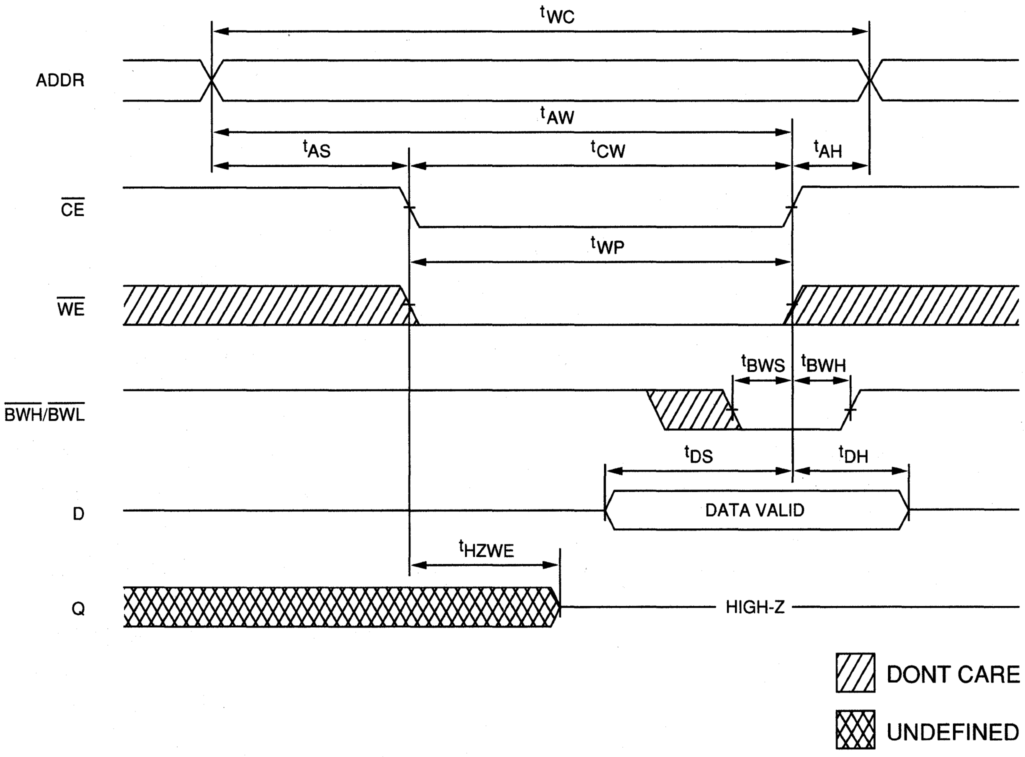
READ CYCLE NO. 3

(ALE = DLE = HIGH) [7, 11, 14]



CACHE DATA/LATCHED SRAM

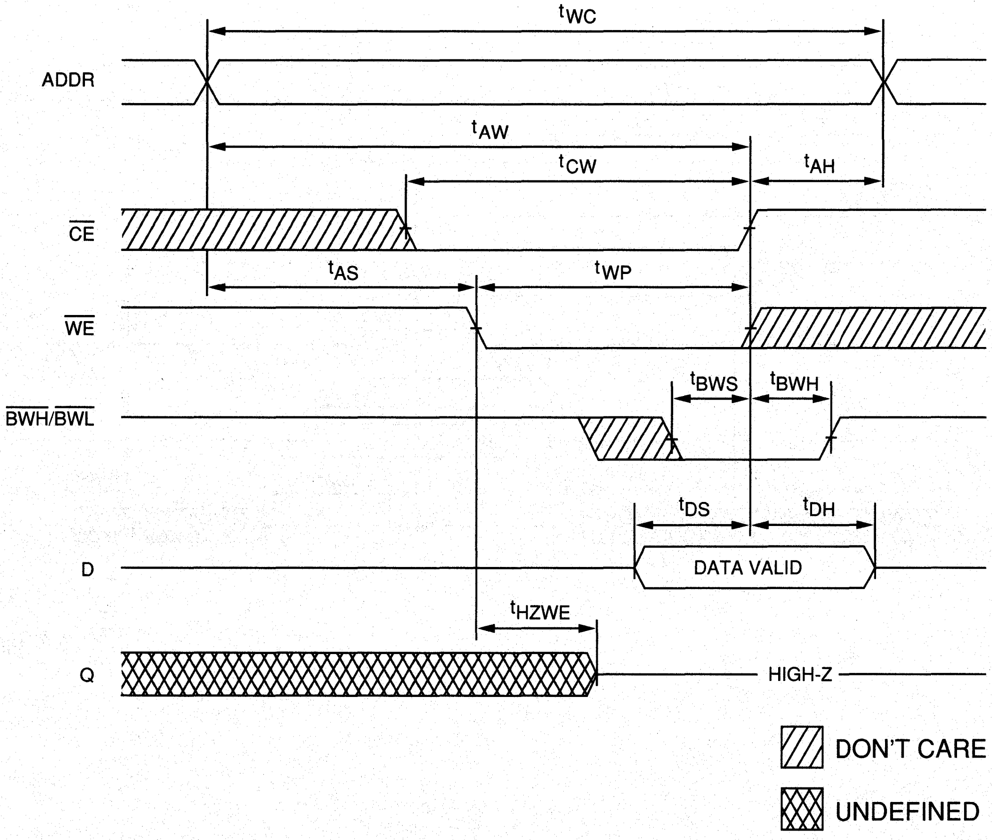
WRITE CYCLE NO. 1
Chip Enable Controlled
(ALE = DLE = HIGH)[10, 14, 15]



WRITE CYCLE NO. 2

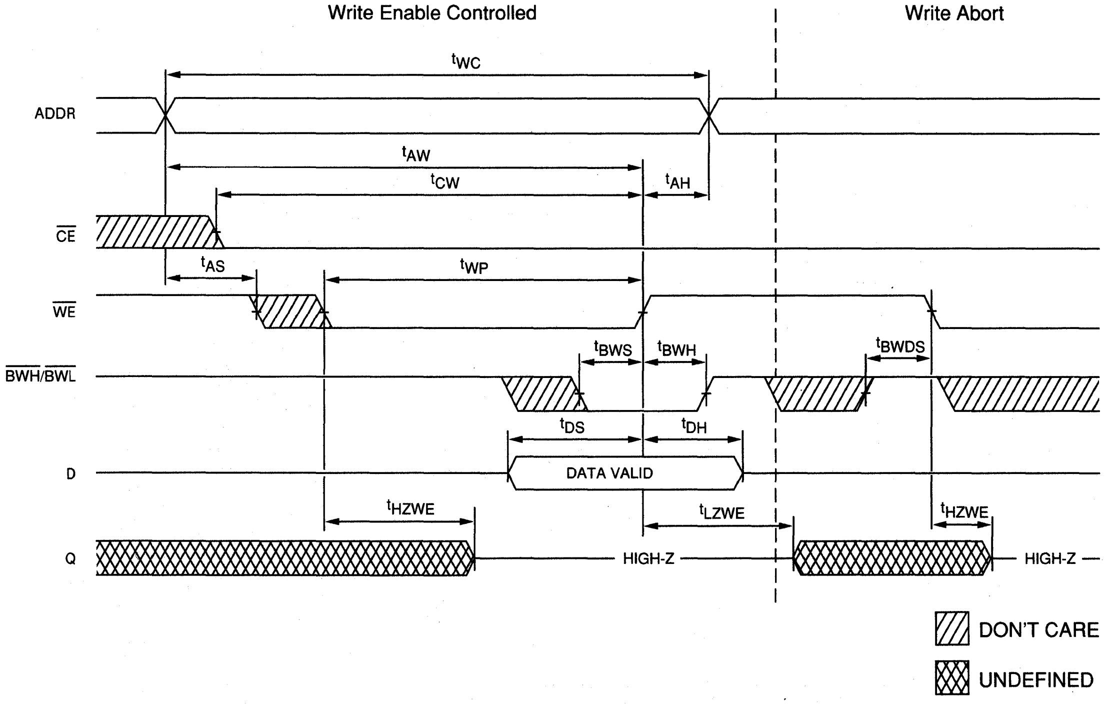
Write Enable Initiated / Chip Enable Terminated

(ALE = DLE = HIGH) [10, 14, 15]

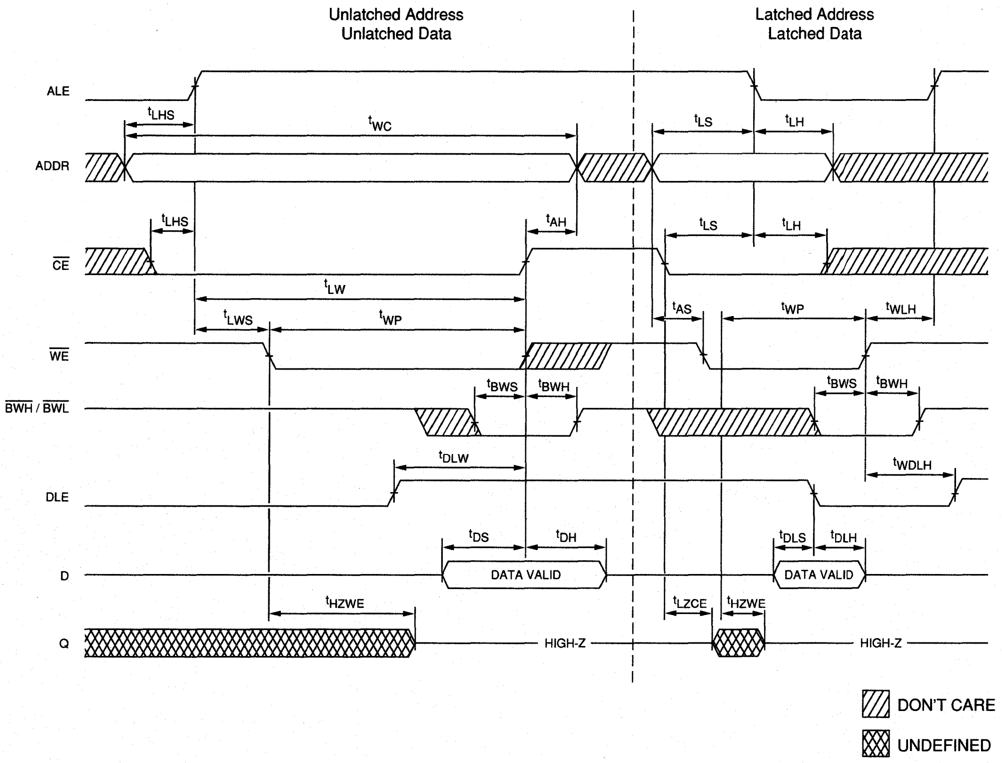


WRITE CYCLE NO. 3

(ALE = DLE = HIGH)[7, 10, 14, 15]



WRITE CYCLE NO. 4 [7, 10, 14, 15]



CACHE DATA SRAM

DUAL 4K x 18 SRAM, SINGLE 8K x 18 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

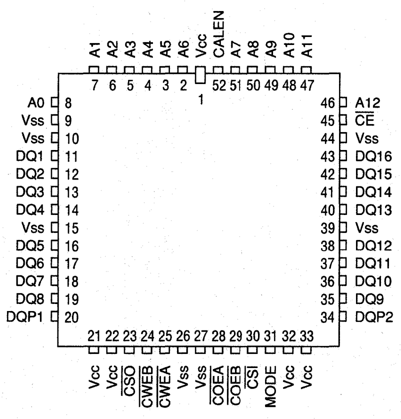
- Operates as two 4K x 18 SRAMs with common addresses and data; also configurable as a single 8K x 18 SRAM
- Built-in input address latches
- Separate upper and lower Byte Select
- Fast access times: 20ns, 25ns and 35ns allow operation with 40, 33 and 25 MHz microprocessor systems
- Fast Output Enable: 8ns
- Directly interfaces with the Intel 82385 cache controller as well as other 80386 cache memory controllers
- Parity bits provided for large cache applications such as secondary cache for the Intel 80486 microprocessors

OPTIONS

OPTIONS	MARKING
• Timing	
20ns access (40 MHz)	-20
25ns access (33 MHz)	-25
35ns access (25 MHz)	-35
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-4)



GENERAL DESCRIPTION

The MT56C0818 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C0818 is a highly integrated cache data memory building block. It easily interfaces with cache controllers for the Intel 80386 in either the DIRECT MAPPED or TWO-WAY SET ASSOCIATIVE mode. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 18-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 18-bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{\text{CE}}$, $\overline{\text{CS0}}$ and $\overline{\text{CS1}}$), output enable ($\overline{\text{COEA}}$ and $\overline{\text{COEB}}$) and write enable ($\overline{\text{CWEA}}$ and $\overline{\text{CWEB}}$) signals.

In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{\text{CE}}$ is a global chip enable, while $\overline{\text{CS0}}$ and $\overline{\text{CS1}}$ control lower and upper byte selection for READ and WRITE operations.

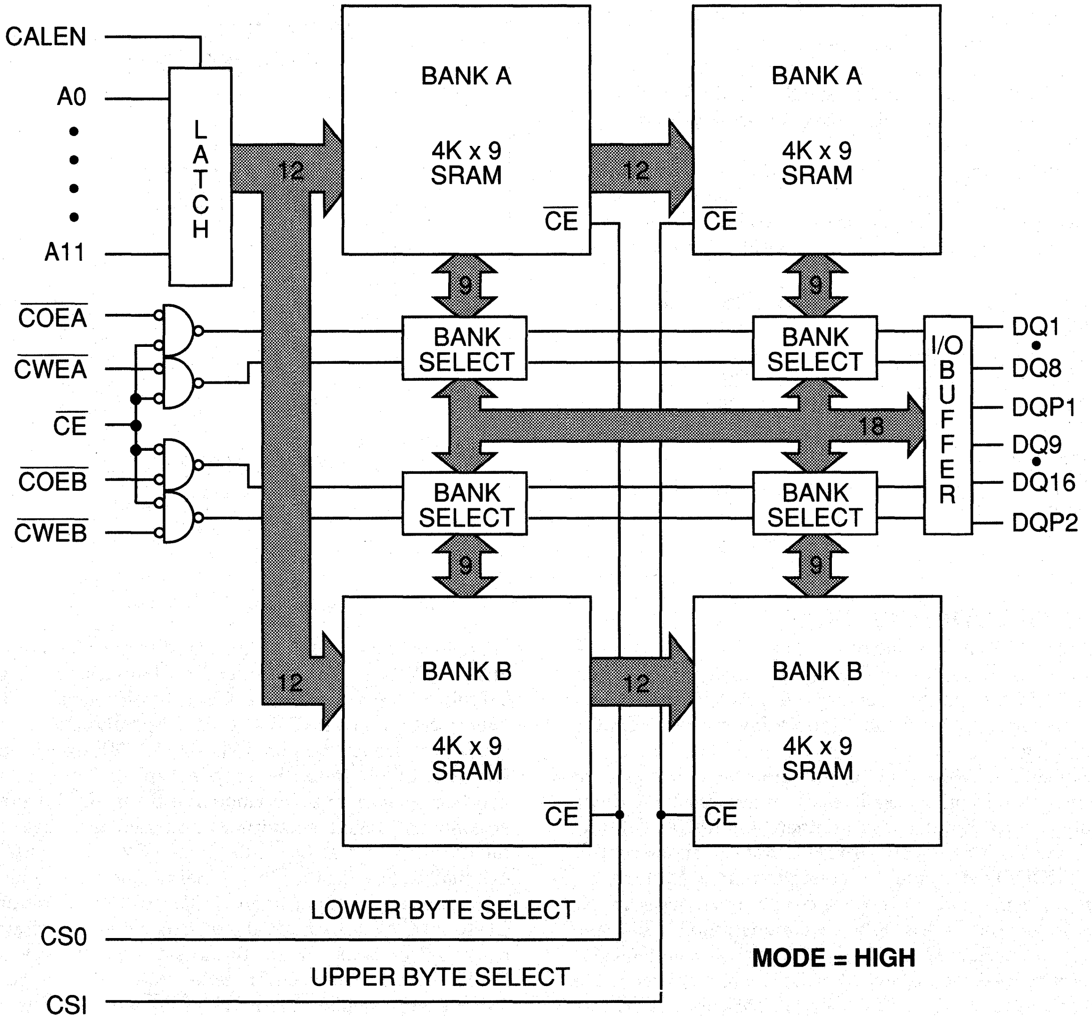
Outputs are enabled on a HIGH to LOW transition of $\overline{\text{COEA}}$ or $\overline{\text{COEB}}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{\text{COEA}}$ and $\overline{\text{COEB}}$ should be connected together externally and used as a single output enable. Alternately, $\overline{\text{COEA}}$ or $\overline{\text{COEB}}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH to LOW transition of $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{\text{CWEA}}$ and $\overline{\text{CWEB}}$ should be connected together externally and used as a single write enable. Alternately, $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C0818 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM

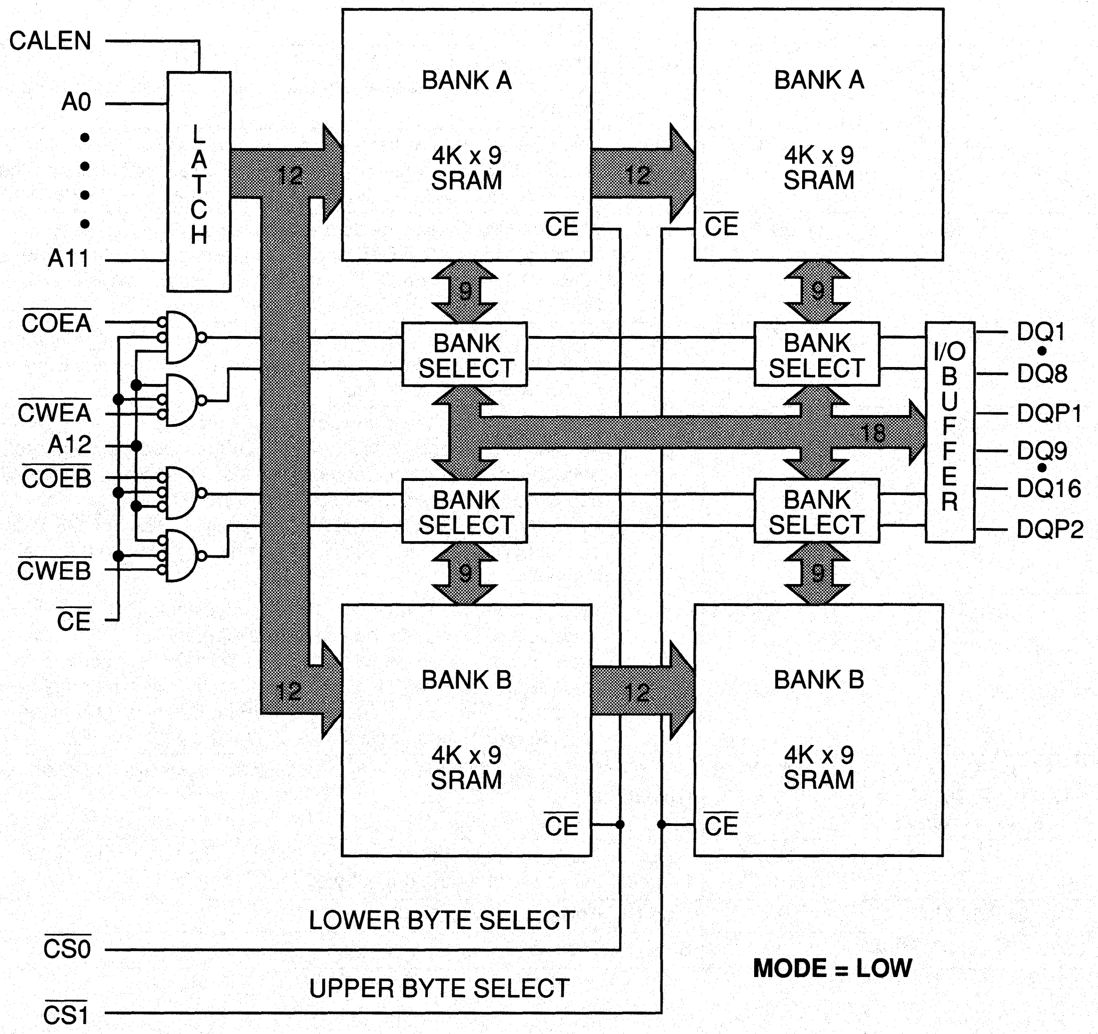
DUAL 4K x 18
(TWO-WAY SET ASSOCIATIVE)



MODE = HIGH

FUNCTIONAL BLOCK DIAGRAM

8K x 18
(DIRECT MAP)



MODE = LOW

PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K x 18 configuration. It is not used in the dual 4K x 18 configuration.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A11).
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 18 configuration. When the pin is tied LOW, the device is configured as an 8K x 18 SRAM.
23, 30	$\overline{\text{CS0}}$, $\overline{\text{CS1}}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{\text{CS0}}$ is LOW, DQ1-DQ8 and DQP1 are enabled. When $\overline{\text{CS1}}$ is LOW, DQ9-DQ16 and DQP2 are enabled.
45	$\overline{\text{CE}}$	Input	Chip Enable: When $\overline{\text{CE}}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{\text{COEA}}$, $\overline{\text{COEB}}$	Input	Output Enable: In the dual configuration the signal that is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{\text{COEA}}$ or $\overline{\text{COEB}}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{\text{CWEA}}$, $\overline{\text{CWEB}}$	Input	Write Enable: In the dual configuration the signal that is LOW enables a data write to the addressed memory location. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$ can be tied LOW externally, allowing the other signal to control the write function.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
20, 34	DQP1 DQP2	Input/ Output	Parity Data I/O: DQP1 is the parity bit for the lower byte. DQP2 is the parity bit for the upper byte.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ±5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 18 (MODE PIN = HIGH)

OPERATION	$\overline{\text{CE}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	$\overline{\text{COEA}}$	$\overline{\text{COEB}}$	$\overline{\text{CWEA}}$	$\overline{\text{CWEB}}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1-DQ8, DQP1 bank A	L	L	H	L	H	H	H
READ DQ1-DQ8, DQP1 bank B	L	L	H	H	L	H	H
READ DQ9-DQ16, DQP2 bank A	L	H	L	L	H	H	H
READ DQ9-DQ16, DQP2 bank B	L	H	L	H	L	H	H
READ DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	L	H	H	H
READ DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	H	L	H	H
WRITE DQ1-DQ8, DQP1 bank A	L	L	H	X	X	L	H
WRITE DQ1-DQ8, DQP1 bank B	L	L	H	X	X	H	L
WRITE DQ9-DQ16, DQP2 bank A	L	H	L	X	X	L	H
WRITE DQ9-DQ16, DQP2 bank B	L	H	L	X	X	H	L
WRITE DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	X	X	L	H
WRITE DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	X	X	H	L
WRITE DQ1-DQ8, DQP1 banks A & B	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2 banks A & B	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2 banks A & B	L	L	L	X	X	L	L

NOTE: $\overline{\text{CE}}$, when taken inactive while $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$ remain active, allows a chip-enable-controlled WRITE to be performed.

TRUTH TABLE
8K x 18 (MODE PIN = LOW)

OPERATION	$\overline{\text{CE}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	$\overline{\text{COEA}}$	$\overline{\text{COEB}}$	$\overline{\text{CWEA}}$	$\overline{\text{CWEB}}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1-DQ8, DQP1	L	L	H	L	L	H	H
READ DQ9-DQ16, DQP2	L	H	L	L	L	H	H
READ DQ1-DQ16, DQP1, DQP2	L	L	L	L	L	H	H
WRITE DQ1-DQ8, DQP1	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2	L	L	L	X	X	L	L

NOTE:

1. $\overline{\text{CE}}$, when taken inactive while $\overline{\text{CWEA}}$ and $\overline{\text{CWEB}}$ remain active, allows a chip-enable-controlled WRITE to be performed.
2. $\overline{\text{COEA}}$ and $\overline{\text{COEB}}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{\text{CWEA}}$ and $\overline{\text{CWEB}}$ must both be LOW to enable a WRITE cycle. Either $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1.0V to +7.0V
Storage Temperature .... -55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		Vcc	4.75	5.25	V	
Input High Voltage		VIH	2.2	Vcc+0.3	V	1
Input Low Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	VIN = GND to Vcc	ILI	-5	5	µA	
Output Leakage Current	VI/O = GND to Vcc Output(s) Disabled	ILO	-5	5	µA	
Output Low Voltage	IOL = 4.0mA	VOL		0.4	V	1
Output High Voltage	IOH = -1.0mA	VOH	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty cycle VIN = GND to Vcc	ICC1	130	220	mA	
Power Supply Current: Average Operating Current	50% Duty cycle VIN = GND to Vcc	ICC2	70	120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0}$ = $\overline{CS1}$ ≥ Vcc - 0.2V Vcc = MAX VIL ≤ Vss + 0.2V VIH ≥ Vcc - 0.2V	ISB	20	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	CIN	6	pF	3
Output Capacitance		CI/O	6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient	Still Air	θJA	100	°C/W	
Thermal resistance – Junction to Case		θJC	45	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$, Vcc = 5V ±5%)

DESCRIPTION		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle									
READ cycle time	^{t}RC	20		25		35		ns	4, 5
Address access time (A0-A11)	^{t}AA		20		25		35	ns	
A12 address access time	^{t}A12A		15		17		25	ns	
Chip Enable access time	^{t}ACE		20		20		25	ns	
Chip Select access time	^{t}ACS		20		25		35	ns	
Output Enable access time	^{t}AOE		8		10		13	ns	
Output hold from address change	^{t}OH	3		3		3		ns	
Chip Select to output Low-Z	^{t}LZCS	3		3		3		ns	
Output Enable to output Low-Z	^{t}LZOE	2		2		2		ns	
Chip deselect to output High-Z	^{t}HZCS		15		15		25	ns	6
Output disable to output High-Z	^{t}HZOE		10		10		14	ns	6
Address Latch Enable pulse width	^{t}CALEN	8		8		10		ns	
Address setup to latch LOW	^{t}ASL	4		4		6		ns	
Address hold from latch LOW	^{t}AHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	^{t}WC	20		25		35		ns	
Address valid to end of write	^{t}AW	15		18		25		ns	
A12 address valid to end of write	^{t}A12W	15		18		25		ns	
Chip Select to end of write	^{t}CW	15		18		25		ns	
Data valid to end of write	^{t}DW	10		10		10		ns	
Data hold from end of write	^{t}DH	0		0		0		ns	
Write Enable output in High-Z	^{t}HZWE		12		15		15	ns	6
Write disable to output in Low-Z	^{t}LZWE	3		3		3		ns	
WRITE pulse width	^{t}WP	15		18		25		ns	
$\overline{\text{CE}}$ pulse width (during Chip Enable controlled write)	^{t}CP	15		18		25		ns	
Address setup time	^{t}AS	0		0		0		ns	
WRITE recovery time	^{t}WR	0		0		0		ns	
Address Latch Enable pulse width	^{t}CALEN	8		8		10		ns	
Address setup to latch LOW	^{t}ASL	4		4		6		ns	
Address hold from latch LOW	^{t}AHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

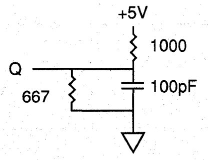


Fig. 1 OUTPUT LOAD EQUIVALENT

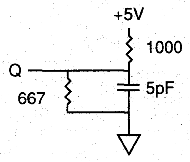


Fig. 2 OUTPUT LOAD EQUIVALENT

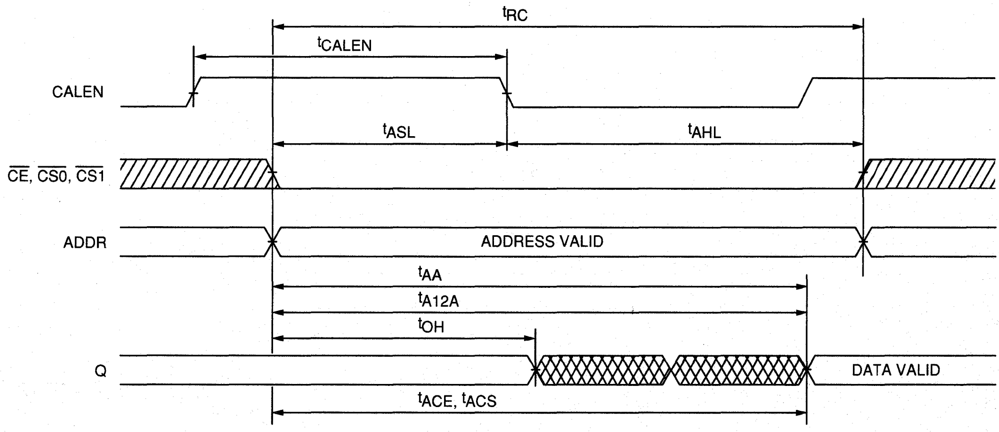
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{\text{CWE}}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. ^{t}HZCS, ^{t}HZOE, and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.

READ CYCLE NO. 1

(Address Controlled)

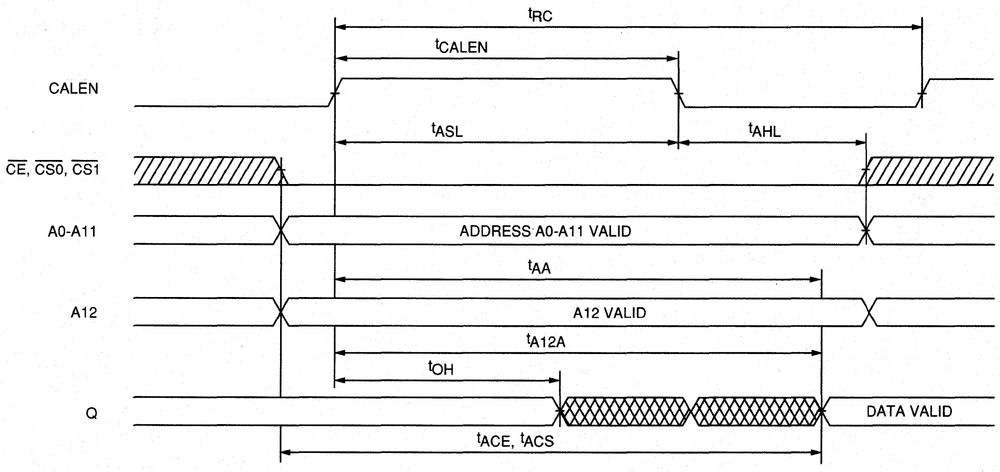
$\overline{CWEA} = \overline{CWEB} = V_{IH}$; $\overline{COEA}$ and/or $\overline{COEB} = V_{IL}$



READ CYCLE NO. 2

(CALEN Controlled)

$\overline{CWEA} = \overline{CWEB} = V_{IH}$; $\overline{COEA}$ and/or $\overline{COEB} = V_{IL}$

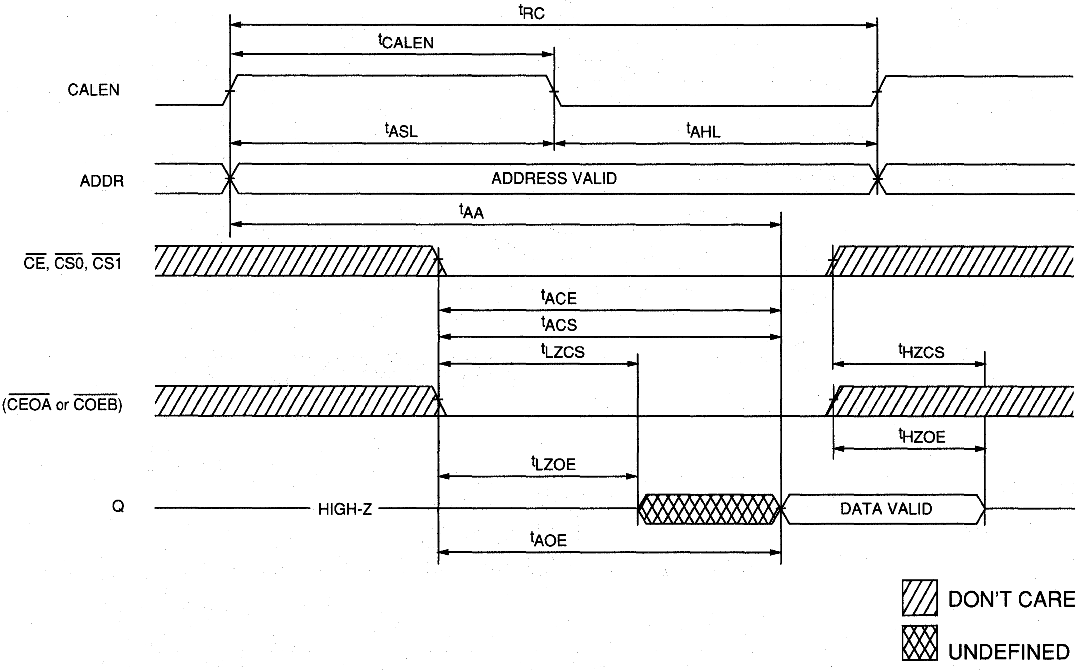


▨ DON'T CARE

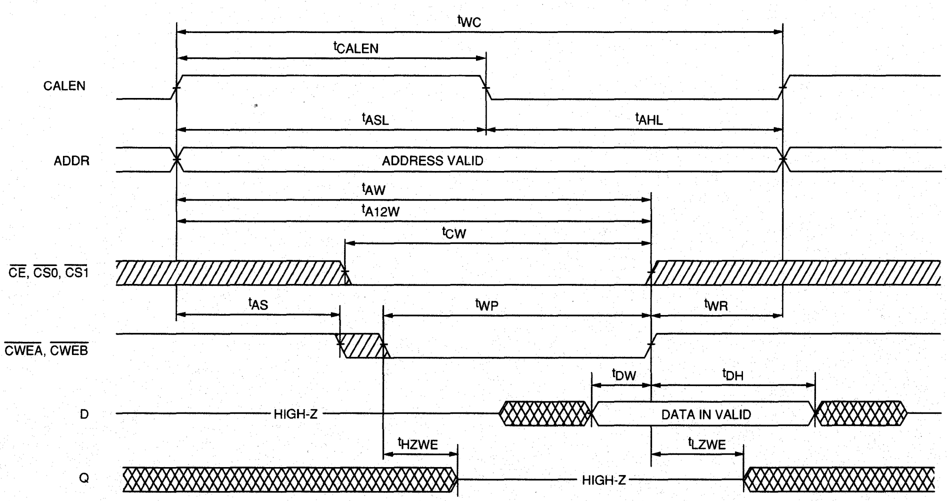
▦ UNDEFINED

READ CYCLE NO. 3

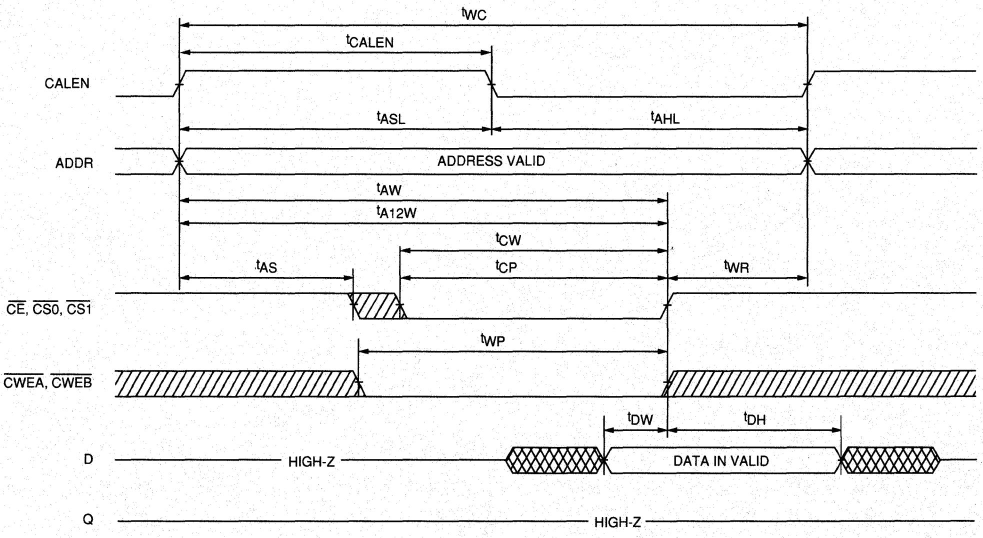
$\overline{\text{CWEA}} = \overline{\text{CWEB}} = V_{IH}$



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



▨ DON'T CARE

▩ UNDEFINED

CACHE DATA SRAM

DUAL 4K x 18 SRAM, SINGLE 8K x 18 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

- Automatic WRITE cycle completion
- Operates as two 4K x 18 SRAMs with common addresses and data; also configurable as a single 8K x 18 SRAM
- Automatically controlled input address latches
- Built-in input data latches
- Separate upper and lower Byte Select
- Fast access times: 24 and 28ns allow operation with 33 MHz and 25 MHz microprocessor systems
- Fast Output Enable: 8ns
- Parity bits provided for large cache applications such as secondary cache for the Intel 80486 microprocessor
- Directly compatible with the Intel 82485 cache controller

OPTIONS	MARKING
• Timing	
24ns access (33 MHz)	-24
28ns access (25 MHz)	-28
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

GENERAL DESCRIPTION

The MT56C2818 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

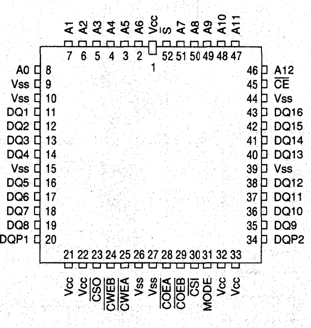
The MT56C2818 is a highly integrated cache data memory building block. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 18-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 18-bit SRAM.

Strobe ($\overline{S}$) controls the on-chip address and data latches. During READ and WRITE cycles the address latch is always transparent except for the time period ^{t}ALO following the rising edge of $\overline{S}$. The addresses are "locked out" during this time.

$\overline{S}$ has no effect on the data latch during a READ cycle. During a WRITE cycle, data is latched on the rising edge of $\overline{S}$. The rising edge of $\overline{S}$ also initiates the completion of the WRITE cycle.

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-4)



The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations. Power consumption may be reduced by keeping either $\overline{CE}$ inactive (HIGH), or $\overline{CS0}$ and $\overline{CS1}$ inactive (HIGH) as much as possible.

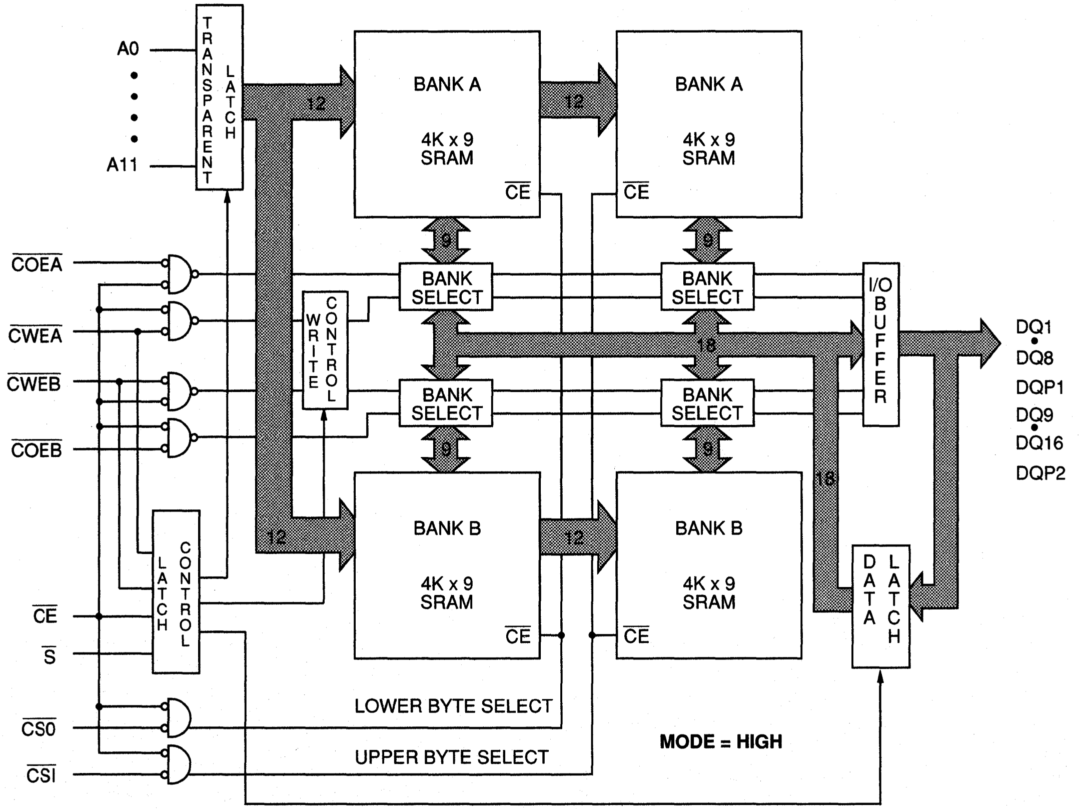
Outputs are enabled on a HIGH to LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH to LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C2818 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

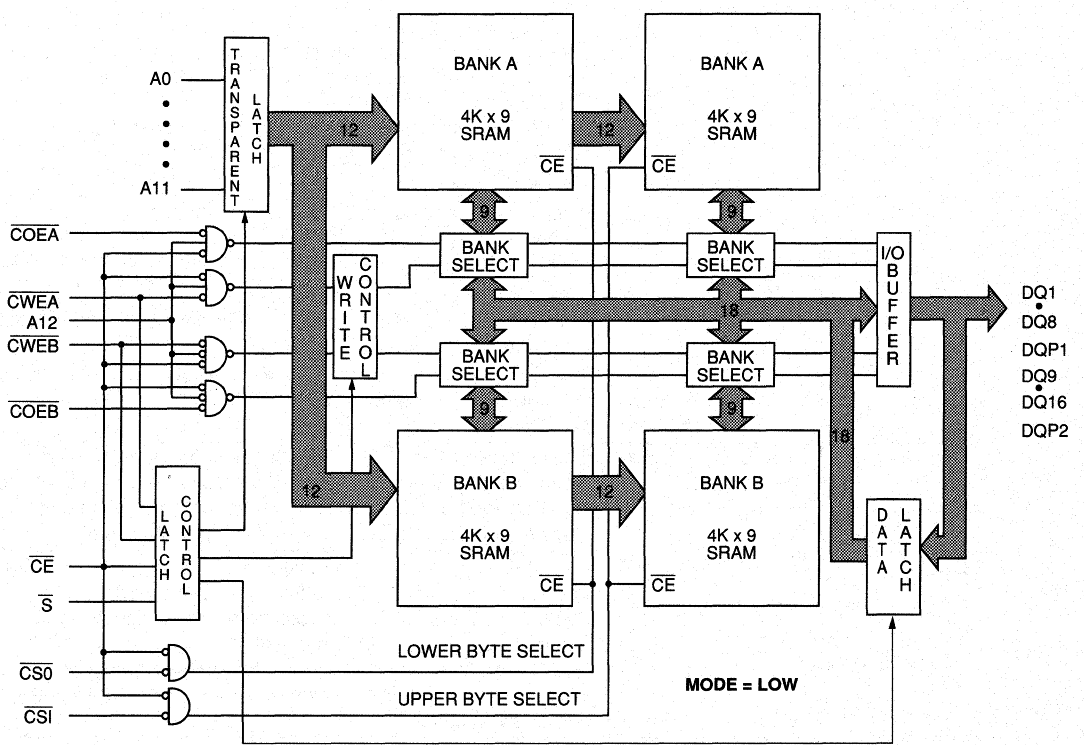
FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 18
(TWO-WAY SET ASSOCIATIVE)



FUNCTIONAL BLOCK DIAGRAM
($\overline{\text{COEA}}$ = $\overline{\text{COEB}}$; $\overline{\text{CWEA}}$ = $\overline{\text{CWEB}}$)

8K x 18
(DIRECT MAP)



PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: A0-A11 are always sampled (transparent latch) except for the time ^{t}WAH and ^{t}ALO following the rising edge of $\overline{\text{S}}$.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K x 18 configuration. It is not used in the dual 4K x 18 configuration.
52	$\overline{\text{S}}$	Input	Strobe: This signal controls the internal data and address latches. The address latch is always transparent except for the time period ^{t}ALO following the rising edge of $\overline{\text{S}}$. The addresses are "locked out" during this time period. $\overline{\text{S}}$ does not affect the data latch during a READ cycle. During a WRITE cycle the rising edge of $\overline{\text{S}}$ latches the data. The rising edge also initiates the termination of the WRITE cycle.
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 18 configuration. When the pin is tied LOW, the device is configured as an 8K x 18 SRAM.
23, 30	$\overline{\text{CS0}}$, $\overline{\text{CS1}}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{\text{CS0}}$ is LOW, DQ1-DQ8 and DQP1 are enabled. When $\overline{\text{CS1}}$ is LOW, DQ9-DQ16 and DQP2 are enabled. Significant power savings can be achieved by keeping $\overline{\text{CS0}}$ and $\overline{\text{CS1}}$ inactive as much as possible.
45	$\overline{\text{CE}}$	Input	Chip Enable: When $\overline{\text{CE}}$ is LOW, the device is enabled. It is a global control signal that activates both bank "A" and bank "B" for READ or WRITE operations. Significant power savings can be achieved by keeping $\overline{\text{CE}}$ inactive as much as possible.
28, 29	$\overline{\text{COEA}}$, $\overline{\text{COEB}}$	Input	Output Enable: In the dual configuration, the signal that is LOW enables bank "A" or "B". Simultaneous LOW assertion will deselect both banks. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{\text{COEA}}$ or $\overline{\text{COEB}}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{\text{CWEA}}$, $\overline{\text{CWEB}}$	Input	Write Enable: In the dual configuration, the signal that is LOW enables a data write to the addressed memory location. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$ can be tied LOW externally, allowing the other signal to control the write function.
20, 34	DQP1, DQP2	Input/ Output	Parity Data I/O: DQP1 is the parity bit for the lower byte. DQP2 is the parity bit for the upper byte.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ±5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE
DUAL 4K x 18 (MODE PIN = HIGH)

OPERATION	$\overline{\text{CE}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	$\overline{\text{COEA}}$	$\overline{\text{COEB}}$	$\overline{\text{CWEA}}$	$\overline{\text{CWEB}}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1-DQ8, DQP1 bank A	L	L	H	L	H	H	H
READ DQ1-DQ8, DQP1 bank B	L	L	H	H	L	H	H
READ DQ9-DQ16, DQP2 bank A	L	H	L	L	H	H	H
READ DQ9-DQ16, DQP2 bank B	L	H	L	H	L	H	H
READ DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	L	H	H	H
READ DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	H	L	H	H
WRITE DQ1-DQ8, DQP1 bank A	L	L	H	X	X	L	H
WRITE DQ1-DQ8, DQP1 bank B	L	L	H	X	X	H	L
WRITE DQ9-DQ16, DQP2 bank A	L	H	L	X	X	L	H
WRITE DQ9-DQ16, DQP2 bank B	L	H	L	X	X	H	L
WRITE DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	X	X	L	H
WRITE DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	X	X	H	L
WRITE DQ1-DQ8, DQP1 banks A & B	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2 banks A & B	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2 banks A & B	L	L	L	X	X	L	L

TRUTH TABLE
8K x 18 (MODE PIN = LOW)

OPERATION	$\overline{\text{CE}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	$\overline{\text{COEA}}$	$\overline{\text{COEB}}$	$\overline{\text{CWEA}}$	$\overline{\text{CWEB}}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1-DQ8, DQP1	L	L	H	L	L	H	H
READ DQ9-DQ16, DQP2	L	H	L	L	L	H	H
READ DQ1-DQ16, DQP1, DQP2	L	L	L	L	L	H	H
WRITE DQ1-DQ8, DQP1	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2	L	L	L	X	X	L	L

NOTE: When mode pin is LOW, $\overline{\text{COEA}}$ and $\overline{\text{COEB}}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{\text{CWEA}}$ and $\overline{\text{CWEB}}$ must both be LOW to enable a WRITE cycle. Either $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	-1.0V to +7.0V
Storage Temperature (Plastic)	-55°C to +150°C
Power Dissipation (PLCC)	1.2W
Power Dissipation (PQFP)	1.2W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		Vcc	4.75	5.25	V	
Input High Voltage		V_{IH}	2.2	Vcc +0.3	V	1
Input Low Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	V_{IN} = GND to Vcc	I_{LI}	-5	5	µA	
Output Leakage Current	$V_{I/O}$ = GND to Vcc Output(s) Disabled	I_{LO}	-5	5	µA	
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1

DESCRIPTION	CONDITIONS		SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty Cycle V_{IN} = GND to Vcc		I_{CC1}	145	220	mA	
Power Supply Current: Average Operating Current	50% Duty Cycle V_{IN} = GND to Vcc		I_{CC2}	70	120	mA	
Power Supply Current: CMOS Standby	$\overline{CS1}$ ≥ Vcc -0.2V and $\overline{CS0}$ ≥ Vcc -0.2V or Vcc = MAX, f = 0 V_{IL} ≤ Vss +0.2V V_{IH} ≥ Vcc -0.2V	CE ≤ Vss +0.2V	I_{SB1}	20	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	C_I	6	pF	3
Input/Output Capacitance		$C_{I/O}$	6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient	Still Air	θ_{JA}	100	°C/W	
Thermal resistance – Junction to Case		θ_{JC}	45	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 8) (0°C ≤ T_A ≤ +70°C, Vcc = 5V ±5%)

DESCRIPTION		-24		-28			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle							
READ cycle time	^{t}RC	24		28		ns	4, 5
Address access time (A0-A11)	^{t}AA		24		28	ns	4, 5
A12 address access time	^{t}A12A		17		19	ns	
Chip Enable access time	^{t}ACE		23		26	ns	
Chip Select access time	^{t}ACS		23		26	ns	
Output Enable access time	^{t}AOE		8		10	ns	
Output hold from address change	^{t}OH	3		3		ns	
Chip Select/Chip Enable to output Low-Z	^{t}LZCS	3		3		ns	
Output Enable to output Low-Z	^{t}LZOE	2		2		ns	
Chip deselect/chip disable to output High-Z	^{t}HZCS		15		15	ns	6
Output disable to output High-Z	^{t}HZOE	2	10	2	10	ns	6
WRITE Cycle							
WRITE cycle time	^{t}WC	24		28		ns	
$\overline{\text{S}}$ strobe HIGH level width	^{t}SWH	11		14		ns	7
$\overline{\text{S}}$ strobe LOW level width	^{t}SWL	11		14		ns	7
WRITE, Chip Enable/Write Enable to $\overline{\text{S}}$ strobe setup	^{t}WSS	10		12		ns	7
WRITE, Chip Enable/Write Enable to $\overline{\text{S}}$ strobe hold	^{t}WSH	2		2		ns	7
WRITE, address setup to $\overline{\text{S}}$ strobe	^{t}WAS	13		16		ns	7
WRITE, address hold to $\overline{\text{S}}$ strobe	^{t}WAH	2		2		ns	7
Address latch closed	^{t}ALO		8		8	ns	7
Chip Select to $\overline{\text{S}}$ strobe setup	^{t}CSS	13		16		ns	7
Chip Select to $\overline{\text{S}}$ strobe hold	^{t}CSH	2		2		ns	7
Data to $\overline{\text{S}}$ strobe setup	^{t}DSS	5		5		ns	7
Data to $\overline{\text{S}}$ strobe hold	^{t}DSH	3		3		ns	7
Write Enable to output in High-Z	^{t}HZWE		15		15	ns	6
Write Enable to output in Low-Z	^{t}LZWE	8		8		ns	

AC TEST CONDITIONS

Input pulse levels .... Vss to 3.0V
Input rise and fall times 3ns
Input timing reference levels 1.5V
Output reference levels 1.5V
Output load .... Reference Figure 1
(see notes 6 and 8).

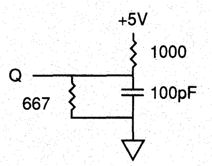


Fig. 1 OUTPUT LOAD EQUIVALENT

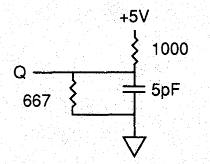
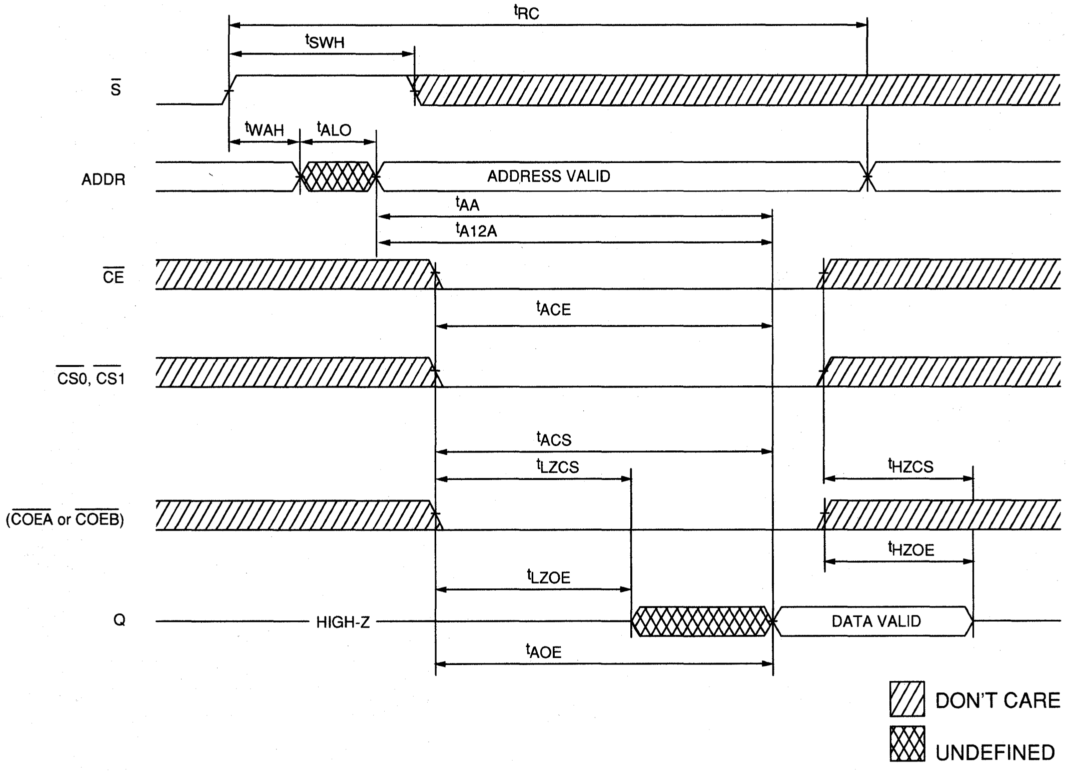


Fig. 2 OUTPUT LOAD EQUIVALENT

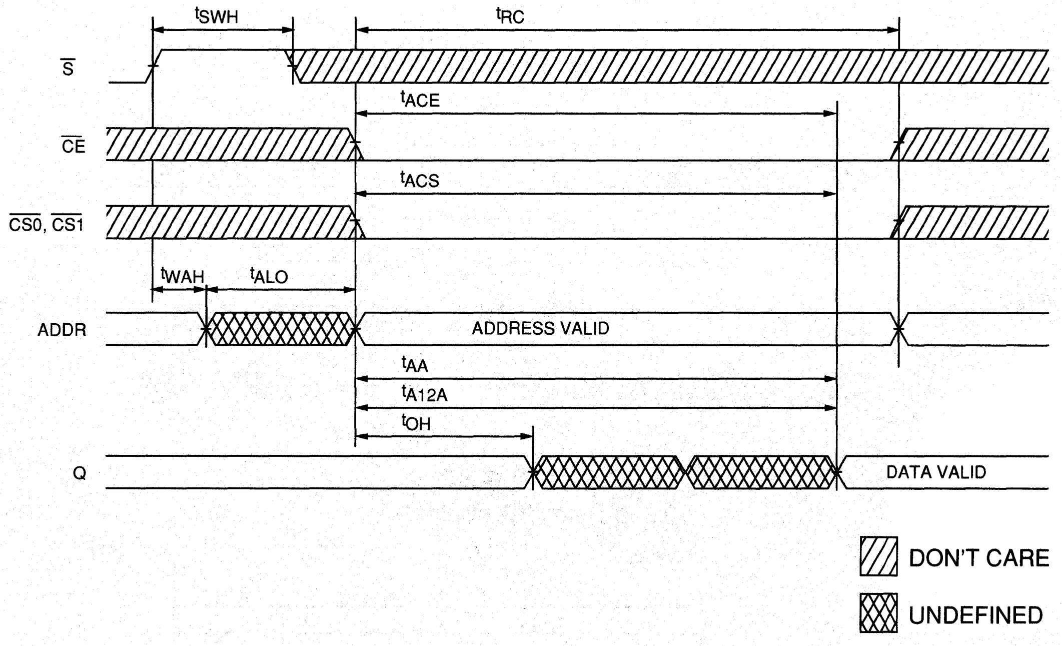
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{\text{CWE}}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. ^{t}HZCS, ^{t}HZOE, and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. Self-timed WRITE parameter.
8. Output timing should be derated by 1ns for each additional 30pf of capacitive loading.

READ CYCLE NO. 1
($\overline{CWEA} = \overline{CWEB} = V_{IH}$)

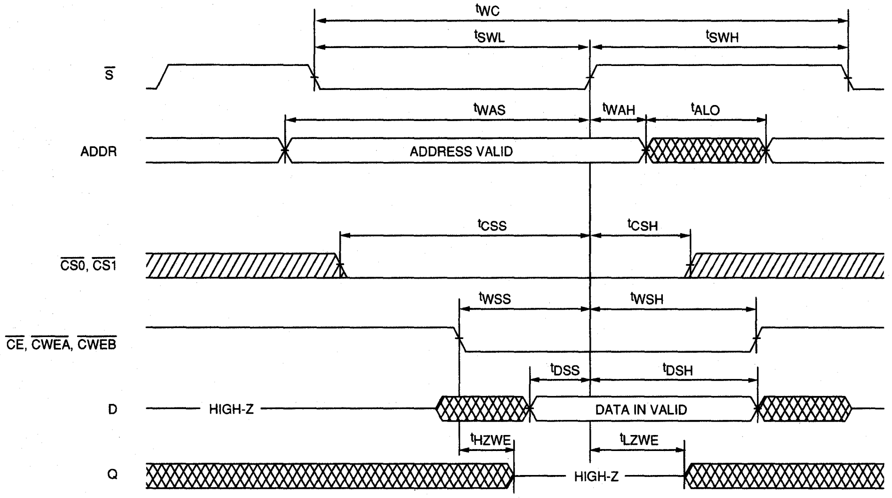


READ CYCLE NO. 2
($\overline{\text{COEA}}$ and/or $\overline{\text{COEB}}$ = V_{IL})
($\overline{\text{CWEA}}$ = $\overline{\text{CWEB}}$ = V_{IH})



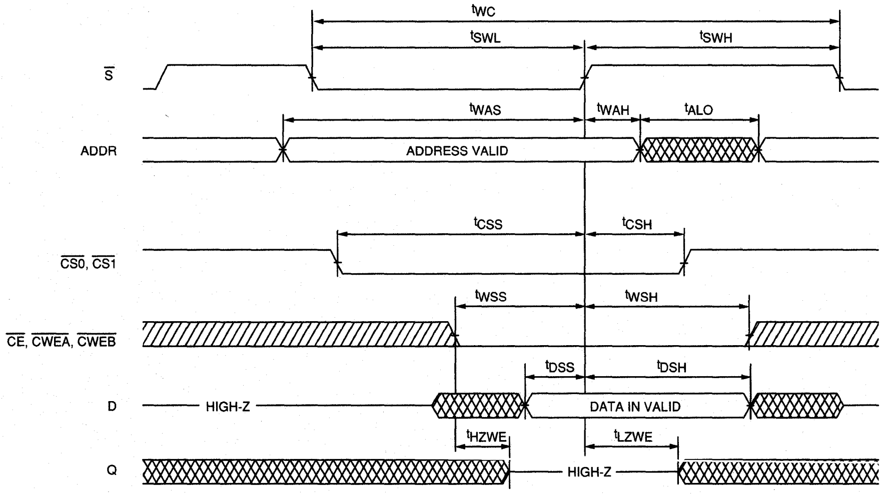
WRITE CYCLE NO. 1

(Write Enable/Chip Enable Controlled)



WRITE CYCLE NO. 2

(Chip Select Controlled)



▨ DON'T CARE

▩ UNDEFINED

CACHE DATA SRAM

DUAL 4K x 18 SRAM, SINGLE 8K x 18 SRAM

CONFIGURABLE CACHE DATA SRAM

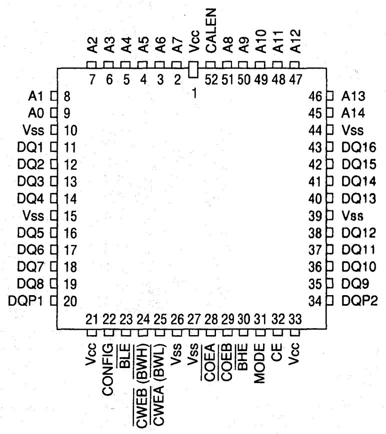
FEATURES

- Operates as two 4K x 18 SRAMs with common addresses and data; also configurable as a single 8K x 18 SRAM
- Built-in input address latches (A0-A12)
- Separate upper and lower Byte Select
- Fast access times: 20, 25 and 35ns allow operation with 40, 33 and 25 MHz microprocessor systems
- Fast Output Enable: 8ns
- Directly interfaces with the Intel 82385 cache controller as well as other 80386 and 80486 cache memory controllers
- Parity bits provided for large cache applications such as secondary cache for the Intel 80486 microprocessors

OPTIONS	MARKING
• Timing	
20ns access (40 MHz)	-20
25ns access (33 MHz)	-25
35ns access (25 MHz)	-35
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-4)



GENERAL DESCRIPTION

The MT56C3818 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C3818 is a highly integrated cache data memory building block. It easily interfaces with cache controllers for the Intel 80386 in either the DIRECT MAPPED or TWO-WAY SET ASSOCIATIVE mode. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 18-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 18-bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations.

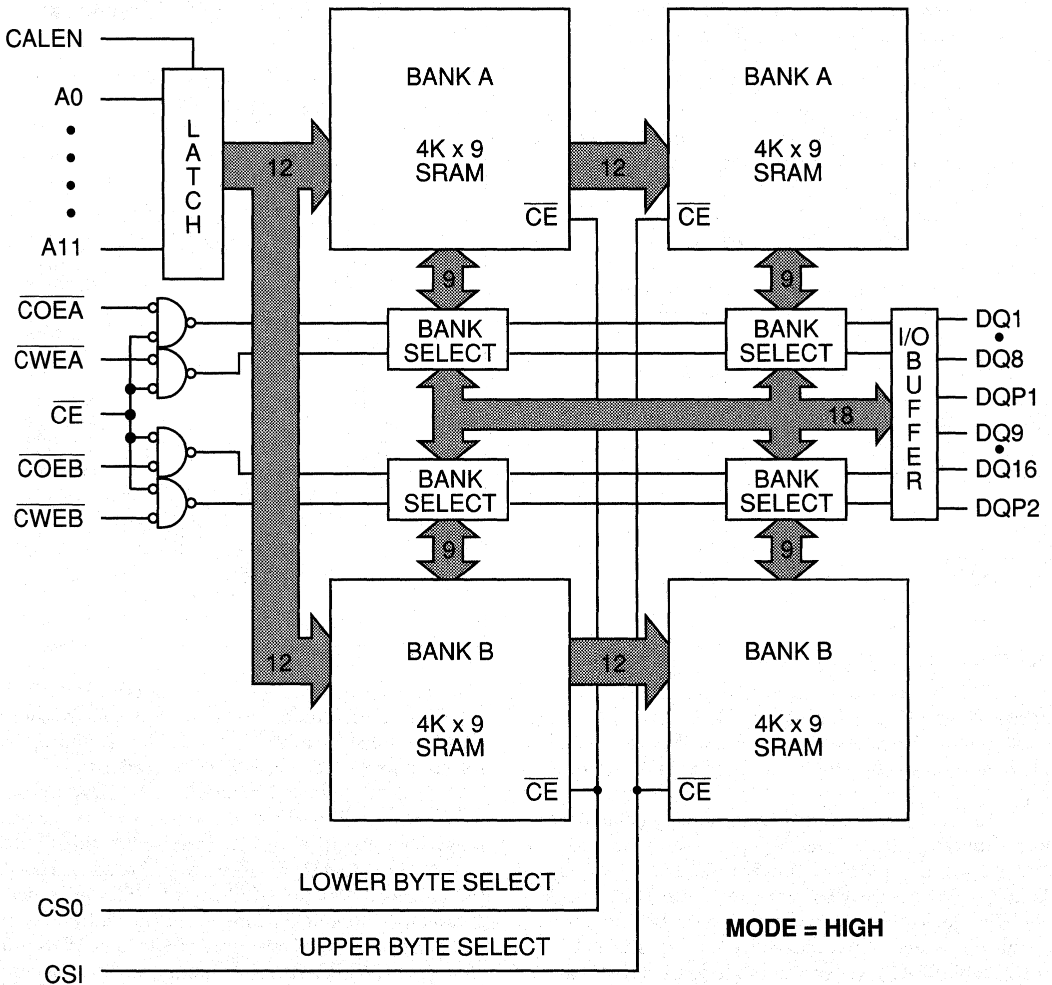
Outputs are enabled on a HIGH to LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH to LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C3818 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM

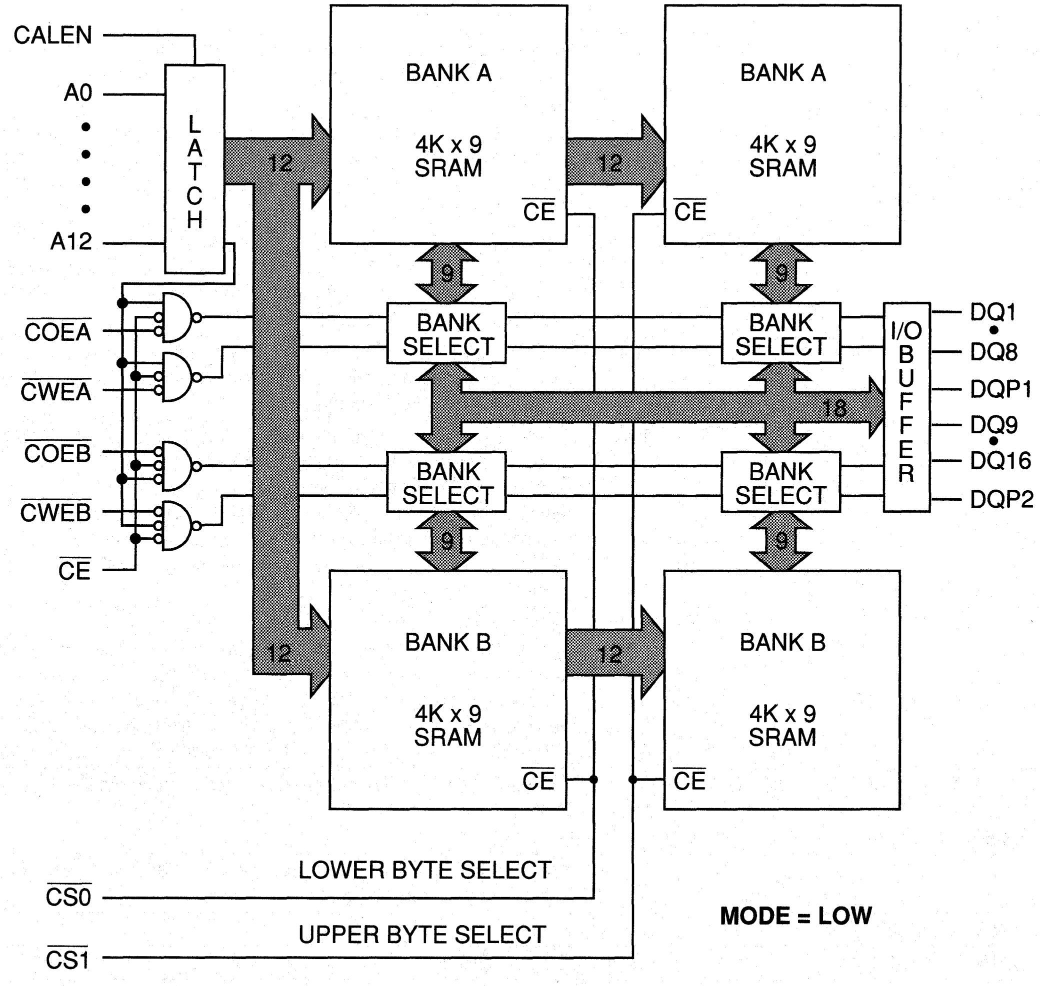
DUAL 4K x 18
(TWO-WAY SET ASSOCIATIVE)



MODE = HIGH

FUNCTIONAL BLOCK DIAGRAM

8K x 18
(DIRECT MAP)



MODE = LOW

PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K x 18 configuration. It is not used in the dual 4K x 18 configuration. This input is latched by the negative edge of CALEN.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A12).
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 18 configuration. When the pin is tied LOW, the device is configured as an 8K x 18 SRAM.
23, 30	$\overline{\text{CS0}}$, $\overline{\text{CS1}}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{\text{CS0}}$ is LOW, DQ1-DQ8 and DQP1 are enabled. When $\overline{\text{CS1}}$ is LOW, DQ9-DQ16 and DQP2 are enabled.
45	$\overline{\text{CE}}$	Input	Chip Enable: When $\overline{\text{CE}}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{\text{COEA}}$, $\overline{\text{COEB}}$	Input	Output Enable: In the dual configuration, the signal that is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{\text{COEA}}$ or $\overline{\text{COEB}}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{\text{CWEA}}$, $\overline{\text{CWEB}}$	Input	Write Enable: In the dual configuration, the signal that is LOW enables a data write to the addressed memory location. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$ can be tied LOW externally, allowing the other signal to control the write function.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
20, 34	DQP1 DQP2	Input/ Output	Parity Data I/O: DQP1 is the parity bit for the lower byte. DQP2 is the parity bit for the upper byte.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ±5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 18 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1-DQ8,DQP1 bank A	L	L	H	L	H	H	H
READ DQ1-DQ8, DQP1 bank B	L	L	H	H	L	H	H
READ DQ9-DQ16, DQP2 bank A	L	H	L	L	H	H	H
READ DQ9-DQ16, DQP2 bank B	L	H	L	H	L	H	H
READ DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	L	H	H	H
READ DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	H	L	H	H
WRITE DQ1-DQ8, DQP1 bank A	L	L	H	X	X	L	H
WRITE DQ1-DQ8, DQP1 bank B	L	L	H	X	X	H	L
WRITE DQ9-DQ16, DQP2 bank A	L	H	L	X	X	L	H
WRITE DQ9-DQ16, DQP2 bank B	L	H	L	X	X	H	L
WRITE DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	X	X	L	H
WRITE DQ1 -DQ16, DQP1, DQP2 bank B	L	L	L	X	X	H	L
WRITE DQ1-DQ8, DQP1 banks A & B	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2 banks A & B	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2 banks A & B	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ or $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

TRUTH TABLE
8K x 18 (MODE PIN = LOW)

OPERATION	$\overline{\text{CE}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	$\overline{\text{COEA}}$	$\overline{\text{COEB}}$	$\overline{\text{CWEA}}$	$\overline{\text{CWEB}}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1-DQ8, DQP1	L	L	H	L	L	H	H
READ DQ9-DQ16, DQP2	L	H	L	L	L	H	H
READ DQ1-DQ16, DQP1, DQP2	L	L	L	L	L	H	H
WRITE DQ1-DQ8, DQP1	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2	L	L	L	X	X	L	L

NOTE:
1. $\overline{\text{CE}}$, when taken inactive while $\overline{\text{CWEA}}$ and $\overline{\text{CWEB}}$ remain active, allows a chip-enable-controlled WRITE to be performed.
2. $\overline{\text{COEA}}$ and $\overline{\text{COEB}}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{\text{CWEA}}$ and $\overline{\text{CWEB}}$ must both be LOW to enable a WRITE cycle. Either $\overline{\text{CWEA}}$ or $\overline{\text{CWEB}}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1.0V to +7.0V
Storage Temperature .... -55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		Vcc	4.75	5.25	V	
Input High Voltage		V_{IH}	2.2	Vcc +0.3	V	1
Input Low Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	V_{IN} = GND to Vcc	IL_I	-5	5	µA	
Output Leakage Current	$V_{I/O}$ = GND to Vcc Output(s) Disabled	IL_O	-5	5	µA	
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty Cycle V_{IN} = GND to Vcc	I_{CC1}	130	220	mA	
Power Supply Current: Average Operating Current	50% Duty Cycle V_{IN} = GND to Vcc	I_{CC2}	70	120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0} = \overline{CS1} \ge$ Vcc -0.2V Vcc = MAX $V_{IL} \le$ Vss +0.2V $V_{IH} \ge$ Vcc -0.2V	I_{SB}	20	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	C_I	6	pF	3
Output Capacitance		$C_{I/O}$	6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient	Still Air	θ_{JA}	100	°C/W	
Thermal resistance – Junction to Case		θ_{JC}	45	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$, Vcc = 5V ±5%)

DESCRIPTION	SYM	-20 MIN	-20 MAX	-25 MIN	-25 MAX	-35 MIN	-35 MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^{t}RC	20		25		35		ns	4, 5
Address access time (A0-A12)	^{t}AA		20		25		35	ns	
Chip Enable access time	^{t}ACE		20		20		25	ns	
Chip Select access time	^{t}ACS		20		25		35	ns	
Output Enable access time	^{t}AOE		8		10		13	ns	
Output hold from address change	^{t}OH	3		3		3		ns	
Chip Select to output Low-Z	^{t}LZCS	3		3		3		ns	
Output Enable to output Low-Z	^{t}LZOE	2		2		2		ns	
Chip deselect to output High-Z	^{t}HZCS		15		15		25	ns	6
Output disable to output High-Z	^{t}HZOE		10		10		14	ns	6
Address Latch Enable pulse width	^{t}CALEN	8		8		10		ns	
Address setup to latch LOW	^{t}ASL	4		4		6		ns	
Address hold from latch LOW	^{t}AHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	^{t}WC	20		25		35		ns	
Address valid to end of write	^{t}AW	15		18		25		ns	
Chip Select to end of write	^{t}CW	15		18		25		ns	
Data valid to end of write	^{t}DW	10		10		10		ns	
Data hold from end of write	^{t}DH	0		0		0		ns	
Write Enable output in High-Z	^{t}HZWE		12		15		15	ns	6
Write disable to output in Low-Z	^{t}LZWE	3		3		3		ns	
WRITE pulse width	^{t}WP	15		18		25		ns	
$\overline{CE}$ pulse width (during Chip Enable controlled write)	^{t}CP	15		18		25		ns	
Address setup time	^{t}AS	0		0		0		ns	
WRITE recovery time	^{t}WR	0		0		0		ns	
Address Latch Enable pulse width	^{t}CALEN	8		8		10		ns	
Address setup to latch LOW	^{t}ASL	4		4		6		ns	
Address hold from latch LOW	^{t}AHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

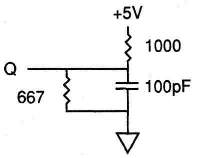


Fig. 1 OUTPUT LOAD EQUIVALENT

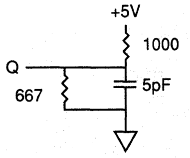


Fig. 2 OUTPUT LOAD EQUIVALENT

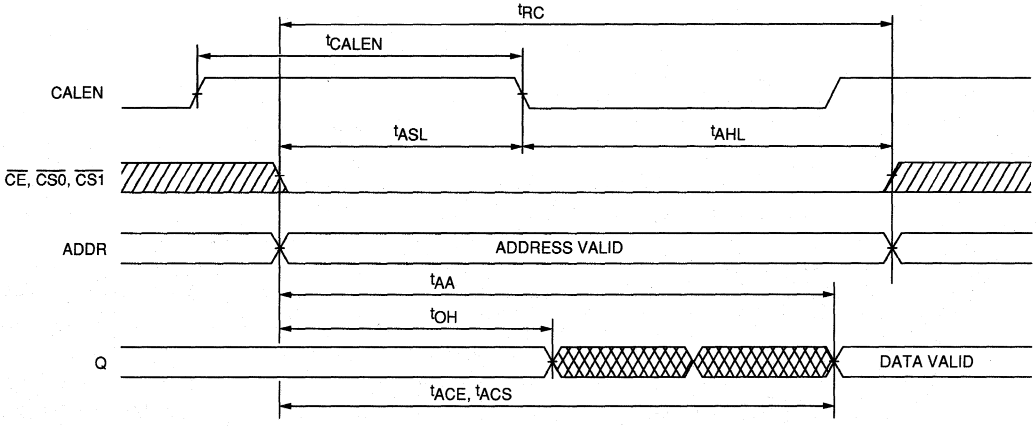
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. ^{t}HZCS, ^{t}HZOE, and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.

READ CYCLE NO. 1

(Address Controlled)

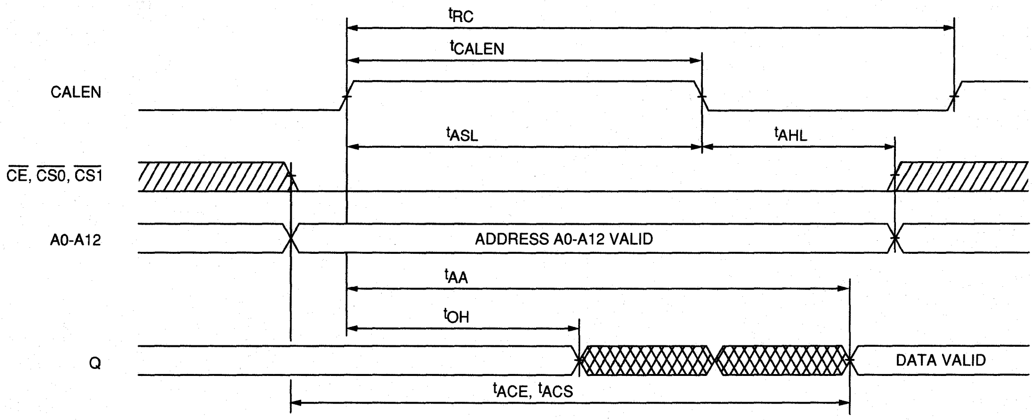
$\overline{\text{CWEA}} = \overline{\text{CWEB}} = \text{V}_{\text{IH}}$; $\overline{\text{COEA}}$ and/or $\overline{\text{COEB}} = \text{V}_{\text{IL}}$



READ CYCLE NO. 2

(CALEN Controlled)

$\overline{\text{CWEA}} = \overline{\text{CWEB}} = \text{V}_{\text{IH}}$; $\overline{\text{COEA}}$ and/or $\overline{\text{COEB}} = \text{V}_{\text{IL}}$

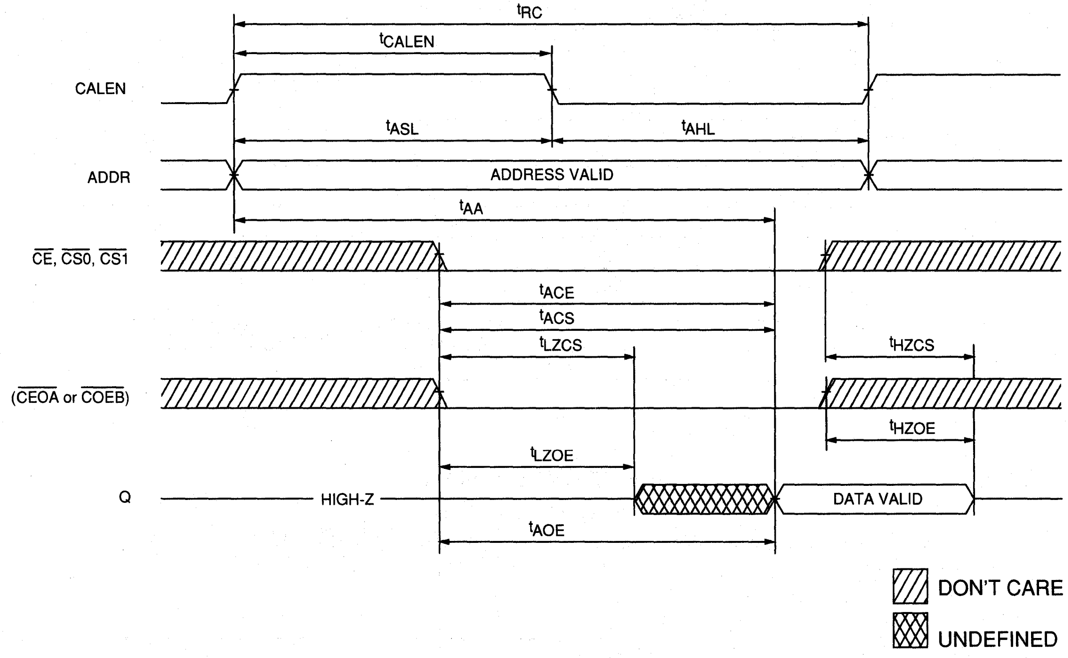


▨ DON'T CARE

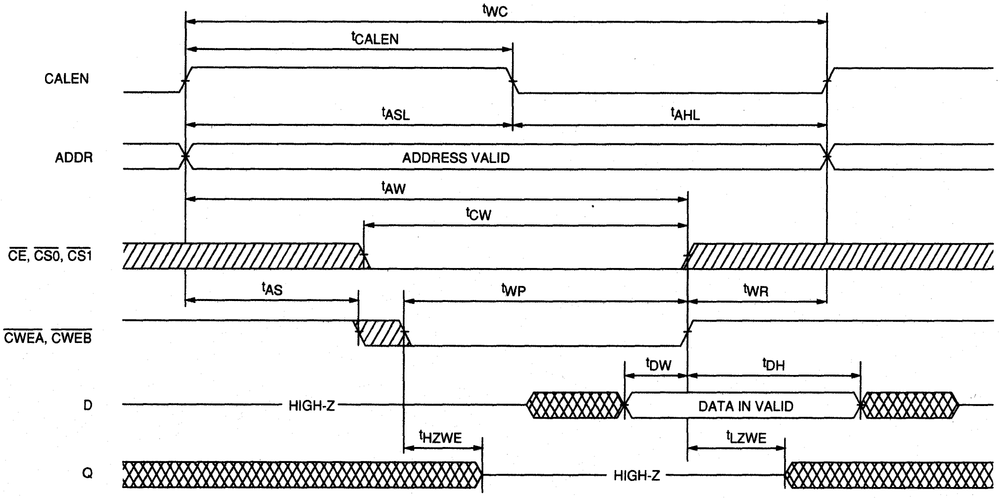
▩ UNDEFINED

READ CYCLE NO. 3

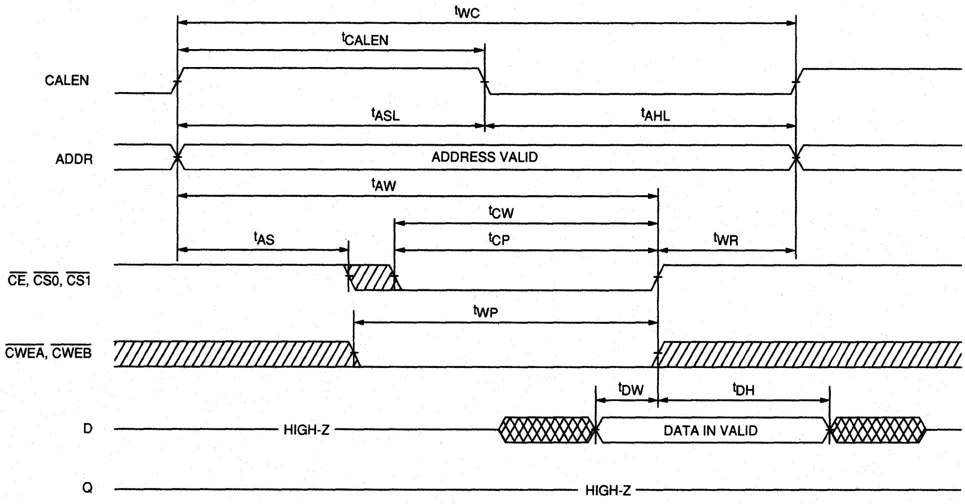
$\overline{\text{CWEA}} = \overline{\text{CWEB}} = \text{V}_{\text{IH}}$



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



▨ DON'T CARE

▩ UNDEFINED

LATCHED SRAM

16K x 18 SRAM

WITH ADDRESS/ DATA INPUT LATCHES

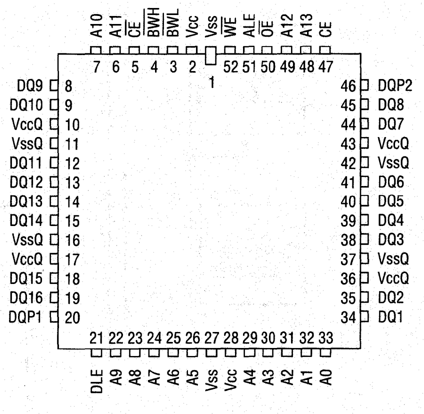
FEATURES

- Fast access times: 15, 17, 20 and 25ns
- Fast Output Enable: 6, 8 and 10ns
- Single +5V ±10% power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Optional +3.3V ±10% output buffer operation
- Separate data input latch
- Common data inputs and data outputs
- BYTE WRITE capability via dual write strobes
- Parity bits
- Address and Chip Enable input latches

OPTIONS	MARKING
• Timing	
15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG
• Density	
16K x 18	MT5C2818

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT5C2818 SRAM integrates a 16K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, latched active HIGH and active LOW chip enables, separate upper and lower byte write strobes and a fast output enable. The device is ideally suited for "pipelined" systems and systems that benefit from a wide data bus. Parity bits are provided for added data integrity.

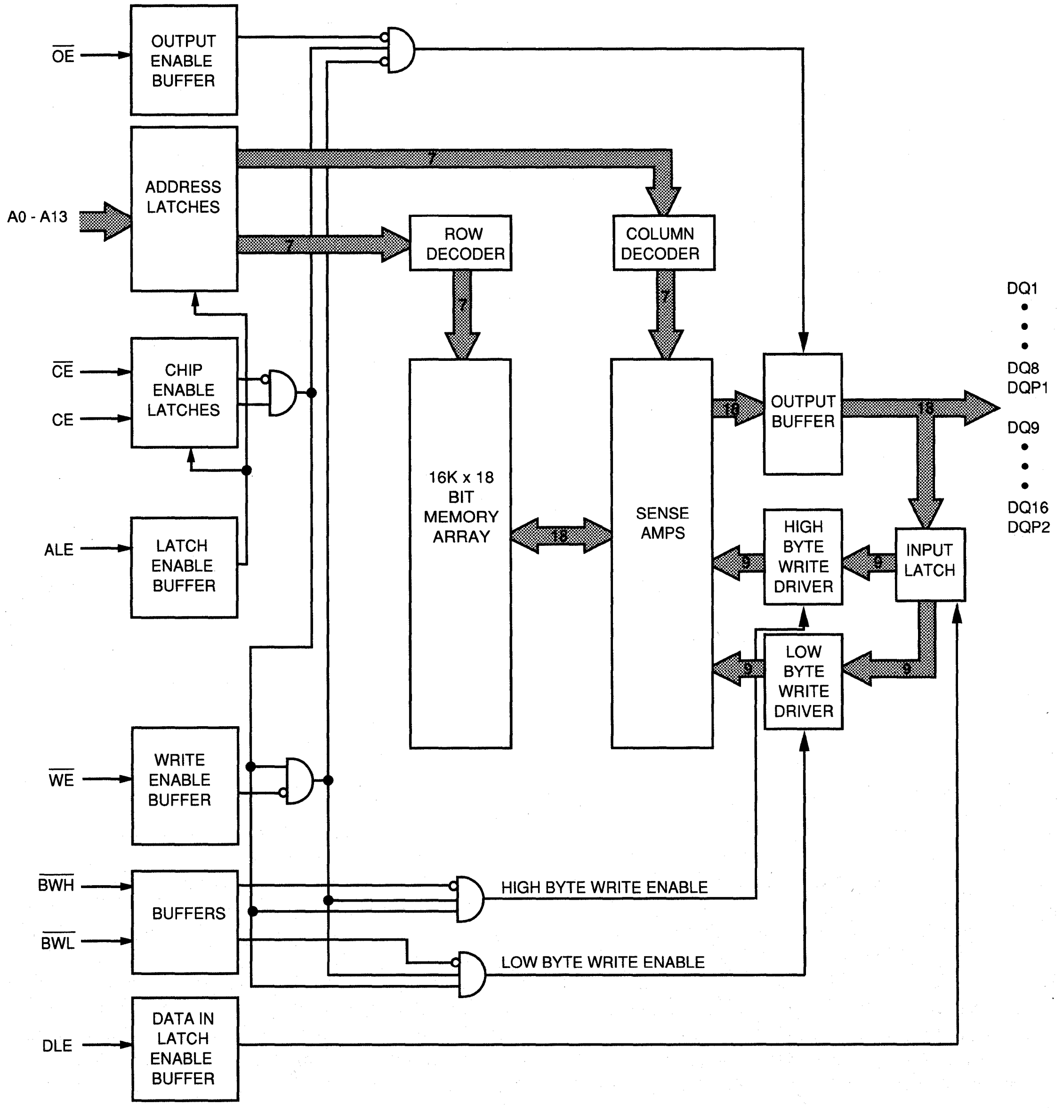
Address and chip enable latches are provided. When address latch enable (ALE) is HIGH, the address and chip enable latches are transparent, allowing the input to flow through the latch. If ALE is LOW, the address and chip enable latch inputs are disabled. This input latch simplifies READ and WRITE cycles by guaranteeing address hold time in a simple fashion.

Dual write strobes ($\overline{\text{BWL}}$ and $\overline{\text{BWH}}$) allow individual bytes to be written. $\overline{\text{BWL}}$ controls DQ1-DQ8 and DQP1, the lower bits. While $\overline{\text{BWH}}$ controls DQ9-DQ16 and DQP2, the upper bits.

A data input latch is provided. When data latch enable (DLE) is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present in the inputs are held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT5C2818 operates from a +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided to allow either +3.3V or +5V TTL operation of the output drivers.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC and PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are either latched or unlatched depending on the state of ALE.
52	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
51	ALE	Input	Address Latch Enable: This signal latches the address, CE, and $\overline{CE}$ inputs on its falling edge. When ALE is HIGH, the latch is transparent.
3, 4	$\overline{BWL}$, $\overline{BWH}$	Input	Byte Write Enables: These active LOW inputs allow individual bytes to be written. When $\overline{BWL}$ is LOW, data is written to the lower byte, D1-D8, DQP1. When $\overline{BWH}$ is LOW, data is written to the upper byte, D9-D16, DQP2. When both $\overline{BWH}$ and $\overline{BWL}$ are HIGH and meet the required setup time to the falling edge of $\overline{WE}$, then the WRITE cycle is aborted.
5, 47	$\overline{CE}$,CE	Input	Chip Enables: These signals are used to enable the device. Both active HIGH (CE) and active LOW ($\overline{CE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH, the data latch is transparent. Input data is latched into the on-chip data latch on the falling edge of DLE.
20, 46	DQP1 DQP2	Input/ Output	Parity Data I/O: These signals are data parity bits. The DQP1 is the parity bit for the lower byte, DQ1-DQ8. DQP2 is the parity bit for the upper byte, DQ9-DQ16.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. When data is latched, DQ1-DQ16 must meet the setup and hold times around DLE.
2, 28	Vcc	Supply	Power Supply: +5V ±10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ±10% or 3.3V ± 10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	CE	$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{BWL}}$	$\overline{\text{BWH}}$	ALE	DLE	$\overline{\text{OE}}$	DQ	DQP
Deselected cycle	L	X	X	X	X	X	X	X	High-Z	High-Z
Deselected	X	H	X	X	X	X	X	X	High-Z	High-Z
READ	H	L	H	X	X	H	X	H	High-Z	High-Z
READ	H	L	H	X	X	H	X	L	Q1-Q16	QP1, QP2
LATCHED READ	H	L	H	X	X	L	X	L	Q1-Q16	QP1, QP2
WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	H	H	X	D1-D16	DP1, DP2
LATCHED WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	L	H	X	D1-D16	DP1, DP2
WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	H	L	X	D1-D16	DP1, DP2
LATCHED WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	L	L	X	D1-D16	DP1, DP2
ABORTED WRITE	H	L	L	H	H	X	X	X	High-Z	High-Z
BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	H	H	X	D1-D8	DP1
LATCHED BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	L	H	X	D1-D8	DP1
BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	H	H	X	D9-D16	DP2
LATCHED BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	L	H	X	D9-D16	DP2
BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	H	L	X	D1-D8	DP1
LATCHED BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	L	L	X	D1-D8	DP1
BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	H	L	X	D9-D16	DP2
LATCHED BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	L	L	X	D9-D16	DP2

NOTE:
1. Latched inputs (Addresses, CE and $\overline{\text{CE}}$) must satisfy the specified setup and hold times around the falling edge of ALE. Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the ^{t}DLW time.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold times for DLE.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative to V_{SS}/V_{SSQ} .... -1.0V to +7.0V
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1.5W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%; $V_{SS} = V_{SSQ}$, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1
Output Buffer Supply Voltage	5V TTL Compatible	V_{CCQ}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, $CE \ge V_{IH}$; V_{CC} = MAX Outputs Open f = MAX = $1/{}^tRC$	I_{CC}	150	250	mA	3
Power Supply Current: Standby	$CE \le V_{IL}$, $\overline{CE} \ge V_{IH}$; V_{CC} = MAX Outputs Open f = MAX = $1/{}^tRC$	I_{SB1}	50	80	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2V; $CE \le V_{SS}$ +0.2V V_{CC} = MAX; $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	5	15	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$	9	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = VccQ = 5V ±10%)

DESCRIPTION		-15		-17		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
ADDRESS LATCH											
Latch cycle time	^{t}LC	15		17		20		25		ns	
Latch HIGH time	^{t}LEH	5		5		5		5		ns	
Address/Chip Enable setup to latch LOW	^{t}LS	2		2		2		2		ns	
Address/Chip Enable hold from latch LOW	^{t}LH	3		3		3		3		ns	
Address/Chip Enable setup to latch HIGH	^{t}LHS	0		0		0		0		ns	
Latch HIGH to output active (Low-Z)	^{t}LZL	2		2		2		2		ns	6, 7, 4
Latch HIGH to output in High-Z	^{t}HZL	2	7	2	7	2	7	2	10	ns	6, 7, 4
READ CYCLE											
READ cycle time	^{t}RC	15		17		20		25		ns	
Address access time	^{t}AA		15		17		20		25	ns	
Chip Enable access time	^{t}ACE		15		17		20		25	ns	
Output hold from address change	^{t}OH	4		4		4		4		ns	
Chip Enable to output in Low-Z	^{t}LZCE	2		2		2		2		ns	6, 7, 4
Chip disable to output in High-Z	^{t}HZCE	2	7	2	7	2	7	2	10	ns	6, 7, 4
Output Enable access time	^{t}AOE		6		7		8		10	ns	
Output Enable to output in Low-Z	^{t}LZOE	0		0		0		0		ns	6, 7, 4
Output disable to output in High-Z	^{t}HZOE	2	6	2	7	2	8	2	10	ns	6, 7, 4
WRITE Cycle											
WRITE cycle time	^{t}WC	15		17		20		25		ns	
Chip Enable to end of write	^{t}CW	13		14		15		20		ns	
Address valid to end of write	^{t}AW	13		14		15		20		ns	
Address setup time	^{t}AS	0		0		0		0		ns	
Address hold from end of write	^{t}AH	0		0		0		0		ns	
WRITE pulse width	^{t}WP	13		14		15		20		ns	
Data setup time	^{t}DS	6		7		8		10		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
Write disable to output in Low-Z	^{t}LZWE	5		5		5		5		ns	6, 7, 4
Write Enable to output in High-Z	^{t}HZWE	0	8	0	8	0	10	0	10	ns	6, 7, 4
Byte Write Enable setup time	^{t}BWS	6		7		8		10		ns	
Byte Write Enable hold time	^{t}BWH	2		2		2		2		ns	
Byte Write disable setup time	^{t}BWDS	0		0		0		0		ns	
Data setup to DLE LOW	^{t}DLS	1		1		1		1		ns	9
Data hold from DLE LOW	^{t}DLH	3		3		3		3		ns	9
DLE HIGH to end of write	^{t}DLW	6		7		8		10		ns	8
End of write to DLE HIGH	^{t}WDLH	0		0		0		0		ns	9
End of write to ALE HIGH	^{t}WLH	0		0		0		0		ns	
ALE HIGH setup time to write enable LOW	^{t}LWS	0		0		0		0		ns	
ALE HIGH to end of write	^{t}LW	13		14		15		20		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

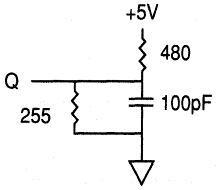


Fig. 1 OUTPUT LOAD EQUIVALENT

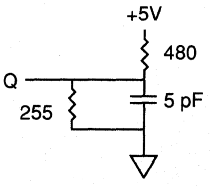
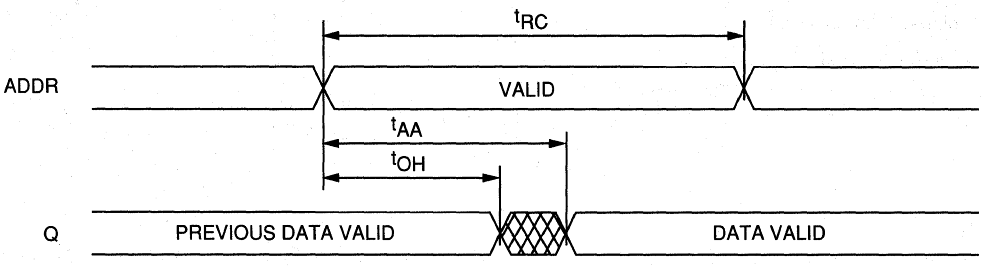


Fig. 2 OUTPUT LOAD EQUIVALENT

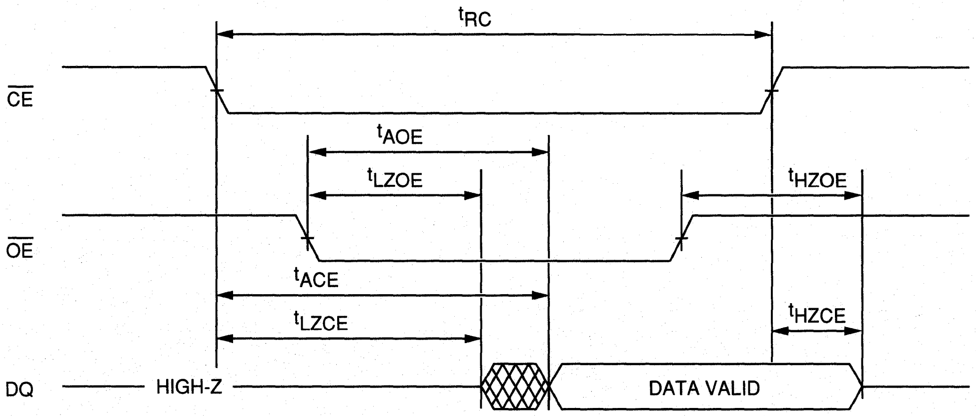
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZOE is less than ^{t}LZOE.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold time with respect to DLE.
10. Any combination of write enable ($\overline{\text{WE}}$) and chip enable ($\overline{\text{CE}}$) can initiate and terminate a WRITE cycle.
11. $\overline{\text{WE}}$ is HIGH for READ cycle.
12. Device is continuously selected. All chip enables are held in their active state.
13. Address valid prior to or coincident with the latest occurring chip enable.
14. CE timing is the same as $\overline{\text{CE}}$ timing. The wave form is inverted.
15. If output enable ($\overline{\text{OE}}$) is inactive (HIGH), the output will be in High-Z instead of undefined.

READ CYCLE NO. 1 [11, 12]



READ CYCLE NO. 2 [7, 11, 13, 14]

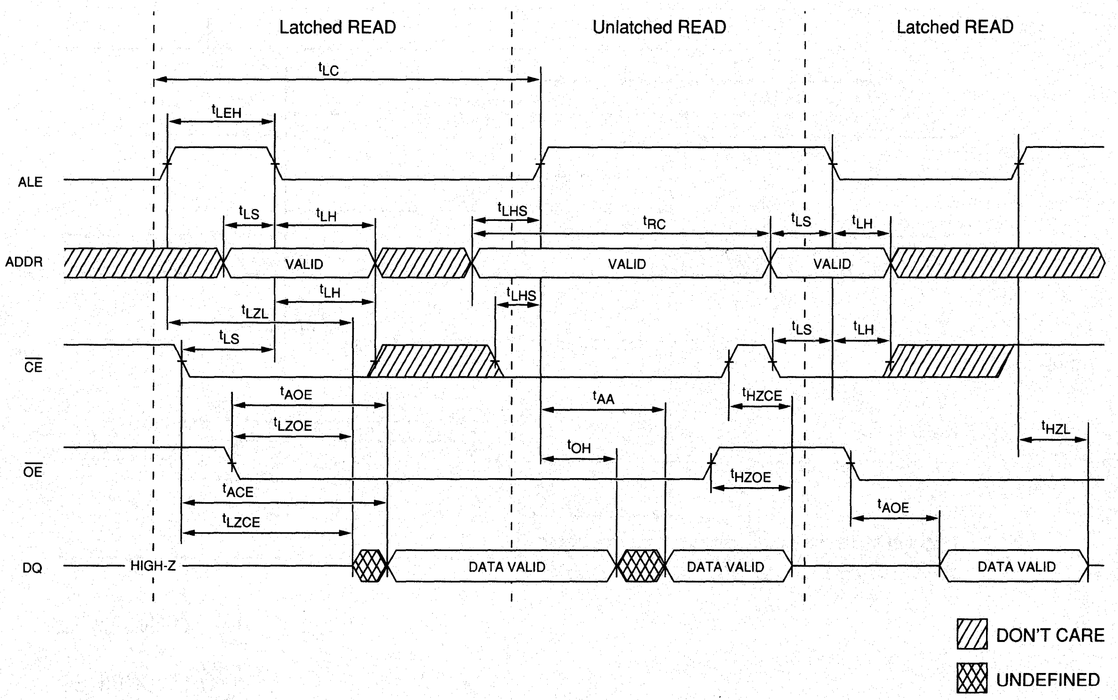


▨ DON'T CARE

▩ UNDEFINED

READ CYCLE NO. 3

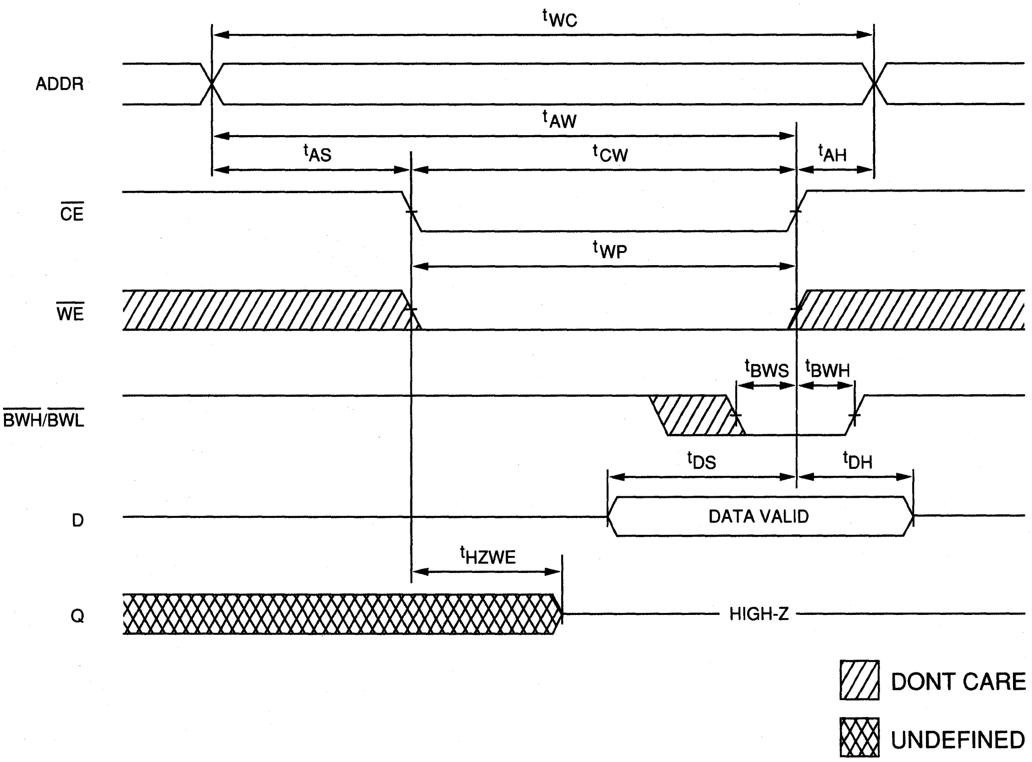
(ALE = DLE = HIGH) [7, 11, 14]



WRITE CYCLE NO. 1

Chip Enable Controlled

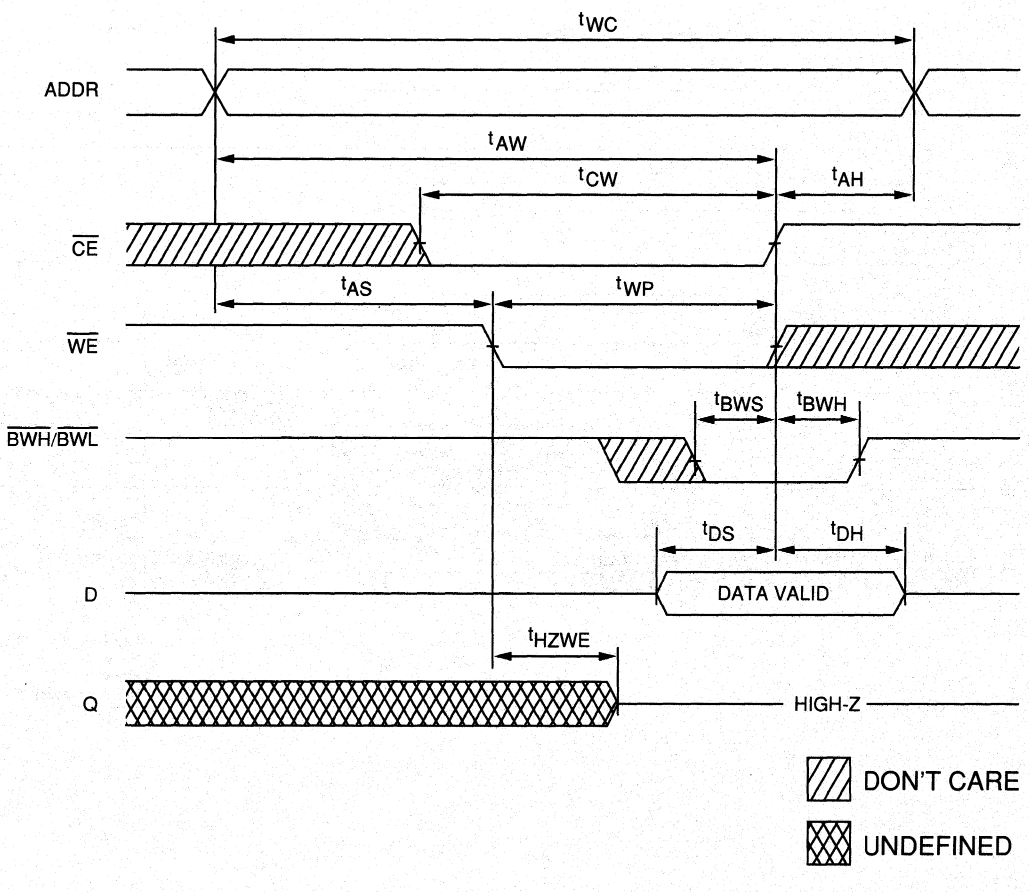
(ALE = DLE = HIGH)[10, 14, 15]



WRITE CYCLE NO. 2

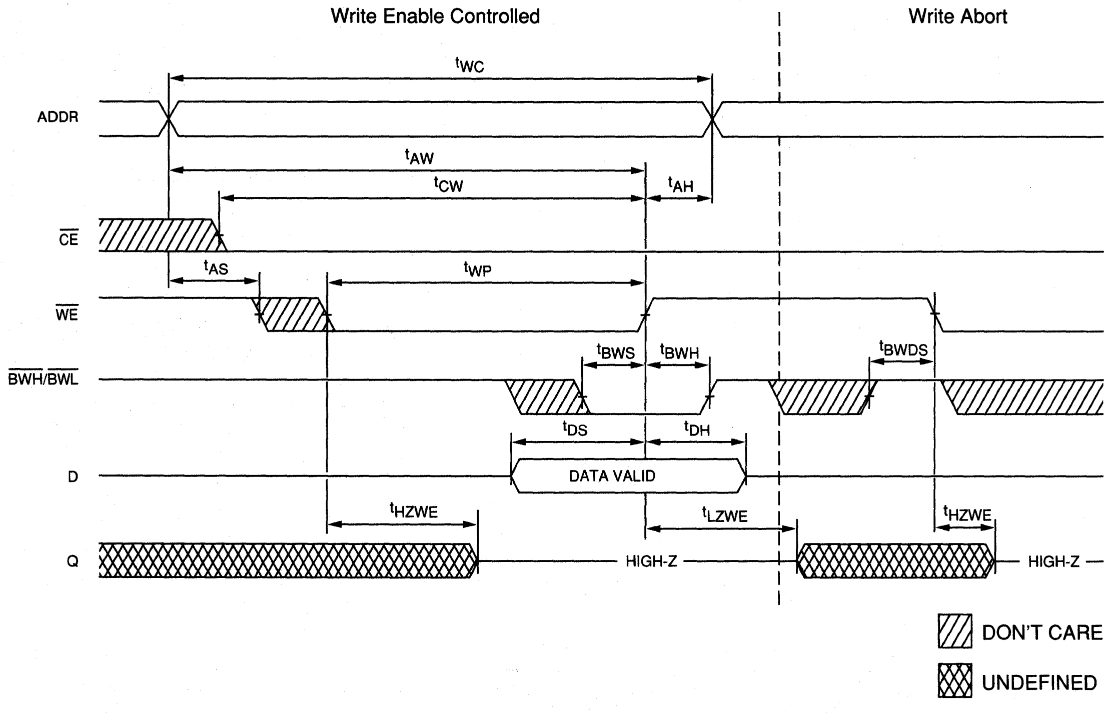
Write Enable Initiated/Chip Enable Terminated

(ALE = DLE = HIGH) [10, 14, 15]

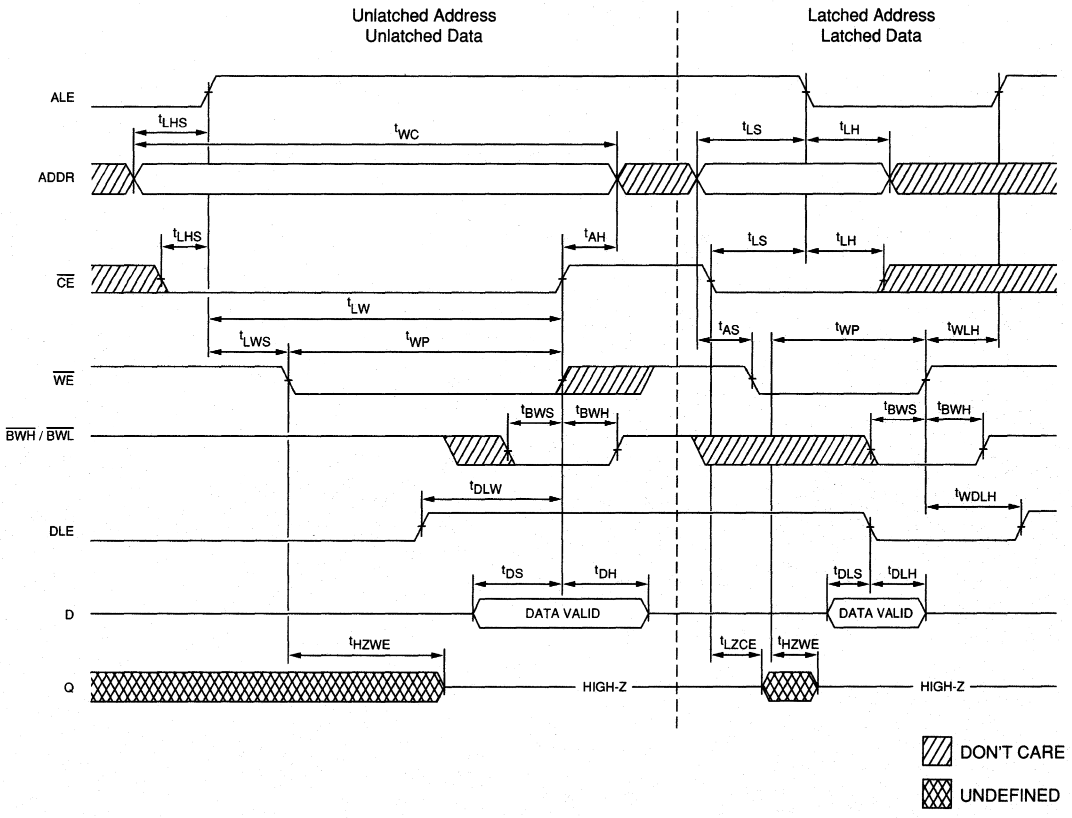


WRITE CYCLE NO. 3

(ALE = DLE = HIGH)[7, 10, 14, 15]



WRITE CYCLE NO. 4[7, 10, 14, 15]



FIFO MEMORIES PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Cycle Time (ns)	Package and Number of Pins			Process	Page
				PDIP	PLCC	SOJ		
512 x 9	Expandable Depth and Width	MT52C9005	15, 20, 25, 35	28	32	28	CMOS	5-1
512 x 9	Programmable Flag Expandable Depth and Width	MT52C9007	15, 20, 25, 35	28	32	28	CMOS	5-13
1K x 9	Expandable Depth and Width	MT52C9010	15, 20, 25, 35	28	32	28	CMOS	5-29
1K x 9	Programmable Flag Expandable Depth and Width	MT52C9012	15, 20, 25, 35	28	32	28	CMOS	5-41
2K x 9	Expandable Depth and Width	MT52C9020	15, 20, 25, 35	28	32	28	CMOS	5-57
2K x 9	Programmable Flag Expandable Depth and Width	MT52C9022	15, 20, 25, 35	28	32	28	CMOS	5-69

NOTE: Many Micron components are available in bare die form. Contact Micron Technology, Inc., for more information.

FIFO

512 x 9 FIFO

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (active)
- TTL compatible inputs and outputs
- Asynchronous READ and WRITE
- Empty, Half-Full and Full Flags
- Half-Full Flag in STAND ALONE mode
- Auto-retransmit capability
- Fully expandable by width and depth
- Pin and function compatible with higher density standard FIFOs

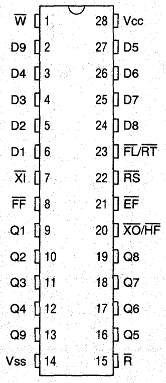
OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
PLCC	EJ
SOJ (300 mil)	DJ

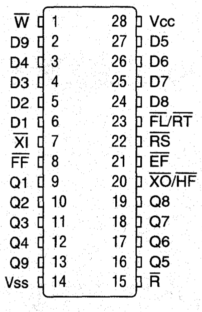
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***

PIN ASSIGNMENT (Top View)

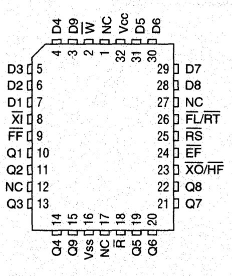
28-Pin DIP
(A-9, A-11)



28-Pin SOJ
(E-8)



32-Pin PLCC
(D-2)



GENERAL DESCRIPTION

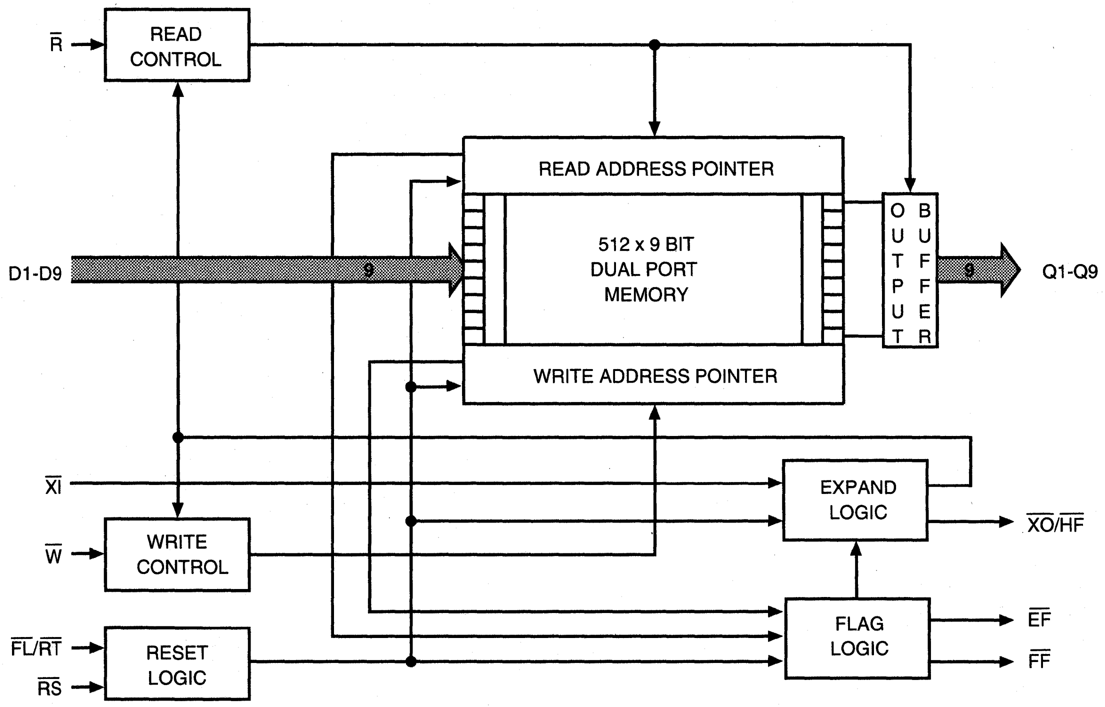
The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual port, six-transistor memory cell with resistor loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information can be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain in High-Z. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. Also, the MT52C9005 is speed, function and pin compatible with higher density FIFOs from Micron. This upward compatibility with 1K and 2K FIFOs provides a single-chip, depth-expansion solution.

FIFO

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1-D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1-Q9).
8	7	$\overline{XI}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$)of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$	Input	First Load: Acts as first load signal in DEPTH EXPANSION mode. $\overline{FL}$, if low, will enable the device as the first to be loaded (enables read and write pointers). $\overline{FL}$ should be tied LOW for the first FIFO in the chain, tied HIGH for all other FIFOs in the chain. Retransmit: Acts as retransmit signal in STAND ALONE mode. $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27 26, 25, 24, 2	D1-D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO}/\overline{HF}$	Output	Expansion Out: Acts as expansion out pin in DEPTH EXPANSION mode. $\overline{XO}$ will pulse LOW on the last physical WRITE or the last physical READ. $\overline{XO}$ should be connected to $\overline{XI}$ of the next FIFO in the daisy chain. Half-Full Flag: Acts as Half-Full Flag in STAND ALONE mode. $\overline{HF}$ goes LOW when the FIFO becomes more than Half-full; will stay LOW until the FIFO becomes Half-full or less.
10, 11, 13, 14, 19, 20, 21, 22, 15	9, 10, 11, 12, 16 17, 18, 19, 13	Q1-Q9	Output	Data Output: Output or High-Z.
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9005 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing the half-full flag, the $\overline{XO}/\overline{HF}$ pin will be shown as $(\overline{XO})/\overline{HF}$.*

RESET

After Vcc is stable, RESET $(\overline{RS})$ must be taken LOW to initialize the read and write pointers and flags. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is LOW. If $\overline{XI}$ is connected to $\overline{XO}$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe $(\overline{W})$ pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins are latched on the rising edge. If the location to be written is the last empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the STAND ALONE mode, $(\overline{XO})/\overline{HF}$ is asserted when the half-full-plus-one location (512/2 + 1) is written. It will stay asserted until the FIFO becomes half-full or less. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

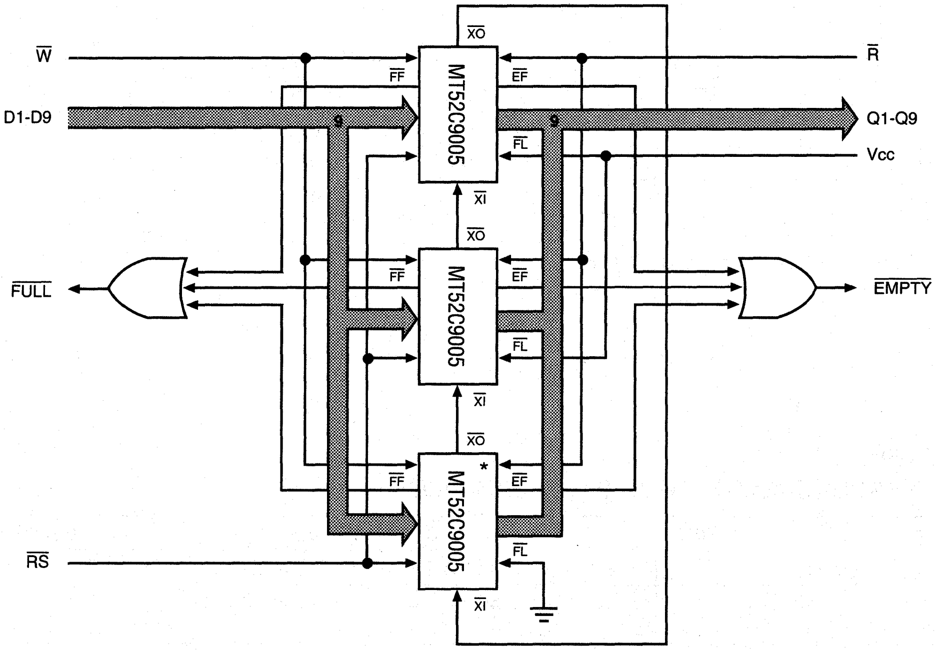
Information is read from the FIFO when the read strobe $(\overline{R})$ pin is taken LOW and the FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^{t}RLZ after the falling edge of $\overline{R}$ and valid data will appear ^{t}A after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is being used in the SINGLE DEVICE mode and the half-full-plus-one location is read, $(\overline{XO})/\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ LOW) and a read is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read to a FIFO will cause $\overline{XO}/\overline{HF}$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9005 allows the receiving device to request that the data read earlier from the FIFO to be repeated, when less than 512 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^{t}RTR after $(\overline{FL})/\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. FLOW-THROUGH READs are initiated from the rising edge of $\overline{W}$ and access time is measured from the rising edge of $\overline{EF}$.



* FIRST DEVICE LOADED

Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the stand alone or groups of expanded-depth mode FIFOs. Expanded-width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1) when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9005s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}/(\overline{HF})$ and $\overline{FL}/(\overline{RT})$. Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered during a RESET cycle, by tying the $\overline{XO}/(\overline{HF})$ pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}/(\overline{RT})$ pin grounded. The remaining devices in the chain will have $\overline{FL}/(\overline{RT})$ tied HIGH. During RESET cycle, $\overline{XO}/(\overline{HF})$ of each device is held HIGH, disabling reads and writes to all FIFOs, except the first load device. When the last physical location of the first device is written, the $\overline{XO}/(\overline{HF})$ pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9005. The writes will continue to go to the second device until last location WRITE. Then it will "pass" the write pointer to the third device.

The full condition of the entire FIFO array is signaled by "OR-ing" all the $\overline{FF}$ pins. On the last physical READ of the first device, its $\overline{XO}/(\overline{HF})$ will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. An empty condition is signaled by OR-ing all of the $\overline{EF}$ pins. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{\text{RS}}$	$\overline{\text{RT}}$	$\overline{\text{XI}}$	**Read Pointer**	**Write Pointer**	$\overline{\text{EF}}$	$\overline{\text{FF}}$	$\overline{\text{HF}}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{\text{RS}}$	$\overline{\text{FL}}$	$\overline{\text{XI}}$	**Read Pointer**	**Write Pointer**	$\overline{\text{EF}}$	$\overline{\text{FF}}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. $\overline{\text{XI}}$ is connected to $\overline{\text{XO}}$ of previous device.
$\overline{\text{RS}}$ = Reset Input, $\overline{\text{FL}}/\overline{\text{RT}}$/DIR= First Load/Retransmit, $\overline{\text{EF}}$ = Empty Flag Output, $\overline{\text{FF}}$ = Full Flag Output, $\overline{\text{XI}}$ = Expansion Input, $\overline{\text{HF}}$ = Half-Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -0.5V to +7.0V
Operating Temperature T_A (ambient) .... 0°C to 70°C
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R}$ ≤ V_{IL}; V_{CC} = MAX Outputs Open	I_{CC}	140	130	120	100	mA	3
Power Supply Current: Standby	W, $\overline{R}$ ≥ V_{IH}; V_{CC} = MAX	I_{SB1}	15	15	15	15	mA	
	$\overline{W}$, $\overline{R}$ ≥ V_{CC} -0.2; V_{CC} = MAX V_{IL} ≤ V_{SS} +0.2 V_{IH} ≥ V_{CC} -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	8	pF	4
Output Capacitance		C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Shift frequency	Fs		40		33.3		28.5		22.2	MHz	
Access time	^{t}A		15		20		25		35	ns	
READ cycle time	^{t}RC	25		30		35		45		ns	
READ recovery time	^{t}RR	10		10		10		10		ns	
READ pulse width	^{t}RPW	15		20		25		35		ns	6
READ LOW to Low-Z	^{t}RLZ	5		5		5		5		ns	
READ HIGH to High-Z	^{t}RHZ		15		15		18		20	ns	
Data hold from $\overline{\text{R}}$ HIGH	^{t}OH	5		5		5		5		ns	
WRITE cycle time	^{t}WC	25		30		35		45		ns	
WRITE pulse width	^{t}WPW	15		20		25		35		ns	6
WRITE recovery time	^{t}WR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^{t}WLZ	5		5		5		5		ns	5
Data setup time	^{t}DS	10		12		15		18		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
RESET cycle time	^{t}RSC	25		30		35		45		ns	
RESET pulse width	^{t}RSP	15		20		25		35		ns	6
RESET recovery time	^{t}RSR	10		10		10		10		ns	
READ HIGH to RESET HIGH	^{t}RRS	15		20		25		35		ns	
WRITE HIGH to RESET HIGH	^{t}WRS	15		20		25		35		ns	
RETRANSMIT cycle time	^{t}RTC	25		30		35		45		ns	
RETRANSMIT pulse width	^{t}RT	15		20		25		35		ns	
RETRANSMIT recovery time	^{t}RTR	10		10		10		12		ns	
RETRANSMIT setup time	^{t}RTS	15		20		25		35		ns	
RESET to $\overline{\text{AEF}}$, $\overline{\text{EF}}$ LOW	^{t}EFL		25		30		35		45	ns	
RESET to $\overline{\text{AEF}}$, $\overline{\text{HF}}$, $\overline{\text{FF}}$ HIGH	^{t}HFH, ^{t}FFH		25		30		35		45	ns	
READ LOW to $\overline{\text{EF}}$ LOW	^{t}REF		20		20		25		30	ns	
READ HIGH to $\overline{\text{FF}}$ HIGH	^{t}RFF		20		20		25		30	ns	
WRITE LOW to $\overline{\text{FF}}$ LOW	^{t}WFF		20		20		25		30	ns	
WRITE HIGH to $\overline{\text{EF}}$ HIGH	^{t}WEF		20		20		25		30	ns	
WRITE LOW to $\overline{\text{HF}}$ LOW	^{t}WHF		25		30		35		45	ns	
READ HIGH to $\overline{\text{HF}}$ HIGH	^{t}RHF		25		30		35		45	ns	
READ HIGH after $\overline{\text{EF}}$ HIGH	^{t}RPE	15		20		25		35		ns	5
WRITE HIGH after $\overline{\text{FF}}$ HIGH	^{t}WPF	15		20		25		35		ns	5
READ/WRITE to $\overline{\text{XO}}$ LOW	^{t}XOL		20		20		25		35	ns	
READ/WRITE to $\overline{\text{XO}}$ HIGH	^{t}XOH		20		20		25		35	ns	
$\overline{\text{XI}}$ pulse width	^{t}XIP	15		20		25		35		ns	
$\overline{\text{XI}}$ setup time	^{t}XIS	10		12		15		15		ns	
$\overline{\text{XI}}$ recovery time	^{t}XIR	10		10		10		10		ns	

NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Flow-through mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

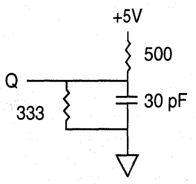
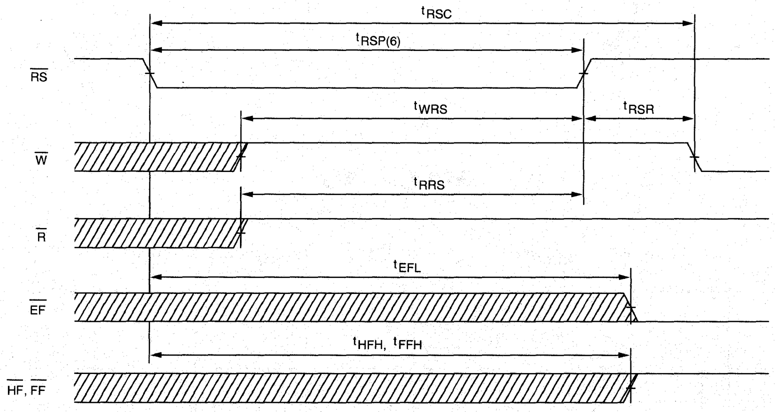
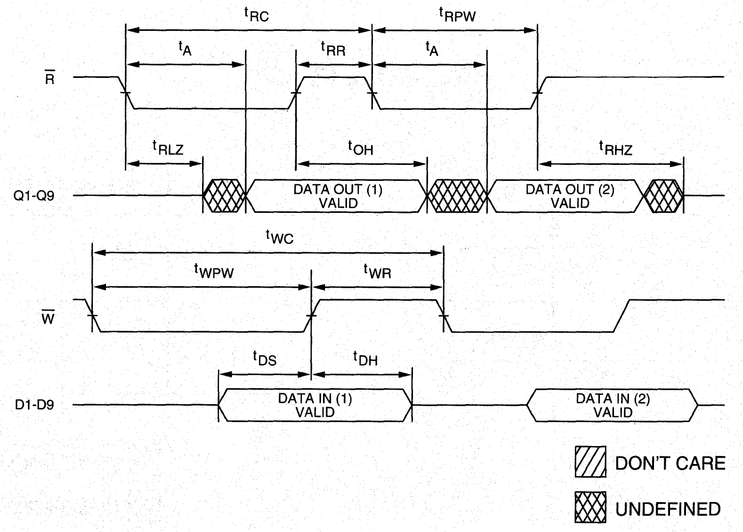


Fig. 2
OUTPUT LOAD EQUIVALENT

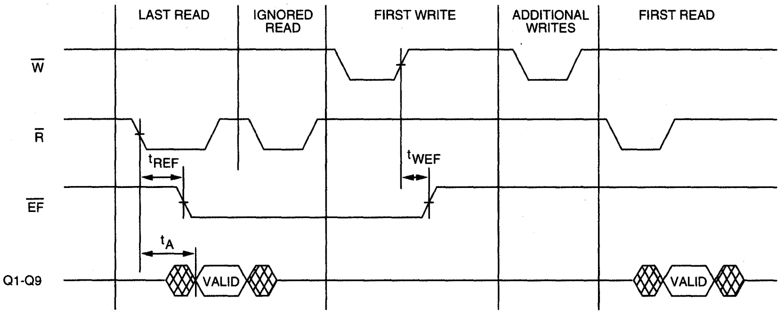
RESET



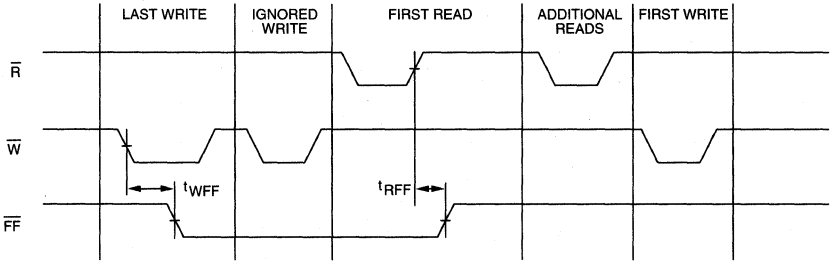
ASYNCHRONOUS READ AND WRITE



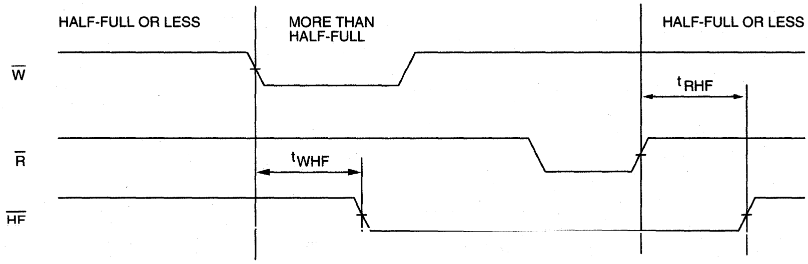
EMPTY FLAG



FULL FLAG



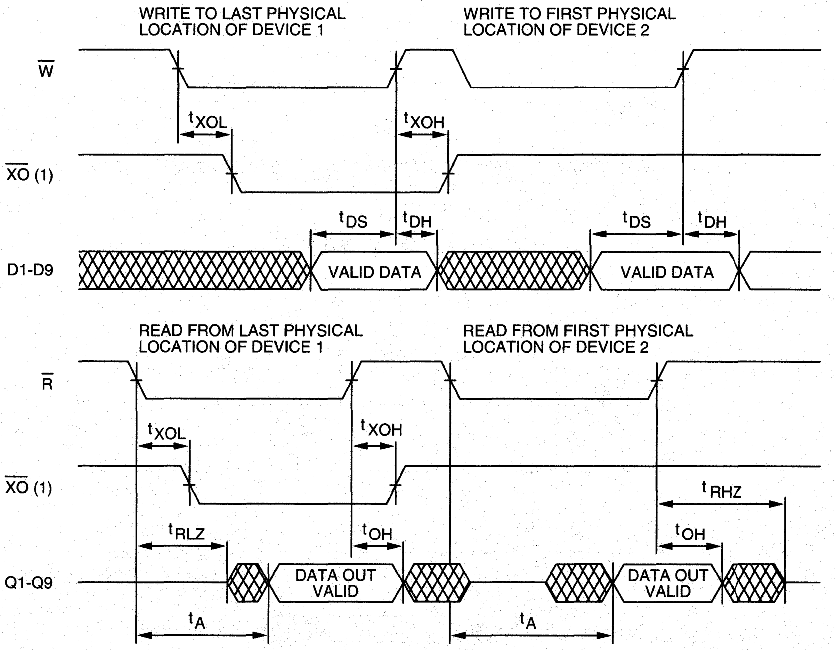
HALF-FULL FLAG



▨ DON'T CARE

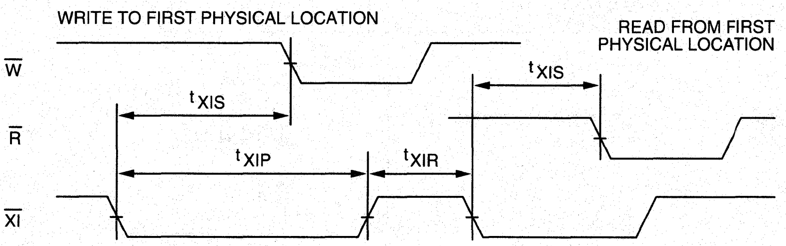
▩ UNDEFINED

EXPANSION MODE ($\overline{XO}$)



NOTE: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

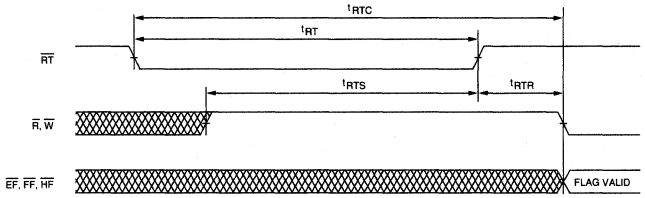
EXPANSION MODE ($\overline{XI}$)



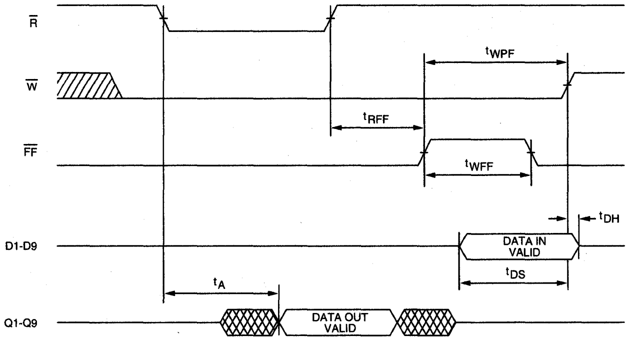
▨ DON'T CARE

▩ UNDEFINED

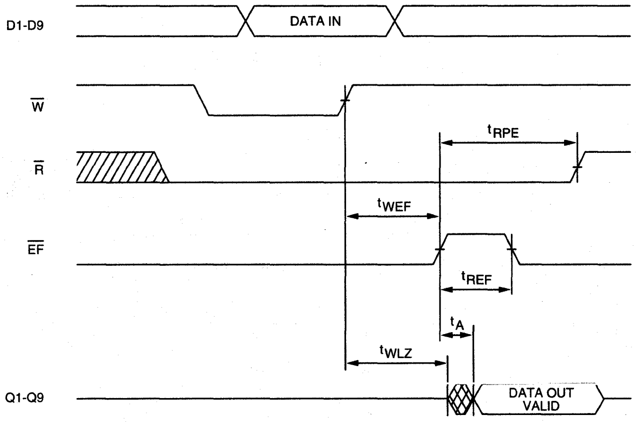
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



▨ DON'T CARE

▩ UNDEFINED

FIFO

512 x 9 FIFO

WITH PROGRAMMABLE FLAGS

FEATURES

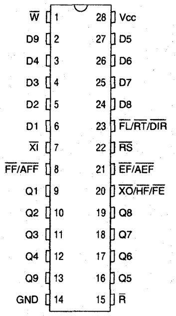
- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typical (standby); 350mW typical (active)
- TTL compatible inputs and outputs
- Asynchronous READ and WRITE
- Two fully configurable Almost-Full and Almost-Empty Flags
- Programmable Half-Full Flag or Full/Empty Flag option eliminates external counter requirement
- Register loading via the input or output pins
- Auto-retransmit capability in SINGLE DEVICE mode
- Fully expandable by width and depth
- Pin and function compatible with standard FIFOs

OPTIONS	MARKING
• Timing	
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
PLCC	EJ
Plastic SOJ	DJ

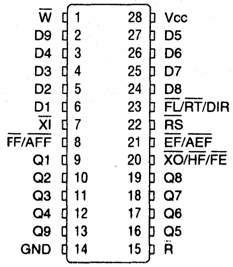
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***

PIN ASSIGNMENT (Top View)

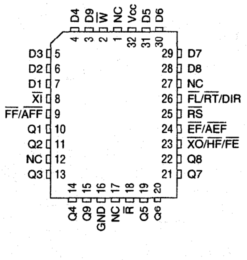
28-Pin DIP
(A-9, A-11)



28-Pin SOJ
(E-8)



32-Pin PLCC
(D-2)



GENERAL DESCRIPTION

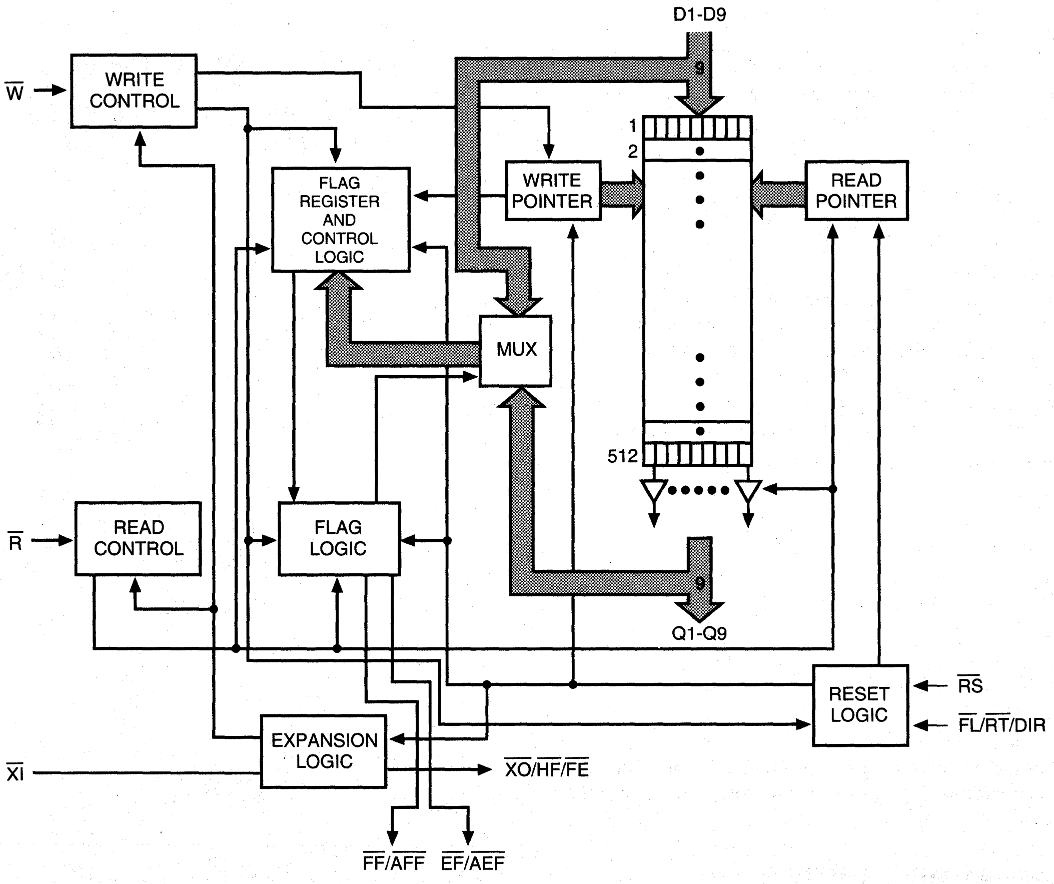
The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual-port, six-transistor memory cell with resistor loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates.

When not configured, the MT52C9007 defaults to a standard FIFO with empty ($\overline{EF}$), full ($\overline{FF}$) and half-full ($\overline{HF}$) flag pins. The MT52C9007 can be configured for programmable flags by loading the internal flag registers (as described under "Register Load Mode" on page 5-17). In configured mode, up to three flags are provided. The first two are the almost-empty flag ($\overline{AEF}$) and the almost-full flag ($\overline{AFF}$) with independently programmable offsets. The third one is either an $\overline{HF}$ or a full and empty ($\overline{FE}$) flag, depending on the bit configuration of the registers. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. Also, the MT52C9007 is speed, function and pin compatible with higher density FIFOs from Micron. This upward compatibility with 1K and 2K FIFOs provides a single-chip depth-expansion solution.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: This pin is used to reset the device and load internal flag registers. During device reset, all internal pointers and registers are cleared.
2	1	$\overline{W}$	Input	Write: A LOW on this pin loads data into the device. The internal write pointer is incremented after the rising edge of the write input.
18	15	$\overline{R}$	Input	Read: A LOW on this pin puts the oldest valid data byte in the memory array on the output bus. The internal read pointer is incremented at the rising edge of the read signal. Outputs are in High-Z when this pin is HIGH.
8	7	$\overline{XI}$	Input	Expansion-In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$)of the previous device in the daisy chain.
26	23	$\overline{FL/RT}$/DIR	Input	First Load/Retransmit/Direction: When in SINGLE DEVICE mode, this pin can be used to initiate a reread of the previously read data. When in REGISTER LOAD mode, the pin is used for register loading direction. When it is LOW, registers are loaded through the data output pins. When it is HIGH, registers are loaded through the data input pins. In DEPTH EXPANSION mode, this pin should be tied LOW if the device is the first one in the chain and tied HIGH if it is not the first one.
7, 6, 5, 4, 31, 30 29, 28, 3	6, 5, 4, 3, 27 26, 25, 24, 2	D1-D9	Input	Data Inputs: Data on these lines are stored in the memory array or flag registers during array WRITE or register programming, respectively.
24	21	$\overline{EF/AEF}$	Output	Empty Flag/Almost-Empty Flag: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is an Empty Flag output. When in CONFIGURED mode, it is an Almost-Empty Flag output. This pin is active LOW.
9	8	$\overline{FF/AFF}$	Output	Full Flag/Almost-Full Flags: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is a Full Flag output. When in CONFIGURED mode, it is an Almost-Full Flag output. This pin is active LOW.
23	20	$\overline{XO/HF/FE}$	Output	Expansion Out/Half Full/Full/Empty: This pin's function is determined by its operation mode. When in SINGLE DEVICE mode, this pin is either HF Flag or a Full/Empty Flag, depending on the state of the most significant bit of Almost-Full Flag Register. The pin is an $\overline{XO}$ output when the part is in DEPTH EXPANSION mode. This pin defaults to $\overline{XO/HF}$ in NONCONFIGURED mode.
10, 11, 13, 14 19, 20, 21, 22,15	9, 10, 11, 12, 16 17, 18, 19, 13	Q1-Q9	I/O	Data Output: These pins may be used for data retrieval. The pins become inputs during register loading with DIR input HIGH. The outputs are disabled (High-Z) during device idle ($\overline{R}$ = HIGH).
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	GND	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9007 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For multiple-function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing half-full flags, the* $\overline{\text{XO}}/\overline{\text{HF}}/\overline{\text{FE}}$ *pin will be shown as* $(\overline{\text{XO}})/\overline{\text{HF}}/(\overline{\text{FE}})$.

RESET

After Vcc is stable, Reset ($\overline{\text{RS}}$) must be taken LOW with both $\overline{\text{R}}$ and $\overline{\text{W}}$ HIGH to initialize the read and write pointers and flags. This also clears all internal registers. During the reset pulse, the state of the $\overline{\text{XI}}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{\text{XI}}$ is tied LOW. If $\overline{\text{XI}}$ is connected to $\overline{\text{XO}}/(\overline{\text{HF}})$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{\text{W}}$) pin is taken LOW and the FIFO is not full. The WRITE cycle is initiated by the falling edge of $\overline{\text{W}}$. Data on the D1-D9 pins are latched on the rising edge. If the location to be written is the last empty location in the FIFO, $\overline{\text{FF}}$ will be asserted (LOW) after the falling edge of $\overline{\text{W}}$. While the $\overline{\text{FF}}$ is asserted, all writes are inhibited and previously stored data are unaffected. The first WRITE to an empty FIFO will cause $\overline{\text{EF}}$ to go HIGH after the rising edge of $\overline{\text{W}}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{\text{XO}}/(\overline{\text{HF}})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{\text{R}}$) pin is taken LOW and FIFO is not empty ($\overline{\text{EF}}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^{t}RLZ after the falling edge of $\overline{\text{R}}$. Valid data will appear ^{t}A after the falling edge of $\overline{\text{R}}$. After the last available data word is read, $\overline{\text{EF}}$ will go LOW upon the falling edge of $\overline{\text{R}}$. While the $\overline{\text{EF}}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is full and a READ is initiated, the $\overline{\text{FF}}$ will go HIGH after the rising edge of $\overline{\text{R}}$. When operating in the expanded mode, the last location read from a FIFO will cause $\overline{\text{XO}}/(\overline{\text{HF}})$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9007 allows the receiving device to request that data just read from the FIFO be repeated, when less than 512 writes have been performed between resets. When the $(\overline{\text{FL}})/\overline{\text{RT}}/(\text{DIR})$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may start reading the data from the beginning of the FIFO ^{t}RTR after $(\overline{\text{FL}})/\overline{\text{RT}}/(\text{DIR})$ is taken HIGH. Some or all flags may be affected depending on the location of the read and write pointers before and after the retransmit.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{\text{W}}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{\text{R}}$. When the FIFO is empty, a flow-through READ can be done by holding $\overline{\text{R}}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{\text{W}}$, and access time is measured from the rising edge of the empty flag.

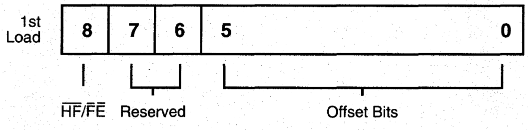
REGISTER LOAD MODE

This mode of operation is used to reset the device and program the internal flag registers. This yields an almost full and an almost-empty flag (DIP package pins 8 and 21 respectively) and a half-full or F/$\overline{E}$ flag (DIP package pin 20).

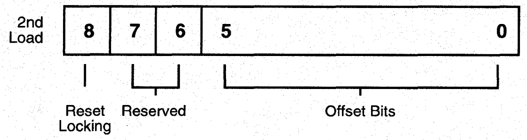
Two 9-bit internal registers have been provided for flag configuration. One is the almost-full flag register (AFFR) and the other is the almost-empty flag register (AEFR). Bit configurations of the two registers are shown below.

REGISTER SET FOR MT52C9007

Almost Full Flag Register (AFFR)



Almost Empty Flag Register (AEFR)



Note that bits 0-5 are used for offset setting. The offset value ranges from 1 to 63 words. Each offset value corresponds to a 2-byte increment. This provides a maximum offset of 126 bytes.

Bits 6 and 7 are reserved for future offset expansion. Bit 8 of the AFFR is used for configuration of $\overline{HF}/\overline{FE}$ pin. When this bit is set LOW, the HF/$\overline{FE}$ pin is configured as an $\overline{HF}$ flag output. When it is set HIGH, the HF/$\overline{FE}$ is configured as an F/$\overline{E}$ flag output.

Bit 8 of the AEFR is used for reset locking. When this bit is set LOW, subsequent device RESET or REGISTER LOADING cycles reset the device. When the bit is programmed HIGH, subsequent RESET cycles are ignored. In this mode, the flag registers may be reconfigured without device reset. The part may be reset by cycling power to the device or by writing zero (0) into bit 8 of the AEFR register followed by a DEVICE RESET or REGISTER LOAD.

Flag registers are loaded by bringing $\overline{RS}$ LOW followed by the $\overline{R}$ input. The $\overline{R}$ pin should be brought LOW ^{t}RS after the $\overline{RS}$ becomes LOW. The registers may be loaded via the input pins or the output pins depending on the status of the DIR control input. Data is latched into the registers at the rising edge of the $\overline{W}$ control pin. The first WRITE loads the AFFR while the second WRITE loads the AEFR. This loading order is fixed.

BIDIRECTIONAL MODE

Applications requiring data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by using two MT52C9007s. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both depth expansion and width expansion may be used in this mode.

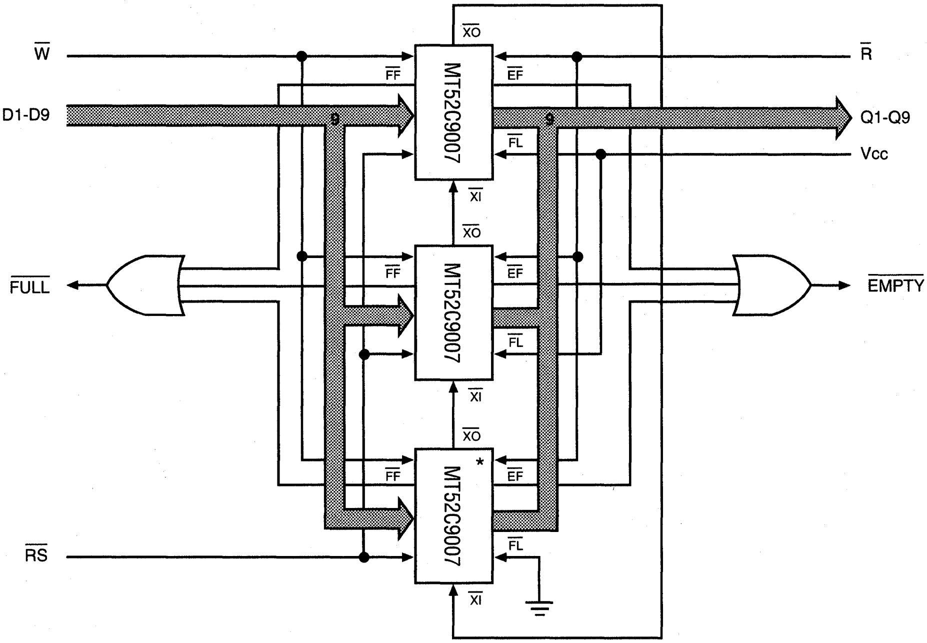
FLAG TIMING

A total of three flag outputs are provided in either CONFIGURED or NONCONFIGURED mode. In the NONCONFIGURED mode, the three flags are $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$. The $\overline{HF}$ flag goes active when more than half the FIFO is full. The flag goes inactive when the FIFO is half full or less.

The full and empty flags are asserted when the last byte is written to or read out of the FIFO, respectively. They are deasserted when the first byte is loaded into an empty FIFO or read out of a full FIFO, respectively. All three flag outputs are active LOW.

When the device is programmed, the $\overline{AFF}$ and $\overline{AEF}$ go active after a READ/WRITE cycle initiation of the location corresponding to the programmed offset value. For example, if the AEFR is programmed with a 10-byte offset (loading a Hex value of 05), the $\overline{AEF}$ flag goes active while reading the 10th location before the FIFO is empty. The flag goes inactive when there are 10 or more bytes left in the FIFO. The assertion timing and deassertion timing of the $\overline{AFF}$ are the same.

The third flag in the PROGRAM mode is either $\overline{HF}$ or F/$\overline{E}$ flag depending on the state of the highest bit of the AFFR. If the device is programmed for $\overline{HF}$ flag, it functions like the $\overline{HF}$ flag in NONPROGRAMMED mode. If the device is configured for F/$\overline{E}$ flag, the pin will be active (LOW) when the FIFO is either empty or full. The condition of the FIFO is determined by the state of F/$\overline{E}$ together with states of $\overline{AFF}$ and $\overline{AEF}$ (example: if F/$\overline{E}$ is LOW and $\overline{AFF}$ is LOW but $\overline{AEF}$ is HIGH, the FIFO is full).



* FIRST DEVICE LOADED

Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9007s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) and $\overline{FL}$/($\overline{RT}$/DIR). Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered by tying the $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$/($\overline{RT}$/DIR) pin grounded. The remaining devices in the chain will have $\overline{FL}$/($\overline{RT}$/DIR) tied HIGH. Upon a reset, reads and writes to all FIFOs are disabled, except the first load device. When the last physical location of the first device is written, the $\overline{XO}$/($\overline{HF}$) pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9007. The writes will continue to go to the second device until last location write. Then it will "pass" the write pointer to the third device. The full condition of the entire FIFO array is signaled when all the $\overline{FF}$/($\overline{AFF}$) pins are LOW.

On the last physical READ of the first device, its $\overline{XO}$ ($\overline{HF}$) will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. On the last READ, an empty condition is signaled by all of the $\overline{EF}$ pins being LOW. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	**Read Pointer**	**Write Pointer**	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	**Read Pointer**	**Write Pointer**	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$/DIR = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -0.5V to +7.0V
Operating Temperature T_A (ambient) .... 0°C to 70°C
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ᵗRC Outputs Open	Icc	140	130	120	100	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ᵗRC	I_{SB1}	15	15	15	15	mA	
	$\overline{W}$, $\overline{R}$ ≥ Vcc -0.2; Vcc = MAX V_{IL} ≤ Vss +0.2 V_{IH} ≥ Vcc -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

(V_{IN} = 0V; V_{OUT} = 0V)

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz	C_I	8	pF	4
Output Capacitance	Vcc = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured and nonconfigured modes) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ CYCLE											
Shift frequency	^{t}RF		40		33.3		28.5		22.2	MHz	
READ cycle time	^{t}RC	25		30		35		45		ns	
Access time	^{t}A		15		20		25		35	ns	6
READ recovery time	^{t}RR	10		10		10		10		ns	
READ pulse width	^{t}RPW	15		20		25		35		ns	
READ LOW to Low-Z	^{t}RLZ	5		5		5		5		ns	7
READ HIGH to High-Z	^{t}RHZ		15		15		18		20	ns	7
Data HOLD from $\overline{R}$ HIGH	^{t}OH	5		5		5		5		ns	
WRITE CYCLE											
WRITE cycle time	^{t}WC	25		30		35		45		ns	
WRITE pulse width	^{t}WPW	15		20		25		35		ns	6
WRITE recovery time	^{t}WR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^{t}WLZ	5		5		5		5		ns	5, 7
Data setup time	^{t}DS	10		12		15		18		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
RETRANSMIT CYCLE											
RESTRANSMIT cycle time	^{t}RTC	25		30		35		45		ns	
RESTRANSMIT pulse width	^{t}RT	15		20		25		35		ns	
RESTRANSMIT recovery time	^{t}RTR	10		10		10		12		ns	
RESTRANSMIT setup time	^{t}RTS	15		20		25		35		ns	
RESET CYCLE											
RESET cycle time (no register programming)	^{t}RSC	25		30		35		45		ns	
RESET pulse width	^{t}RSP	15		20		25		35		ns	6
RESET recovery time	^{t}RSR	10		10		10		10		ns	
$\overline{RS}$ LOW to $\overline{R}$ LOW	^{t}RS	15		20		25		35		ns	
RESET and register programming cycle time	^{t}RSPC	85		100		115		145		ns	
$\overline{R}$ LOW to DIR valid (register load cycle)	^{t}RDV	5		5		5		5		ns	
$\overline{R}$ LOW to register load	^{t}RW	10		10		10		10		ns	
$\overline{W}$ HIGH to $\overline{RS}$ LOW	^{t}WRS	0		0		0		0		ns	
$\overline{R}$ HIGH to $\overline{RS}$ LOW	^{t}RRS	0		0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured mode only) (T_A = 0°C to 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Mode Timing											
$\overline{R/W}$ to $\overline{XO}$ LOW	^{t}XOL		20		20		25		35	ns	
$\overline{R/W}$ to $\overline{XO}$ HIGH	^{t}XOH		20		20		25		35	ns	
$\overline{XI}$ pulse width	^{t}XIP	15		20		25		35		ns	
$\overline{XI}$ setup time to $\overline{R/W}$	^{t}XIS	10		12		15		15		ns	
$\overline{XI}$ recovery time	^{t}XIR	10		10		10		10		ns	
Flags Timing											
$\overline{W}$ HIGH to Flags Valid	^{t}WFV		15		15		15		15	ns	
$\overline{RS}$ to $\overline{AEF}$, $\overline{EF}$ LOW	^{t}EFL		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{EF}$ LOW	^{t}REF		20		20		25		30	ns	
$\overline{W}$ HIGH to $\overline{EF}$ HIGH	^{t}WEF		20		20		25		30	ns	
$\overline{R}$ HIGH after $\overline{EF}$ HIGH	^{t}RPE	15		20		25		35		ns	5
$\overline{RS}$ to $\overline{AFF}$, $\overline{HF}$, $\overline{FF}$ HIGH	^{t}HFH, ^{t}FFH		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{FF}$ HIGH	^{t}RFF		15		20		25		30	ns	
$\overline{W}$ LOW to $\overline{FF}$ LOW	^{t}WFF		20		20		25		30	ns	
$\overline{W}$ HIGH after $\overline{FF}$ HIGH	^{t}WPF	15		20		25		35		ns	5
$\overline{W}$ LOW to $\overline{HF}$ LOW	^{t}WHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{HF}$ HIGH	^{t}RHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{AFF}$ HIGH	^{t}RAFF		25		30		35		45	ns	
$\overline{W}$ LOW to $\overline{AFF}$ LOW	^{t}WAFF		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{AEF}$ LOW	^{t}RAEF		25		30		35		45	ns	
$\overline{W}$ HIGH to $\overline{AEF}$ HIGH	^{t}WAEF		25		30		35		45	ns	

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

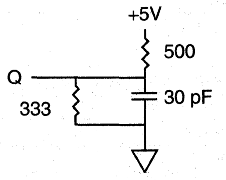
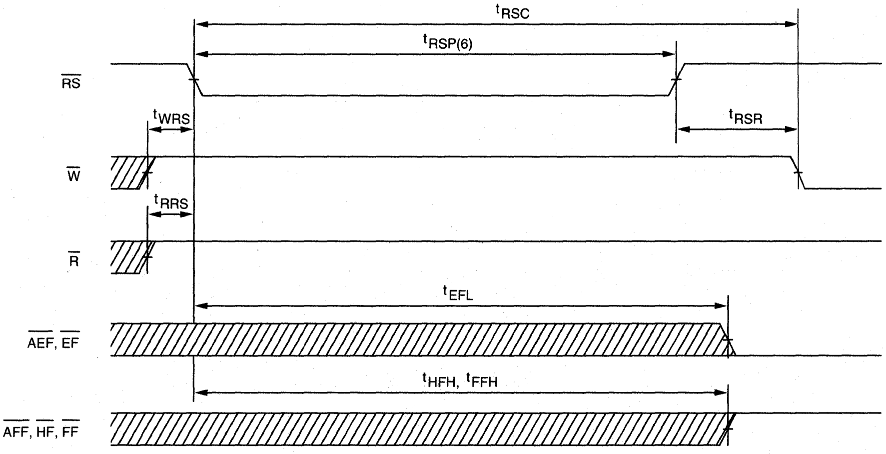


Figure 2
OUTPUT LOAD EQUIVALENT

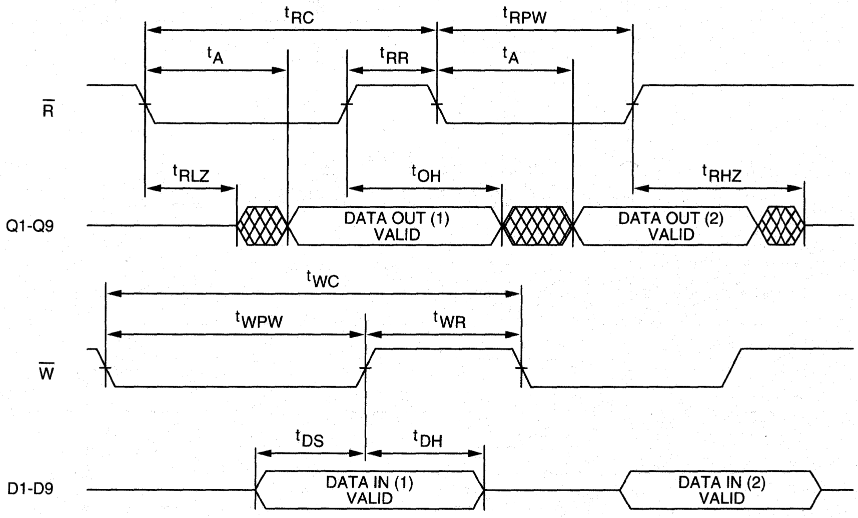
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.
7. Values guaranteed by design, not currently tested.
8. $\overline{R}$ and DIR signals must go inactive (HIGH) coincident with $\overline{RS}$ going inactive (HIGH).
9. DIR must become valid before $\overline{W}$ goes active (LOW).

RESET
(WITH NO REGISTER PROGRAMMING)



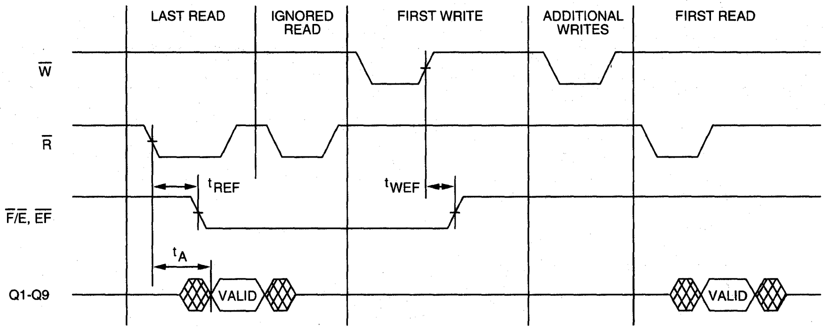
ASYNCHRONOUS READ AND WRITE



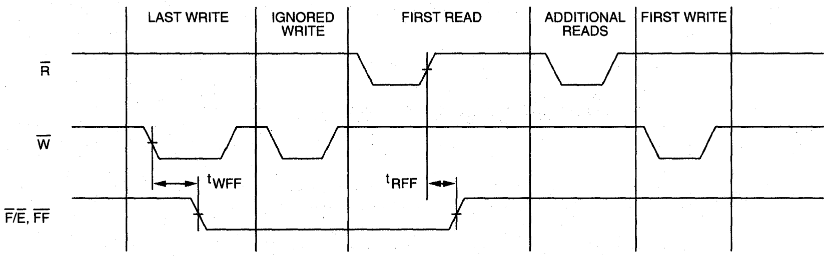
▨ DON'T CARE

▩ UNDEFINED

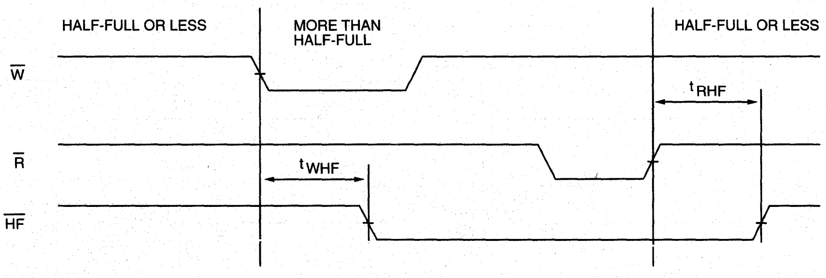
EMPTY FLAG



FULL FLAG



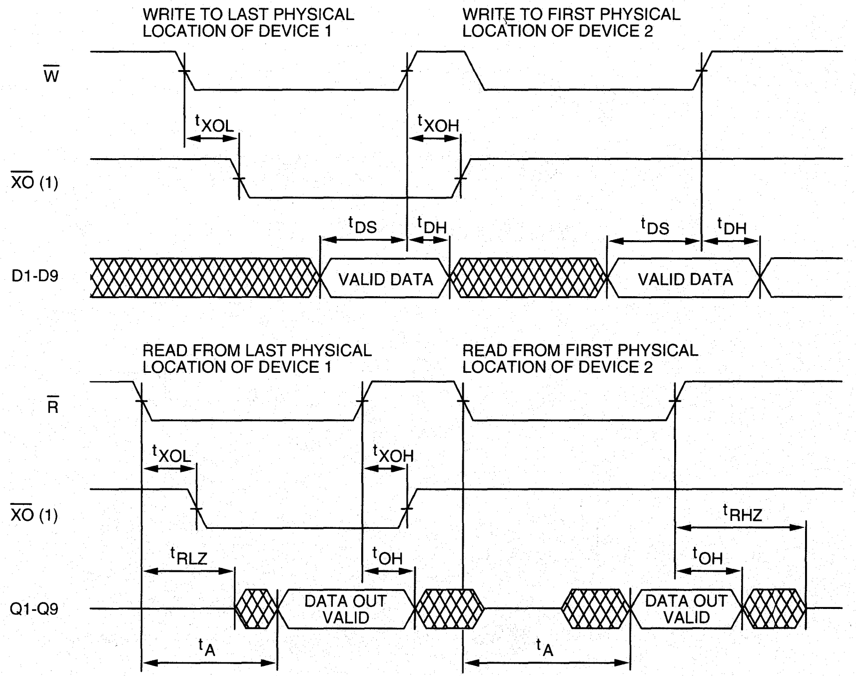
HALF-FULL FLAG
(FOR CONFIGURED AND NONCONFIGURED MODES)



▨ DON'T CARE

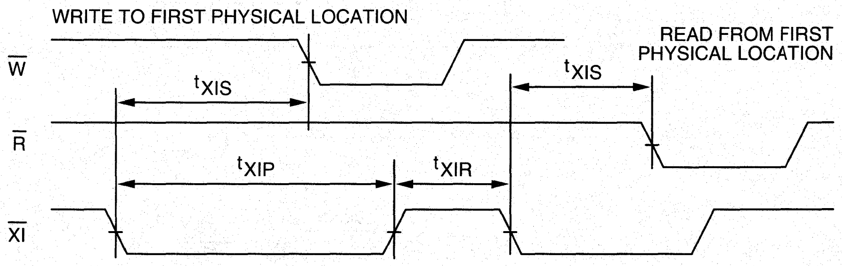
▩ UNDEFINED

EXPANSION MODE ($\overline{XO}$)



NOTE: 1. $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)



▨ DON'T CARE

▩ UNDEFINED

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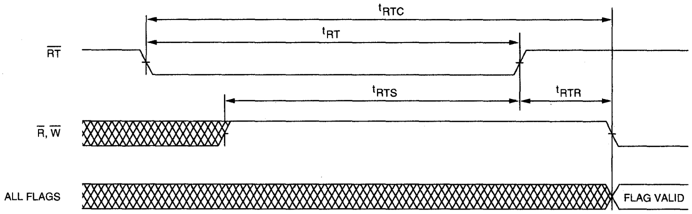
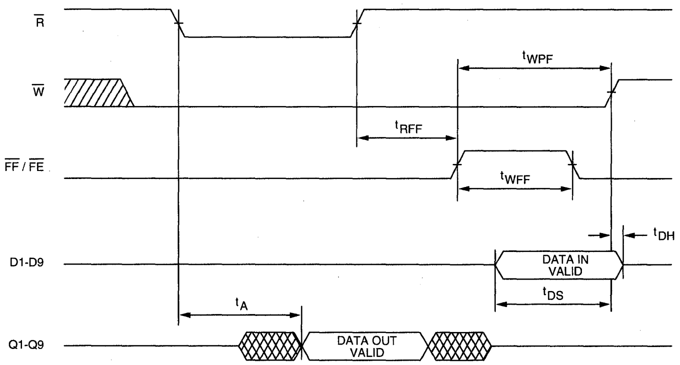
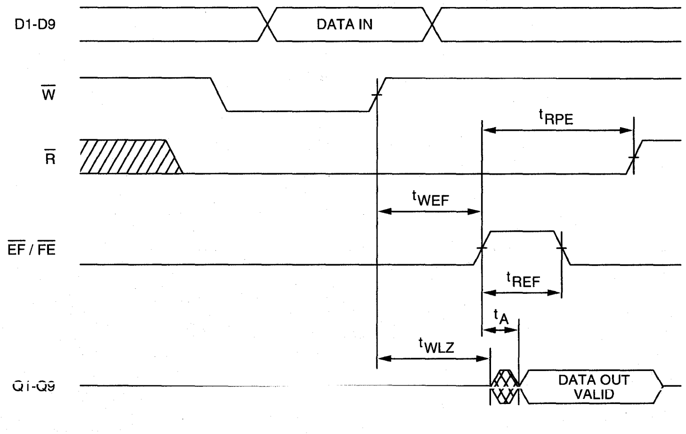
RETRANSMIT



WRITE FLOW-THROUGH



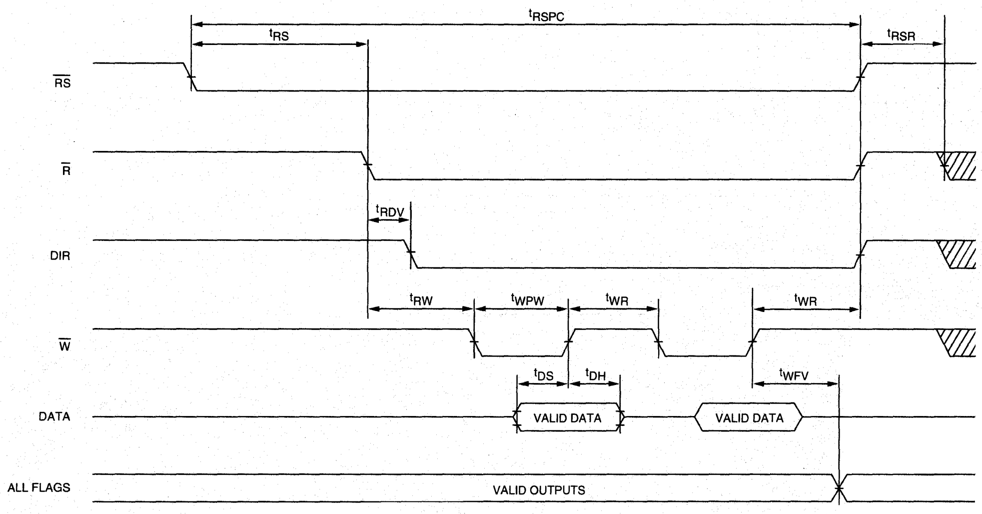
READ FLOW-THROUGH



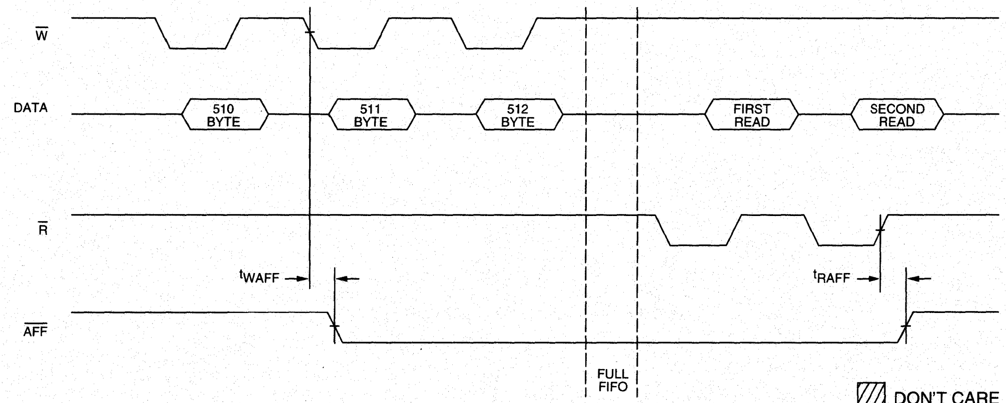
▨ DON'T CARE

▦ UNDEFINED

RESET/REGISTER PROGRAMMING CYCLE TIME[8, 9]



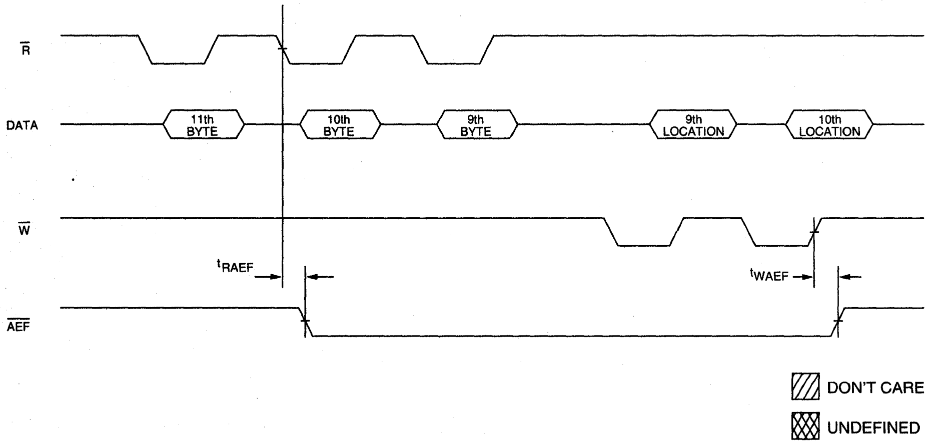
ALMOST-FULL FLAG (2-BYTE OFFSET)



▨ DON'T CARE

▩ UNDEFINED

ALMOST-EMPTY FLAG (10-BYTE OFFSET)



ADVANCE

MICRON TECHNOLOGY, INC.

MT52C9010

FIFO

1K x 9 FIFO

FEATURES

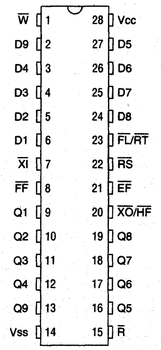
- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (active)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Half-Full Flag capability in STAND ALONE mode
- Auto-retransmit capability
- Fully expandable by width and depth
- Pin and function compatible with higher density standard FIFOs

OPTIONS	MARKING
• Timing	
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
PLCC	EJ
SOJ (300 mil)	DJ

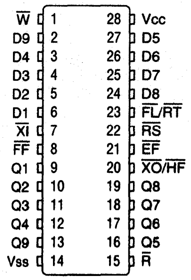
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***

PIN ASSIGNMENT (Top View)

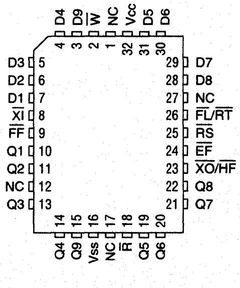
28-Pin DIP
(A-9, A-11)



28-Pin SOJ
(E-8)



32-Pin PLCC
(D-2)



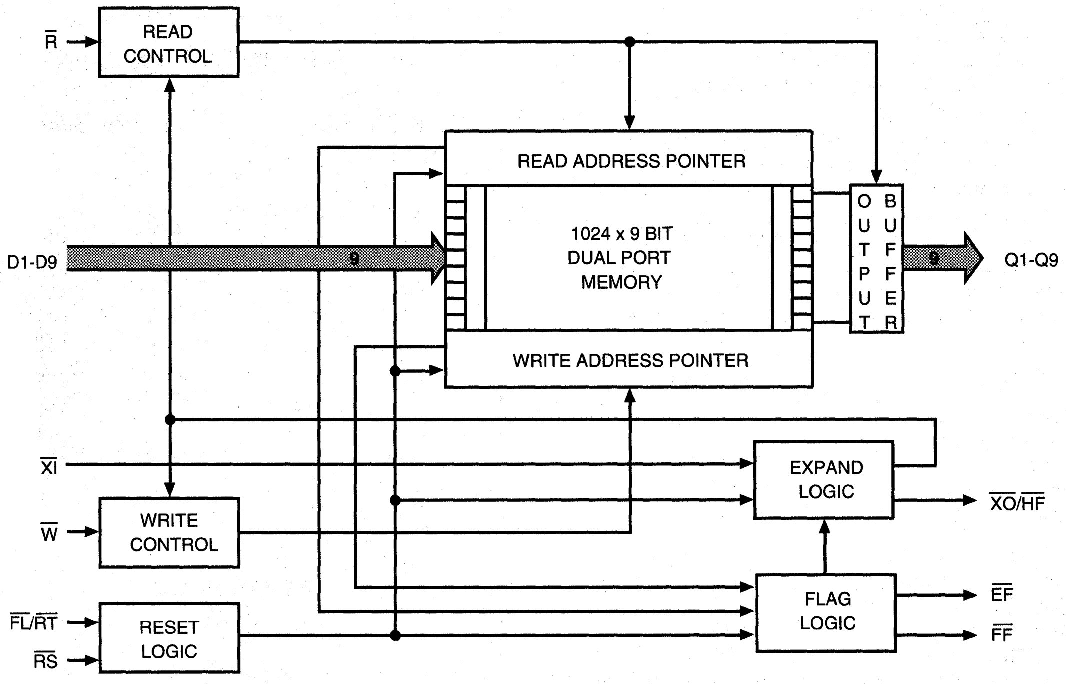
GENERAL DESCRIPTION

The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual port, six-transistor memory cell with resistor loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information can be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain in High-Z. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. Also, the MT52C9010 is speed, function and pin compatible with higher density FIFOs from Micron. This upward compatibility with the 2K x 9 FIFO provides a single-chip, depth-expansion solution.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1-D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1-Q9).
8	7	$\overline{XI}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$)of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$	Input	First Load: Acts as first load signal in DEPTH EXPANSION mode. $\overline{FL}$ if low, will enable the device as the first to be loaded (enables read and write pointers). $\overline{FL}$ should be tied low for the first FIFO in the chain, tied HIGH for all other FIFOs in the chain. Retransmit: Acts as retransmit signal in STAND ALONE mode. $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27 26, 25, 24, 2	D1-D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO}/\overline{HF}$	Output	Expansion Out: Acts as expansion out pin in DEPTH EXPANSION mode. $\overline{XO}$ will pulse LOW on the last physical WRITE or the last physical read. $\overline{XO}$ should be connected to $\overline{XI}$ of the next FIFO in the daisy chain. Half-Full Flag: Acts as Half-Full Flag in STAND ALONE mode. $\overline{HF}$ goes LOW when the FIFO becomes more than half-full; will stay LOW until the FIFO becomes half-full or less.
10, 11, 13, 14, 19, 20, 21, 22, 15	9, 10, 11, 12, 16 17, 18, 19, 13	Q1-Q9	Output	Data Output: Output or High-Z.
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9010 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing the half-full flags, the $\overline{XO}/\overline{HF}$ pin will be shown as ($\overline{XO}$)/$\overline{HF}$.*

RESET

After Vcc is stable, RESET ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is LOW. If $\overline{XI}$ is tied to $\overline{XO}$/($\overline{HF}$) of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins are latched on the rising edge. If the location to be written is the last empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the STAND ALONE mode, ($\overline{XO}$)/$\overline{HF}$ is asserted when the half-full-plus-one location (1024/2 + 1) is written. It will stay asserted until the FIFO becomes half-full or less. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, write to the last location of the FIFO will cause $\overline{XO}$/($\overline{HF}$) to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

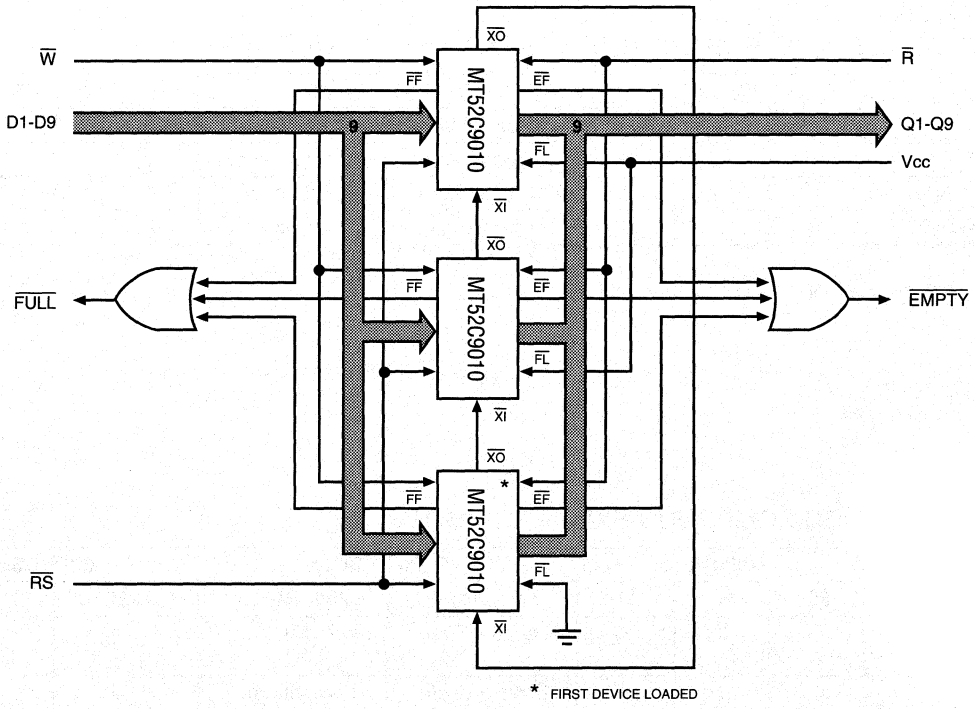
Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and the FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^tRLZ after the falling edge of $\overline{R}$ and valid data will appear ^tA after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is being used in the SINGLE DEVICE mode and the half-full-plus-one location is read, ($\overline{XO}$)/$\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ LOW) and a read is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read to a FIFO will cause $\overline{XO}$/($\overline{HF}$) to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9010 allows the receiving device to request that the data read earlier from the FIFO to be repeated, when less than 1024 writes have been performed between resets. When the ($\overline{FL}$)/$\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^tRTR after ($\overline{FL}$)/$\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume (useful only in SINGLE mode with no wraparound).

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. FLOW-THROUGH READs are initiated from the rising edge of $\overline{W}$ and access time is measured from the rising edge of $\overline{EF}$.



* FIRST DEVICE LOADED

Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the stand alone or groups of expanded-depth mode FIFOs. Expanded-width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1) when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9010s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}/(\overline{HF})$ and $\overline{FL}/(\overline{RT})$. Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered during a RESET cycle, by tying the $\overline{XO}/(\overline{HF})$ pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}/(\overline{RT})$ pin grounded. The remaining devices in the chain will have $\overline{FL}/(\overline{RT})$ tied HIGH. During RESET cycle, $\overline{XO}/(\overline{HF})$ of each device is held HIGH, disabling reads and writes to all FIFOs, except the first load device. When the last physical location of the first device is written, the $\overline{XO}/(\overline{HF})$ pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9010. The writes will continue to go to the second device until last location WRITE. Then it will "pass" the write pointer to the third device.

The full condition of the entire FIFO array is signaled by "OR-ing" all the $\overline{FF}$ pins. On the last physical READ of the first device, its $\overline{XO}/(\overline{HF})$ will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. An empty condition is signaled by OR-ing all of the $\overline{EF}$ pins. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{\text{RS}}$	$\overline{\text{RT}}$	$\overline{\text{XI}}$	**Read Pointer**	**Write Pointer**	$\overline{\text{EF}}$	$\overline{\text{FF}}$	$\overline{\text{HF}}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{\text{RS}}$	$\overline{\text{FL}}$	$\overline{\text{XI}}$	**Read Pointer**	**Write Pointer**	$\overline{\text{EF}}$	$\overline{\text{FF}}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{\text{XO}}$ of previous device.
$\overline{\text{RS}}$ = Reset Input, $\overline{\text{FL}}/\overline{\text{RT}}$/DIR= First Load/Retransmit, $\overline{\text{EF}}$ = Empty Flag Output, $\overline{\text{FF}}$ = Full Flag Output, $\overline{\text{XI}}$ = Expansion Input, $\overline{\text{HF}}$ = Half-Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -0.5V to +7.0V
Operating Temperature T_A (ambient) .... 0°C to 70°C
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R}$ ≤ V_{IL}; V_{CC} = MAX Outputs Open	I_{CC}	140	130	120	100	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R}$ ≥ V_{IH}; V_{CC} = MAX	I_{SB1}	15	15	15	15	mA	
	$\overline{W}$, $\overline{R}$ ≥ V_{CC} -0.2; V_{CC} = MAX V_{IL} ≤ V_{SS} +0.2 V_{IH} ≥ V_{CC} -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	8	pF	4
Output Capacitance		C_O	8	pF	4

Micron Technology, Inc., reserves the right to change products or specifications without notice.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Shift frequency	Fs		40		33.3		28.5		22.2	MHz	
Access time	^{t}A		15		20		25		35	ns	
READ cycle time	^{t}RC	25		30		35		45		ns	
READ recovery time	^{t}RR	10		10		10		10		ns	
READ pulse width	^{t}RPW	15		20		25		35		ns	6
READ LOW to Low-Z	^{t}RLZ	5		5		5		5		ns	
READ HIGH to High-Z	^{t}RHZ		15		15		18		20	ns	
Data hold from $\overline{\text{R}}$ HIGH	^{t}OH	5		5		5		5		ns	
WRITE cycle time	^{t}WC	25		30		35		45		ns	
WRITE pulse width	^{t}WPW	15		20		25		35		ns	6
WRITE recovery time	^{t}WR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^{t}WLZ	5		5		5		5		ns	5
Data setup time	^{t}DS	10		12		15		18		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
RESET cycle time	^{t}RSC	25		30		35		45		ns	
RESET pulse width	^{t}RSP	15		20		25		35		ns	6
RESET recovery time	^{t}RSR	10		10		10		10		ns	
READ HIGH to RESET HIGH	^{t}RRS	15		20		25		35		ns	
WRITE HIGH to RESET HIGH	^{t}WRS	15		20		25		35		ns	
RETRANSMIT cycle time	^{t}RTC	25		30		35		45		ns	
RETRANSMIT pulse width	^{t}RT	15		20		25		35		ns	
RETRANSMIT recovery time	^{t}RTR	10		10		10		12		ns	
RETRANSMIT setup time	^{t}RTS	15		20		25		35		ns	
RESET to $\overline{\text{AEF}}$, $\overline{\text{EF}}$ LOW	^{t}EFL		25		30		35		45	ns	
RESET to $\overline{\text{AFF}}$, $\overline{\text{HF}}$, $\overline{\text{FF}}$ HIGH	^{t}HFH, ^{t}FFH		25		30		35		45	ns	
READ LOW to $\overline{\text{EF}}$ LOW	^{t}REF		20		20		25		30	ns	
READ HIGH to $\overline{\text{FF}}$ HIGH	^{t}RFF		20		20		25		30	ns	
WRITE LOW to $\overline{\text{FF}}$ LOW	^{t}WFF		20		20		25		30	ns	
WRITE HIGH to $\overline{\text{EF}}$ HIGH	^{t}WEF		20		20		25		30	ns	
WRITE LOW to $\overline{\text{HF}}$ LOW	^{t}WHF		25		30		35		45	ns	
READ HIGH to $\overline{\text{HF}}$ HIGH	^{t}RHF		25		30		35		45	ns	
READ HIGH after $\overline{\text{EF}}$ HIGH	^{t}RPE	15		20		25		35		ns	5
WRITE HIGH width after $\overline{\text{FF}}$ HIGH	^{t}WPF	15		20		25		35		ns	5
READ/WRITE to $\overline{\text{XO}}$ LOW	^{t}XOL		20		20		25		35	ns	
READ/WRITE to $\overline{\text{XO}}$ HIGH	^{t}XOH		20		20		25		35	ns	
$\overline{\text{XI}}$ pulse width	^{t}XIP	15		20		25		35		ns	
$\overline{\text{XI}}$ setup time	^{t}XIS	10		12		15		15		ns	
$\overline{\text{XI}}$ recovery time	^{t}XIR	10		10		10		10		ns	

NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Flow-through mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

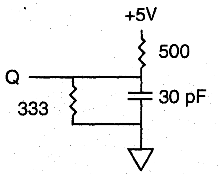
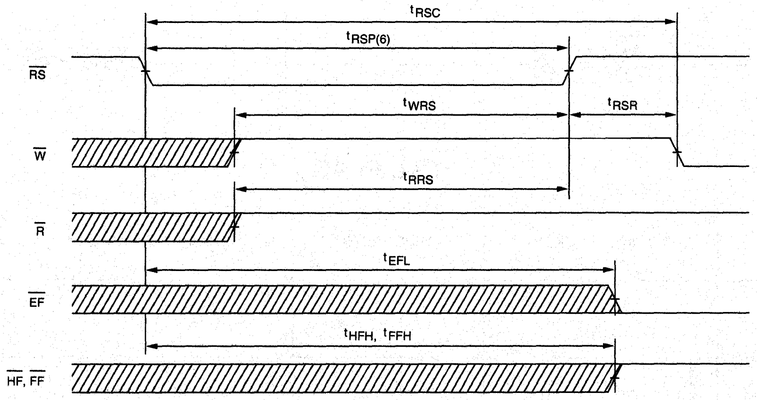
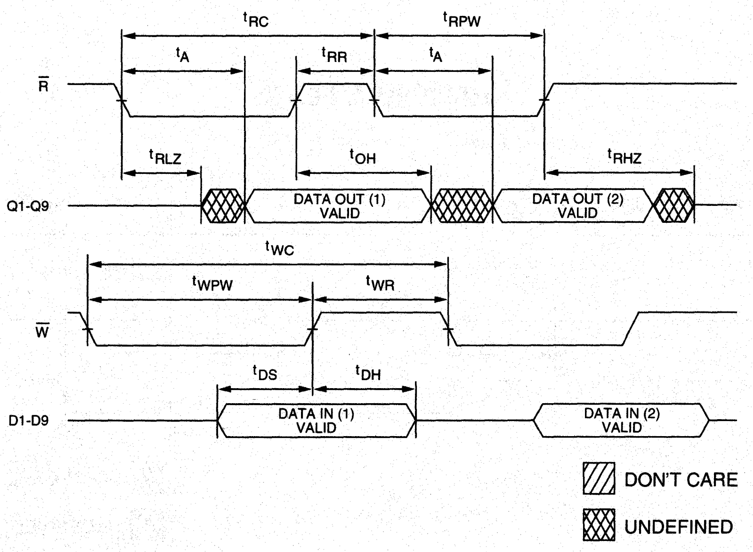


Fig. 2
OUTPUT LOAD EQUIVALENT

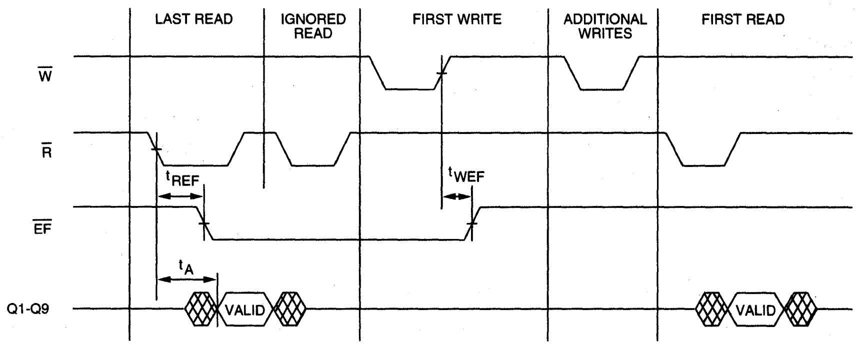
RESET



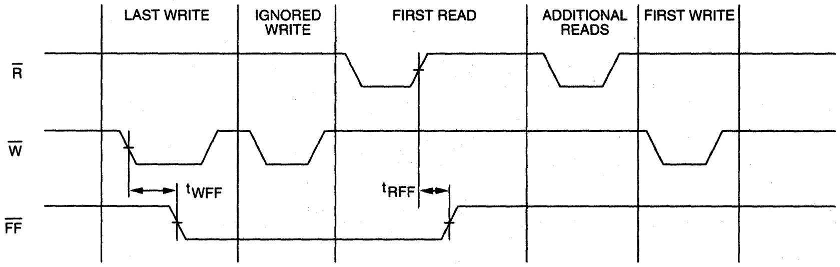
ASYNCHRONOUS READ AND WRITE



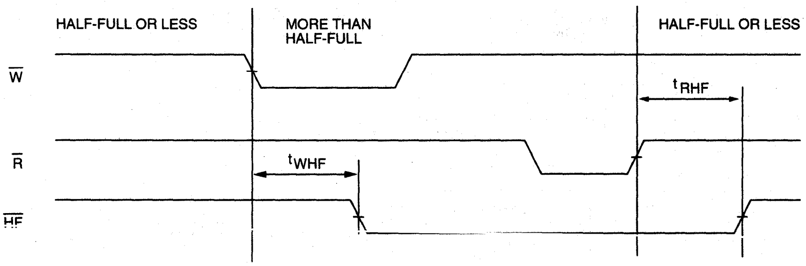
EMPTY FLAG



FULL FLAG



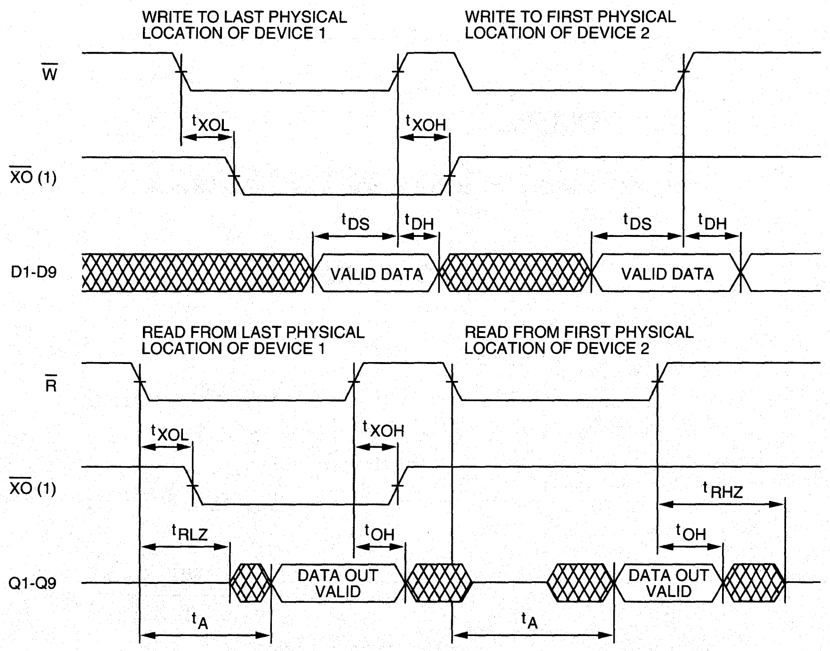
HALF-FULL FLAG



▨ DON'T CARE

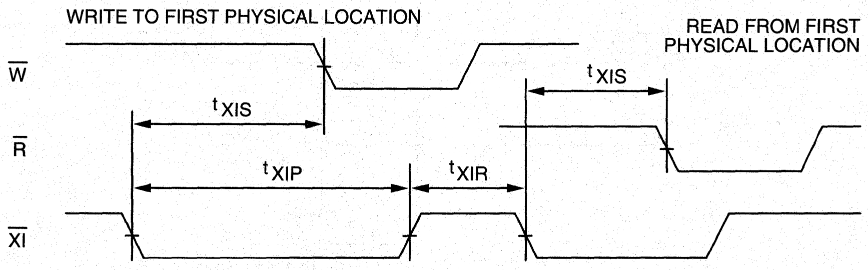
▩ UNDEFINED

EXPANSION MODE ($\overline{\text{XO}}$)



NOTE: $\overline{\text{XO}}$ of the Device 1 is connected to $\overline{\text{XI}}$ of Device 2.

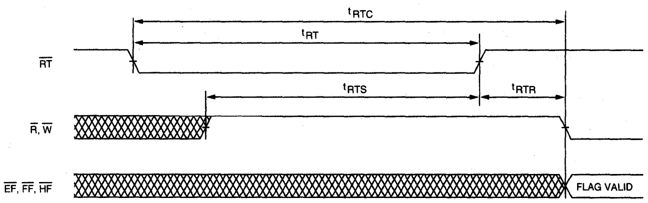
EXPANSION MODE ($\overline{\text{XI}}$)



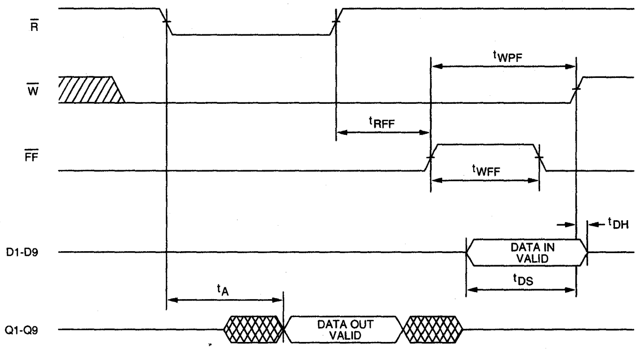
▨ DON'T CARE

▩ UNDEFINED

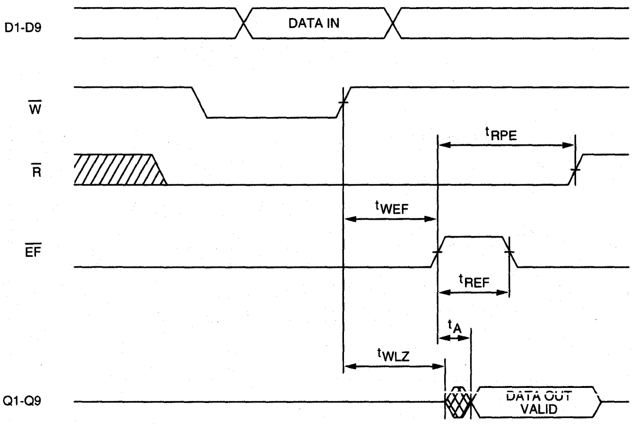
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



▨ DON'T CARE

▩ UNDEFINED

PRELIMINARY

MICRON TECHNOLOGY, INC.

MT52C9012

FIFO

1K x 9 FIFO

WITH PROGRAMMABLE FLAGS

FEATURES

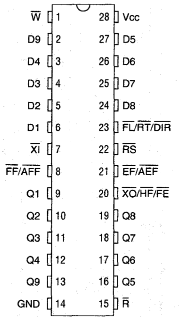
- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typical (standby); 350mW typical (active)
- TTL compatible inputs and outputs
- Asynchronous READ and WRITE
- Two fully configurable Almost-Full and Almost-Empty Flags
- Programmable Half-Full Flag or Full/Empty Flag option eliminates external counter requirement
- Register loading via the input or output pins
- Auto-retransmit capability in SINGLE DEVICE mode
- Fully expandable by width and depth
- Pin and function compatible with standard FIFOs

OPTIONS	MARKING
• Timing	
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
PLCC	EJ
Plastic SOJ	DJ

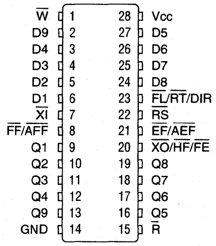
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***

PIN ASSIGNMENT (Top View)

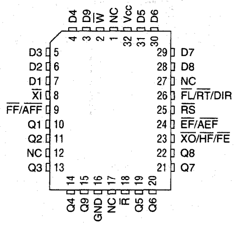
28-Pin DIP
(A-9, A-11)



28-Pin SOJ
(E-8)



32-Pin PLCC
(D-2)



GENERAL DESCRIPTION

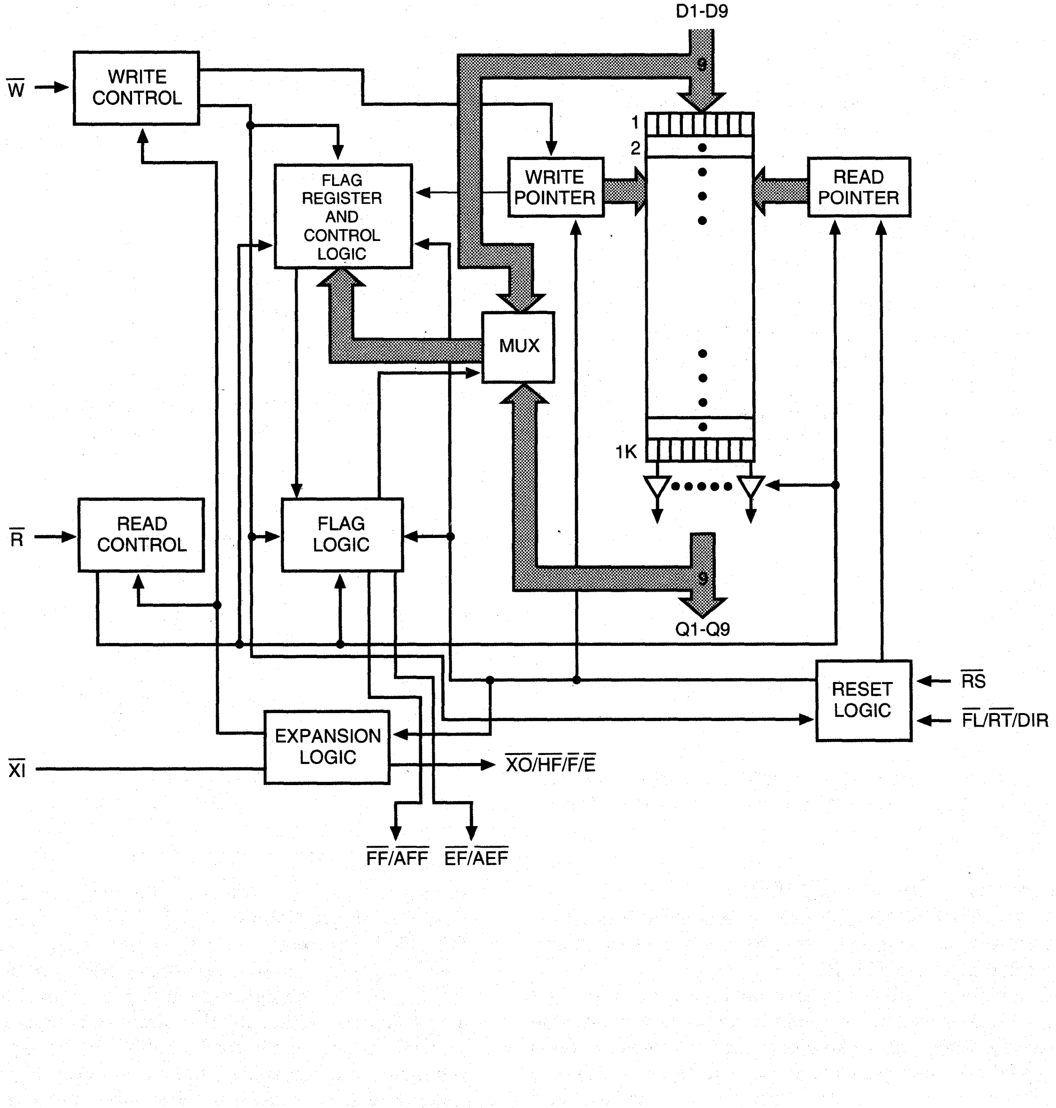
The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual-port, six-transistor memory cell with resistor loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates.

When not configured, the MT52C9012 defaults to a standard FIFO with empty ($\overline{EF}$), full ($\overline{FF}$) and half-full ($\overline{HF}$) flag pins. The MT52C9012 can be configured for programmable flags by loading the internal flag registers (as described under "Register Load Mode" on page 5-45). In CONFIGURED mode, up to three flags are provided. The first two are the almost-empty flag ($\overline{AEF}$) and the almost-full flag ($\overline{AFF}$) with independently programmable offsets. The third one is either an $\overline{HF}$ or a full and empty ($\overline{FE}$) flag, depending on the bit configuration of the registers. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the stand-alone mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. Also, the MT52C9012 is speed, function and pin compatible with higher and lower density FIFOs from Micron. This upward compatibility with 2K FIFOs provides a single-chip depth-expansion solution.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: This pin is used to reset the device and load internal flag registers. During device reset, all internal pointers and registers are cleared.
2	1	$\overline{W}$	Input	Write: A LOW on this pin loads data into the device. The internal write pointer is incremented after the rising edge of the write input.
18	15	$\overline{R}$	Input	Read: A LOW on this pin puts the oldest valid data byte in the memory array on the output bus. The internal read pointer is incremented at the rising edge of the read signal. Outputs are in High-Z when this pin is HIGH.
8	7	$\overline{XI}$	Input	Expansion-In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$) of the previous device in the daisy chain.
26	23	$\overline{FL/RT}$/DIR	Input	First Load/Retransmit/Direction: When in SINGLE DEVICE mode, this pin can be used to initiate a reread of the previously read data. When in REGISTER LOAD mode, the pin is used for register loading direction. When it is LOW, registers are loaded through the data output pins. When it is HIGH, registers are loaded through the data input pins. In DEPTH EXPANSION mode, this pin should be tied LOW if the device is the first one in the chain and tied HIGH if it is not the first one.
7, 6, 5, 4, 31, 30 29, 28, 3	6, 5, 4, 3, 27 26, 25, 24, 2	D1-D9	Input	Data Inputs: Data on these lines are stored in the memory array or flag registers during array WRITE or register programming, respectively.
24	21	$\overline{EF/AEF}$	Output	Empty Flag/Almost-Empty Flag: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is an Empty Flag output. When in CONFIGURED mode, it is an Almost-Empty Flag output. This pin is active LOW.
9	8	$\overline{FF/AFF}$	Output	Full Flag/Almost-Full Flags: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is a Full Flag output. When in CONFIGURED mode, it is an Almost-Full Flag output. This pin is active LOW.
23	20	$\overline{XO/HF/FE}$	Output	Expansion Out/Half-Full/Full/Empty: This pin's function is determined by its operation mode. When in SINGLE DEVICE mode, this pin is either HF Flag or a Full/Empty Flag, depending on the state of the most significant bit of Almost-Full Flag Register. The pin is an $\overline{XO}$ output when the part is in DEPTH EXPANSION mode. This pin defaults to $\overline{XO/HF}$ in NONCONFIGURED mode.
10, 11, 13, 14 19, 20, 21, 22,15	9, 10, 11, 12, 16 17, 18, 19, 13	Q1-Q9	I/O	Data Output: These pins may be used for data retrieval. The pins become inputs during register loading with DIR input HIGH. The outputs are disabled (High-Z) during device idle ($\overline{R}$ = HIGH).
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	GND	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9012 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For multiple-function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing half-full flags, the* $\overline{XO}/\overline{HF}/\overline{FE}$ *pin will be shown as* $(\overline{XO})/\overline{HF}/(\overline{FE})$.

RESET

After Vcc is stable, Reset ($\overline{\text{RS}}$) must be taken LOW with both $\overline{\text{R}}$ and $\overline{\text{W}}$ HIGH to initialize the read and write pointers and flags. This also clears all internal registers. During the reset pulse, the state of the $\overline{\text{XI}}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{\text{XI}}$ is tied LOW. If $\overline{\text{XI}}$ is connected to $\overline{\text{XO}}/(\overline{\text{HF}})$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{\text{W}}$) pin is taken LOW and if the FIFO is not full. The WRITE cycle is initiated by the falling edge of $\overline{\text{W}}$. Data on the D1-D9 pins are latched on the rising edge. If the location to be written is the last empty location in the FIFO, $\overline{\text{FF}}$ will be asserted (LOW) after the falling edge of $\overline{\text{W}}$. While $\overline{\text{FF}}$ is asserted, all writes are inhibited and previously stored data are unaffected. The first WRITE to an empty FIFO will cause $\overline{\text{EF}}$ to go HIGH after the rising edge of $\overline{\text{W}}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{\text{XO}}/(\overline{\text{HF}})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{\text{R}}$) pin is taken LOW and FIFO is not empty ($\overline{\text{EF}}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^{t}RLZ after the falling edge of $\overline{\text{R}}$. Valid data will appear ^{t}A after the falling edge of $\overline{\text{R}}$. After the last available data word is read, $\overline{\text{EF}}$ will go LOW upon the falling edge of $\overline{\text{R}}$. While $\overline{\text{EF}}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is full and a READ is initiated, the $\overline{\text{FF}}$ will go HIGH after the rising edge of $\overline{\text{R}}$. When operating in the expanded mode, the last location read from a FIFO will cause $\overline{\text{XO}}/(\overline{\text{HF}})$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9012 allows the receiving device to request that data just read from the FIFO be repeated, when less than 1024 writes have been performed between resets. When the $(\overline{\text{FL}})/\overline{\text{RT}}/$(DIR) pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may start reading the data from the beginning of the FIFO ^{t}RTR after $(\overline{\text{FL}})/\overline{\text{RT}}/$(DIR) is taken HIGH. Some or all flags may be affected depending on the location of the read and write pointers before and after the retransmit.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{\text{W}}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{\text{R}}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{\text{R}}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{\text{W}}$, and access time is measured from the rising edge of the empty flag.

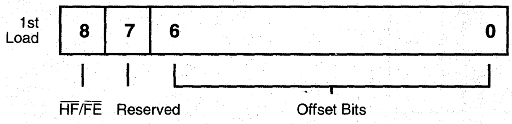
REGISTER LOAD MODE

This mode of operation is used to reset the device and program the internal flag registers. This yields an almost full and an almost-empty flag (DIP package pins 8 and 21 respectively) and a half-full or $\overline{F}/\overline{E}$ flag (DIP package pin 20).

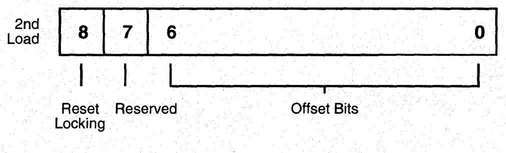
Two 9-bit internal registers have been provided for flag configuration. One is the almost-full flag register (AFFR) and the other is the almost-empty flag register (AEFR). Bit configurations of the two registers are shown below.

REGISTER SET FOR MT52C9012

Almost Full Flag Register (AFFR)



Almost Empty Flag Register (AEFR)



Note that bits 0-6 are used for offset setting. The offset value ranges from 1 to 127 words. Each offset value corresponds to a 2-byte increment. This provides a maximum offset of 254 bytes.

Bits 6 and 7 are reserved for future offset expansion. Bit 8 of the AFFR is used for configuration of $\overline{HF}/\overline{FE}$ pin. When this bit is set LOW, the HF/$\overline{FE}$ pin is configured as an $\overline{HF}$ flag output. When it is set HIGH, the HF/$\overline{FE}$ is configured as an $\overline{F}/\overline{E}$ flag output.

Bit 8 of the AEFR is used for reset locking. When this bit is set LOW, subsequent device RESET or REGISTER LOADING cycles reset the device. When the bit is programmed HIGH, subsequent RESET cycles are ignored. In this mode, the flag registers can be reconfigured without device reset. The part can be reset by cycling power to the device or by writing zero (0) into bit 8 of the AEFR register followed by a DEVICE RESET or REGISTER LOAD.

Flag registers are loaded by bringing $\overline{RS}$ LOW followed by the $\overline{R}$ input. The $\overline{R}$ pin should be brought LOW ^tRS after the $\overline{RS}$ becomes LOW. The registers may be loaded via the input pins or the output pins depending on the status of the DIR control input. Data is latched into the registers at the rising edge of the $\overline{W}$ control pin. The first WRITE loads the AFFR while the second WRITE loads the AEFR. This loading order is fixed.

BIDIRECTIONAL MODE

Applications requiring data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by using two MT52C9012s. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both depth expansion and width expansion may be used in this mode.

FLAG TIMING

A total of three flag outputs are provided in either CONFIGURED or NONCONFIGURED mode. In the NONCONFIGURED mode, the three flags are $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$. The $\overline{HF}$ flag goes active when more than half the FIFO is full. The flag goes inactive when the FIFO is half full or less.

The full and empty flags are asserted when the last byte is written to or read out of the FIFO, respectively. They are deasserted when the first byte is loaded into an empty FIFO or read out of a full FIFO, respectively. All three flag outputs are active LOW.

When the device is programmed, the $\overline{AFF}$ and $\overline{AEF}$ go active after a READ/WRITE cycle initiation of the location corresponding to the programmed offset value. For example, if the AEFR is programmed with a 10-byte offset (loading a Hex value of 05), the $\overline{AEF}$ flag goes active while reading the 10th location before the FIFO is empty. The flag goes inactive when there are 10 or more bytes left in the FIFO. The assertion timing and deassertion timing of the $\overline{AFF}$ are the same.

The third flag in the PROGRAM mode is either $\overline{HF}$ or $\overline{F}/\overline{E}$ flag depending on the state of the highest bit of the AFFR. If the device is programmed for $\overline{HF}$ flag, it functions like the $\overline{HF}$ flag in NONPROGRAMMED mode. If the device is configured for $\overline{F}/\overline{E}$ flag, the pin will be active (LOW) when the FIFO is either empty or full. The condition of the FIFO is determined by the state of $\overline{F}/\overline{E}$ together with states of $\overline{AFF}$ and $\overline{AEF}$ (example: if $\overline{F}/\overline{E}$ is LOW and $\overline{AFF}$ is LOW but $\overline{AEF}$ is HIGH, the FIFO is full).

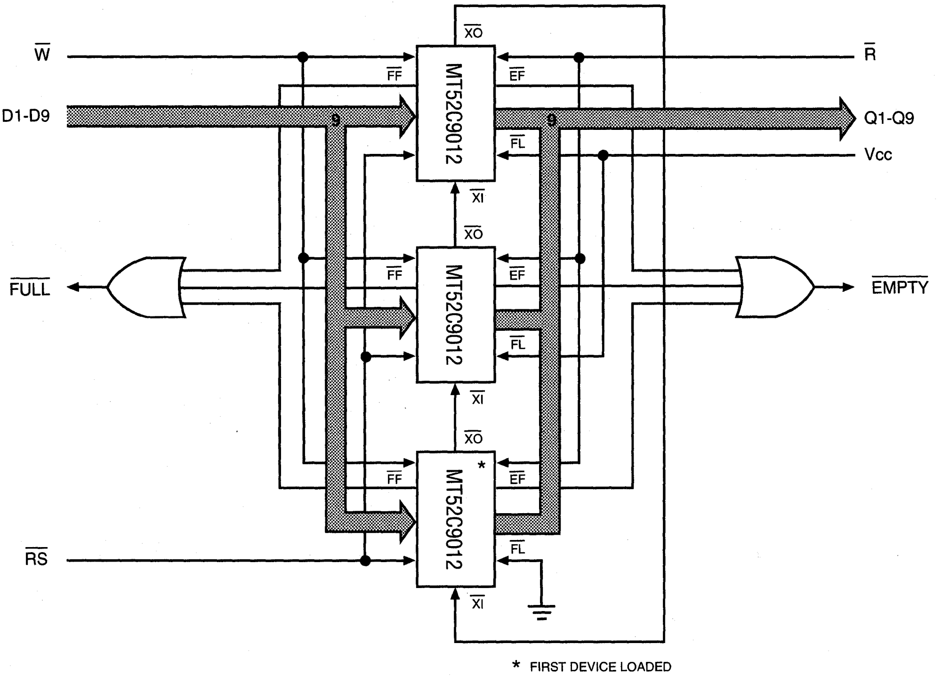


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9012s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) and $\overline{FL}$/($\overline{RT}$/DIR). Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered by tying the $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$/($\overline{RT}$/DIR) pin grounded. The remaining devices in the chain will have $\overline{FL}$/($\overline{RT}$/DIR) tied HIGH. Upon a reset, reads and writes to all FIFOs are disabled, except the first load device. When the last physical location of the first device is written, the $\overline{XO}$/($\overline{HF}$) pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9012. The writes will continue to go to the second device until last location write. Then it will "pass" the write pointer to the third device. The full condition of the entire FIFO array is signaled when all the $\overline{FF}$/($\overline{AFF}$) pins are LOW.

On the last physical READ of the first device, its $\overline{XO}$ ($\overline{HF}$) will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. On the last READ, an empty condition is signaled by all of the $\overline{EF}$ pins being LOW. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

MODE	**INPUTS**			**INTERNAL STATUS**		**OUTPUTS**		
	$\overline{\text{RS}}$	**$\overline{\text{RT}}$**	**$\overline{\text{XI}}$**	**Read Pointer**	**Write Pointer**	**$\overline{\text{EF}}$**	**$\overline{\text{FF}}$**	**$\overline{\text{HF}}$**
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

MODE	**INPUTS**			**INTERNAL STATUS**		**OUTPUTS**	
	$\overline{\text{RS}}$	**$\overline{\text{FL}}$**	**$\overline{\text{XI}}$**	**Read Pointer**	**Write Pointer**	**$\overline{\text{EF}}$**	**$\overline{\text{FF}}$**
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{\text{XO}}$ of previous device.
$\overline{\text{RS}}$ = Reset Input, $\overline{\text{FL}}/\overline{\text{RT}}$/DIR = First Load/Retransmit, $\overline{\text{EF}}$ = Empty Flag Output, $\overline{\text{FF}}$ = Full Flag Output, $\overline{\text{XI}}$ = Expansion Input, $\overline{\text{HF}}$ = Half-Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -0.5V to +7.0V
Operating Temperature T_A (ambient) .... 0°C to 70°C
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}, \overline{R} \le V_{IL}$; Vcc = MAX f = MAX = 1/ ${}^tRC$ Outputs Open	I_{CC}	140	130	120	100	mA	3
Power Supply Current: Standby	$\overline{W}, \overline{R} \ge V_{IH}$; Vcc = MAX f = MAX = 1/ ${}^tRC$	I_{SB1}	15	15	15	15	mA	
	$\overline{W}, \overline{R} \ge V_{CC}$ -0.2; Vcc = MAX $V_{IL} \le V_{SS}$ +0.2 $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

(V_{IN} = 0V; V_{OUT} = 0V)

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	C_I	8	pF	4
Output Capacitance		C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured and nonconfigured modes) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Shift frequency	^{t}RF		40		33.3		28.5		22.2	MHz	
READ cycle time	^{t}RC	25		30		35		45		ns	
Access time	^{t}A		15		20		25		35	ns	6
READ recovery time	^{t}RR	10		10		10		10		ns	
READ pulse width	^{t}RPW	15		20		25		35		ns	
READ LOW to Low-Z	^{t}RLZ	5		5		5		5		ns	7
READ HIGH to High-Z	^{t}RHZ		15		15		18		20	ns	7
Data HOLD from $\overline{R}$ HIGH	^{t}OH	5		5		5		5		ns	
WRITE Cycle											
WRITE cycle time	^{t}WC	25		30		35		45		ns	
WRITE pulse width	^{t}WPW	15		20		25		35		ns	6
WRITE recovery time	^{t}WR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^{t}WLZ	5		5		5		5		ns	5, 7
Data setup time	^{t}DS	10		12		15		18		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
RETRANSMIT Cycle											
RESTRANSMIT cycle time	^{t}RTC	25		30		35		45		ns	
RESTRANSMIT pulse width	^{t}RT	15		20		25		35		ns	
RESTRANSMIT recovery time	^{t}RTR	10		10		10		12		ns	
RESTRANSMIT setup time	^{t}RTS	15		20		25		35		ns	
RESET Cycle											
RESET cycle time (no register programming)	^{t}RSC	25		30		35		45		ns	
RESET pulse width	^{t}RSP	15		20		25		35		ns	6
RESET recovery time	^{t}RSR	10		10		10		10		ns	
$\overline{RS}$ LOW to $\overline{R}$ LOW	^{t}RS	15		20		25		35		ns	
RESET and register programming cycle time	^{t}RSPC	85		100		115		145		ns	
$\overline{R}$ LOW to DIR valid (register load cycle)	^{t}RDV	5		5		5		5		ns	
$\overline{R}$ LOW to register load	^{t}RW	10		10		10		10		ns	
$\overline{W}$ HIGH to $\overline{RS}$ LOW	^{t}WRS	0		0		0		0		ns	
$\overline{R}$ HIGH to $\overline{RS}$ LOW	^{t}RRS	0		0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured mode only) (T_A = 0°C to 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Mode Timing											
R/W to XO LOW	^{t}XOL		20		20		25		35	ns	
R/W to XO HIGH	^{t}XOH		20		20		25		35	ns	
XI pulse width	^{t}XIP	15		20		25		35		ns	
XI setup time to R/W	^{t}XIS	10		12		15		15		ns	
XI recovery time	^{t}XIR	10		10		10		10		ns	
Flags Timing											
W HIGH to Flags Valid	^{t}WFV		15		15		15		15	ns	
RS to AEF, EF LOW	^{t}EFL		25		30		35		45	ns	
R LOW to EF LOW	^{t}REF		20		20		25		30	ns	
W HIGH to EF HIGH	^{t}WEF		20		20		25		30	ns	
R HIGH after EF HIGH	^{t}RPE	15		20		25		35		ns	5
RS to AFF, HF, FF HIGH	^{t}HFH, ^{t}FFH		25		30		35		45	ns	
R HIGH to FF HIGH	^{t}RFF		15		20		25		30	ns	
W LOW to FF LOW	^{t}WFF		20		20		25		30	ns	
W HIGH after FF HIGH	^{t}WPF	15		20		25		35		ns	5
W LOW to HF LOW	^{t}WHF		25		30		35		45	ns	
R HIGH to HF HIGH	^{t}RHF		25		30		35		45	ns	
R HIGH to AFF HIGH	^{t}RAFF		25		30		35		45	ns	
W LOW to AFF LOW	^{t}WAFF		25		30		35		45	ns	
R LOW to AEF LOW	^{t}RAEF		25		30		35		45	ns	
W HIGH to AEF HIGH	^{t}WAEF		25		30		35		45	ns	

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

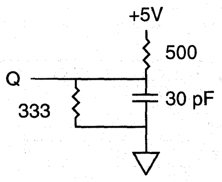
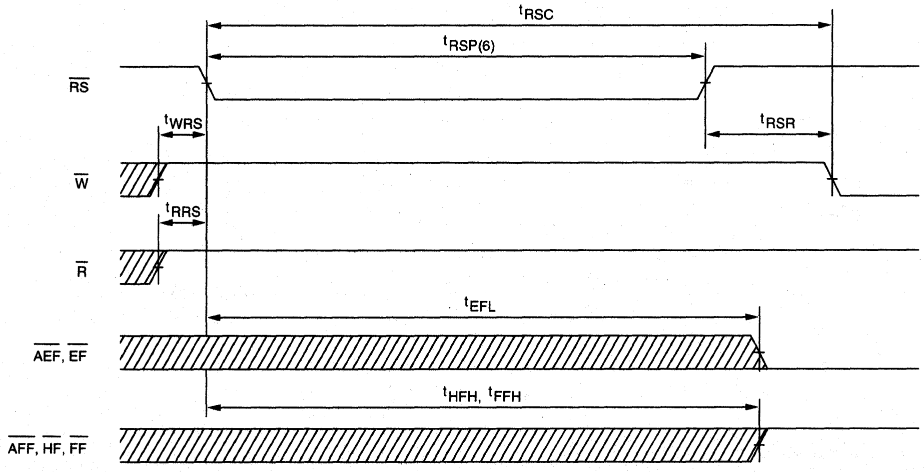


Figure 2
OUTPUT LOAD EQUIVALENT

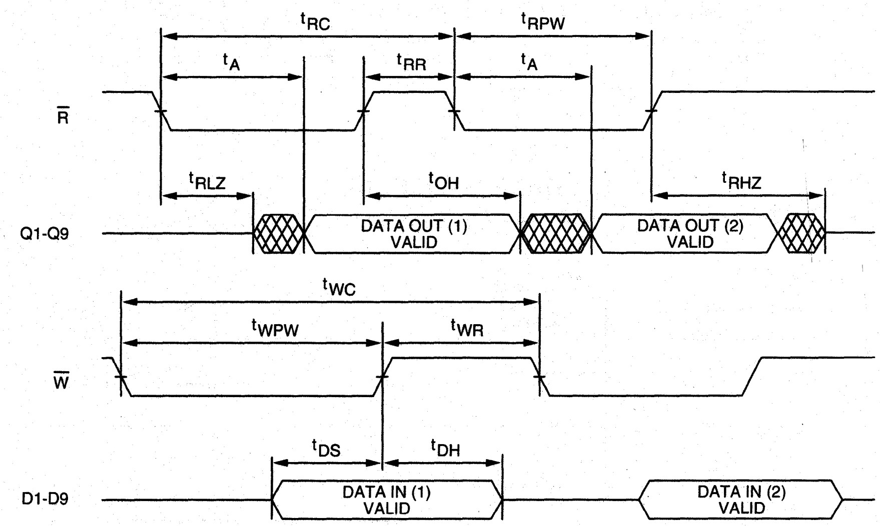
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.
7. Values guaranteed by design, not currently tested.
8. R and DIR signals must go inactive (HIGH) coincident with RS going inactive (HIGH).
9. DIR must become valid before W goes active (LOW).

RESET
(WITH NO REGISTER PROGRAMMING)



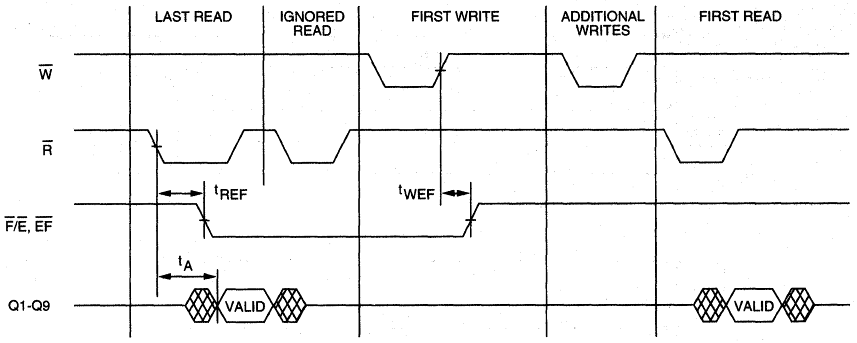
ASYNCHRONOUS READ AND WRITE



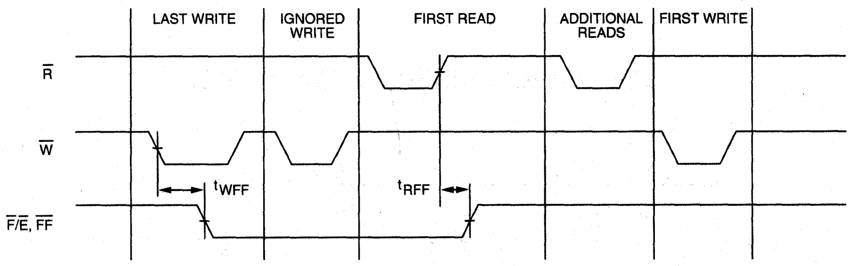
▨ DON'T CARE

▦ UNDEFINED

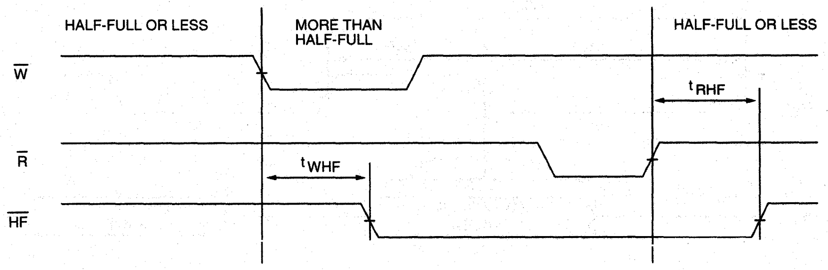
EMPTY FLAG



FULL FLAG



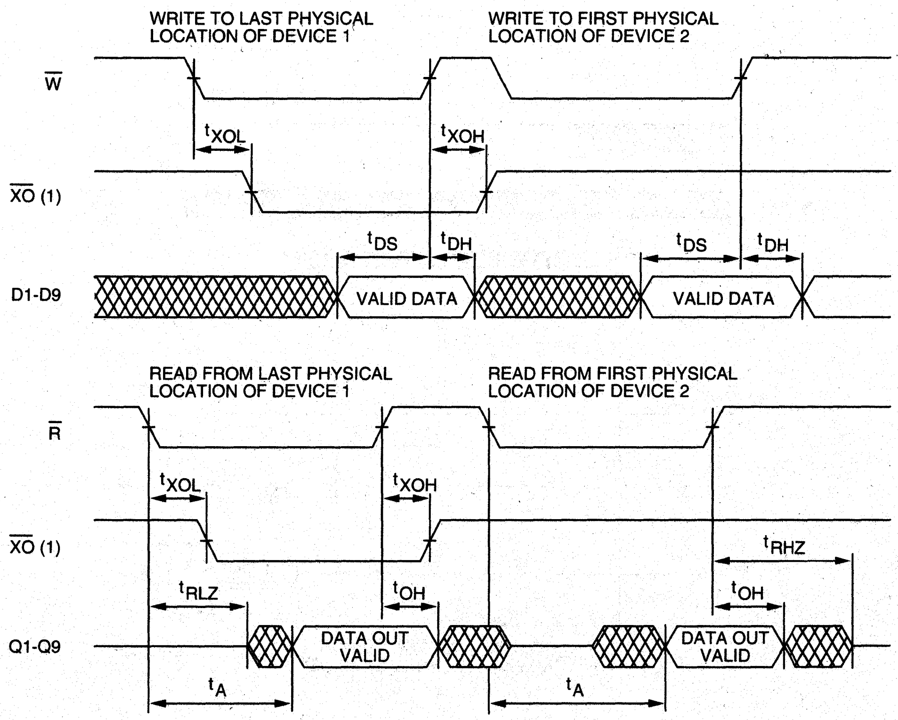
HALF-FULL FLAG
(FOR CONFIGURED AND NONCONFIGURED MODES)



▨ DON'T CARE

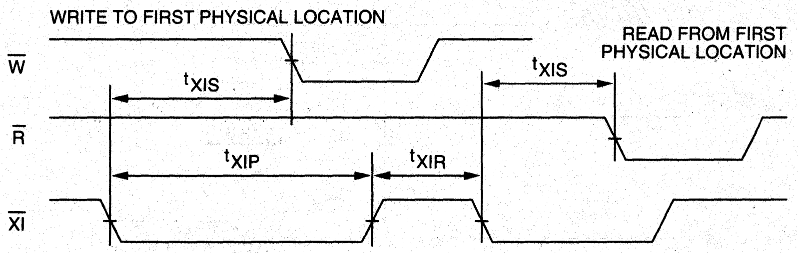
▩ UNDEFINED

EXPANSION MODE ($\overline{XO}$)



NOTE: 1. $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

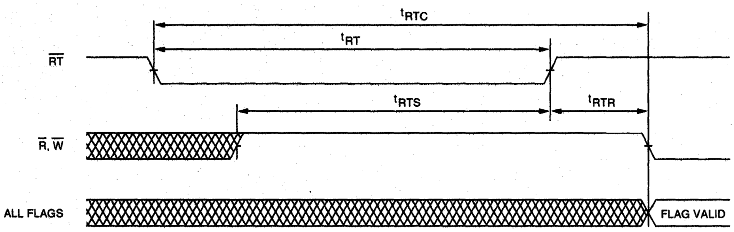
EXPANSION MODE ($\overline{XI}$)



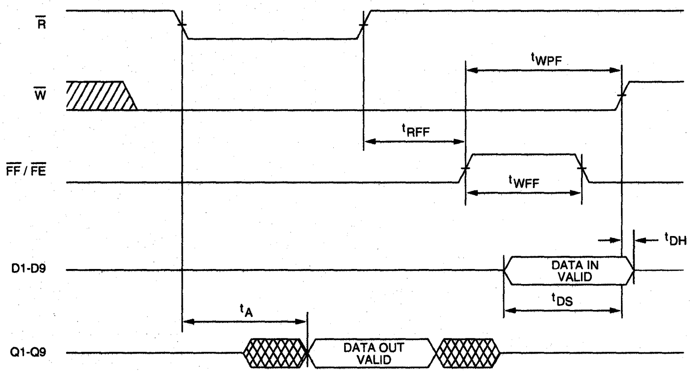
▨ DON'T CARE

▩ UNDEFINED

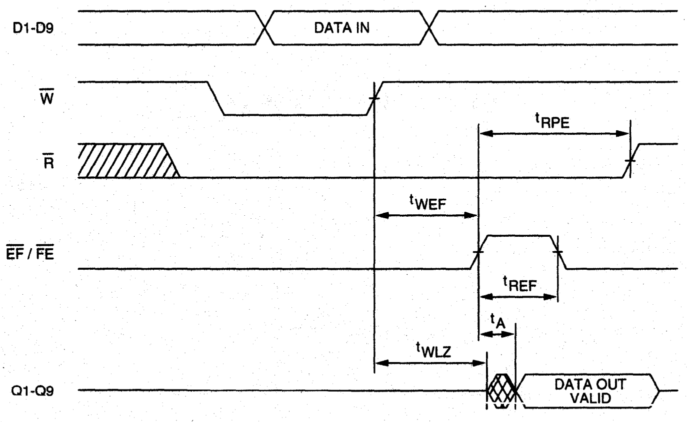
RETRANSMIT



WRITE FLOW-THROUGH



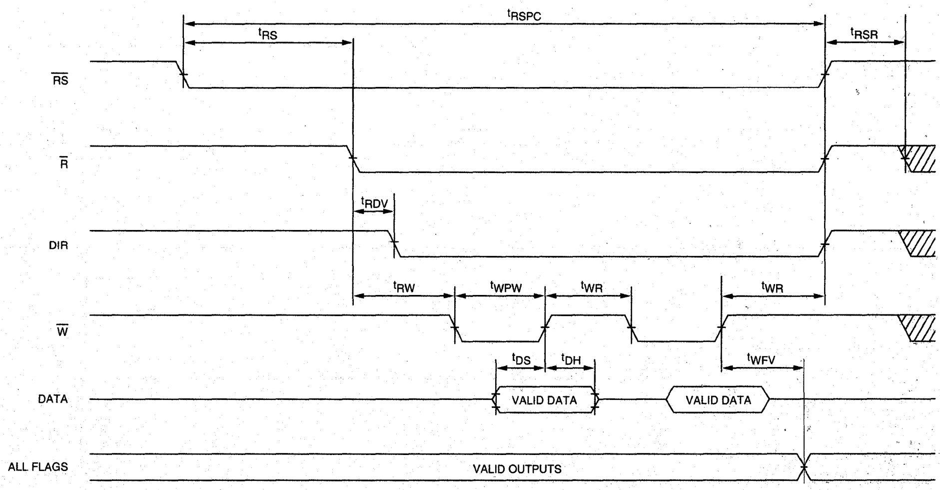
READ FLOW-THROUGH



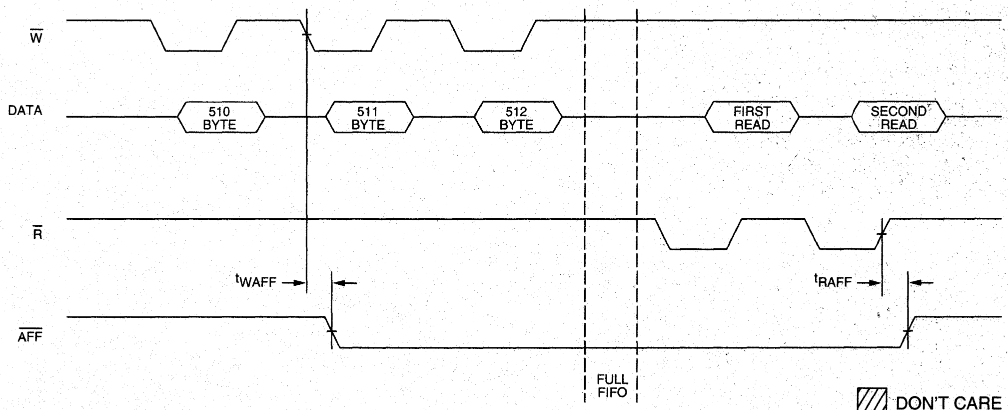
▨ DON'T CARE

▩ UNDEFINED

RESET/REGISTER PROGRAMMING CYCLE TIME[8, 9]



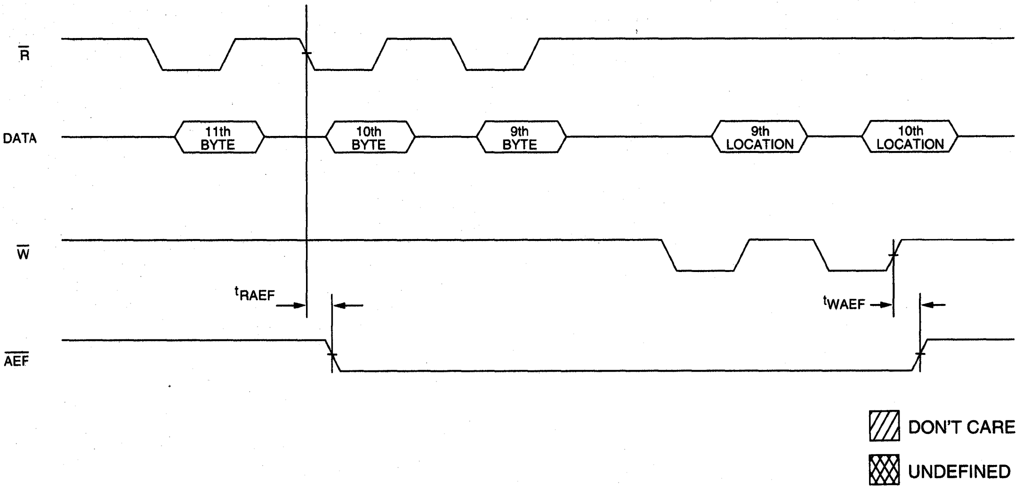
ALMOST-FULL FLAG (2-BYTE OFFSET)



▨ DON'T CARE

▩ UNDEFINED

ALMOST-EMPTY FLAG (10-BYTE OFFSET)



FIFO

2K x 9 FIFO

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (active)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Half-Full Flag in STAND ALONE mode
- Auto-retransmit capability
- Fully expandable by width and depth
- Pin and function compatible with other standard FIFOs

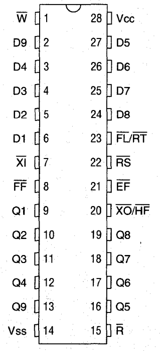
OPTIONS

OPTIONS	MARKING
• Timing	
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
PLCC	EJ
SOJ (300 mil)	DJ

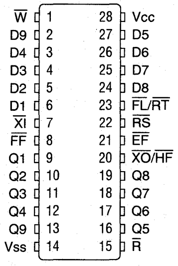
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***

PIN ASSIGNMENT (Top View)

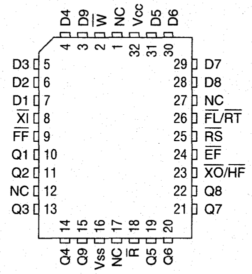
28-Pin DIP
(A-9, A-11)



28-Pin SOJ
(E-8)



32-Pin PLCC
(D-2)



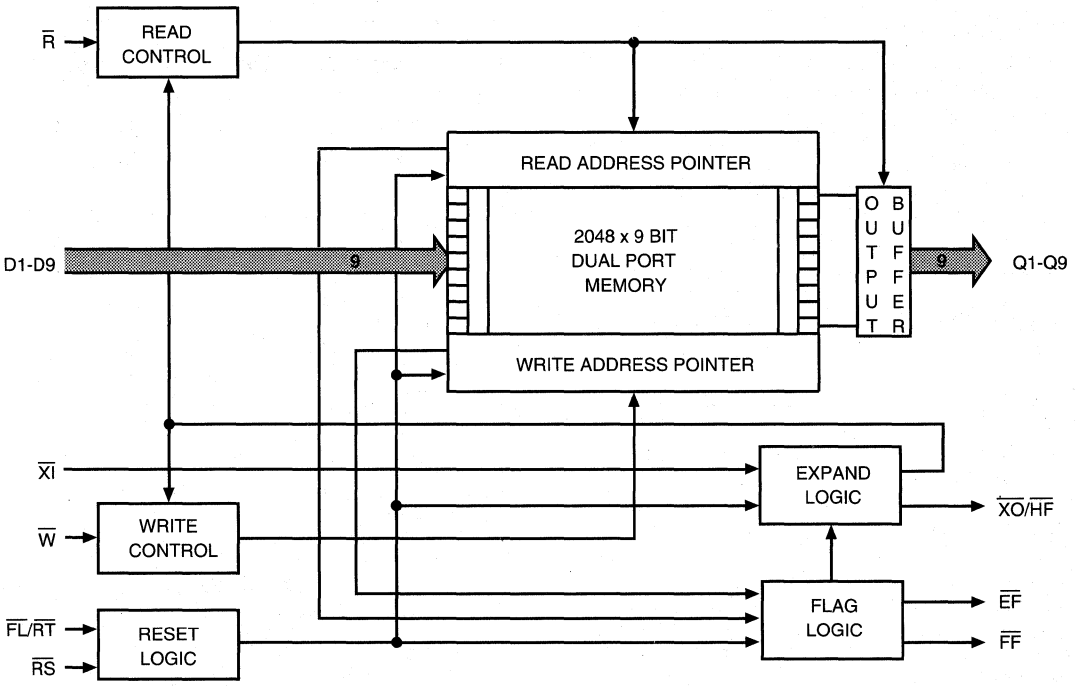
GENERAL DESCRIPTION

The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual port, six-transistor memory cell with resistor loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information can be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain in High-Z. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{\text{RS}}$	Input	Reset: Taking $\overline{\text{RS}}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place.
2	1	$\overline{\text{W}}$	Input	Write Strobe: $\overline{\text{W}}$ is taken LOW to write data from the input port (D1-D9) into the FIFO memory array.
18	15	$\overline{\text{R}}$	Input	Read Strobe: $\overline{\text{R}}$ is taken LOW to read data from the FIFO memory array to the output port (Q1-Q9).
8	7	$\overline{\text{XI}}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{\text{XO}}$)of the previous device in the daisy chain.
26	23	$\overline{\text{FL}}/\overline{\text{RT}}$	Input	First Load: Acts as first load signal in DEPTH EXPANSION mode. $\overline{\text{FL}}$ if low, will enable the device as the first to be loaded (enables read and write pointers). $\overline{\text{FL}}$ should be tied low for the first FIFO in the chain, and tied HIGH for all other FIFOs in the chain. Retransmit: Acts as retransmit signal in STAND ALONE mode. $\overline{\text{RT}}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{\text{RT}}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27 26, 25, 24, 2	D1-D9	Input	Data Inputs
24	21	$\overline{\text{EF}}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{\text{FF}}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{\text{XO}}/\overline{\text{HF}}$	Output	Expansion Out: Acts as expansion out pin in DEPTH EXPANSION mode. $\overline{\text{XO}}$ will pulse LOW on the last physical WRITE or the last physical read. $\overline{\text{XO}}$ should be connected to $\overline{\text{XI}}$ of the next FIFO in the daisy chain. Half-Full Flag: Acts as Half-Full Flag in STAND ALONE mode. $\overline{\text{HF}}$ goes LOW when the FIFO becomes more than Half-Full; will stay LOW until the FIFO becomes Half-Full or less.
10, 11, 13, 14, 19, 20, 21, 22, 15	9, 10, 11, 12, 16 17, 18, 19, 13	Q1-Q9	Output	Data Output: Output or High-Z.
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9020 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing the half-full flags, the* $\overline{XO}/\overline{HF}$ *pin will be shown as* $(\overline{XO})/\overline{HF}$.

RESET

After Vcc is stable, RESET ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is LOW. If $\overline{XI}$ is tied to $\overline{XO}$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins are latched on the rising edge. If the location to be written is the last empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the STAND ALONE mode, $(\overline{XO})/\overline{HF}$ is asserted when the half-full-plus-one location (2048/2 + 1) is written. It will stay asserted until the FIFO becomes half-full or less. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/\overline{HF}$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

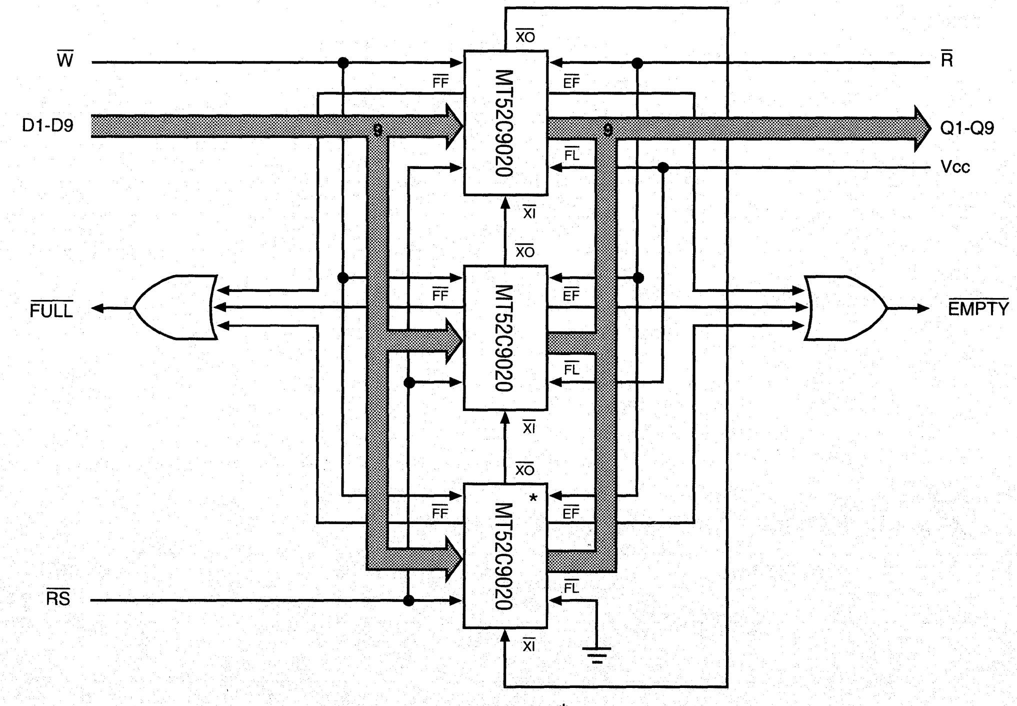
Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and the FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^{t}RLZ after the falling edge of $\overline{R}$ and valid data will appear ^{t}A after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is being used in the SINGLE DEVICE mode and the half-full-plus-one location is read, $(\overline{XO})/\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ LOW) and a READ is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read to a FIFO will cause $\overline{XO}/\overline{HF}$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9020 allows the receiving device to request that the data read earlier from the FIFO to be repeated, when less than 2047 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^{t}RTR after $(\overline{FL})/\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. FLOW-THROUGH READs are initiated from the rising edge of $\overline{W}$ and access time is measured from the rising edge of $\overline{EF}$.



* FIRST DEVICE LOADED

Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the stand alone or groups of expanded-depth mode FIFOs. Expanded-width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1) when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9020s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}$/($\overline{HF}$) and $\overline{FL}$/($\overline{RT}$). Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered during a RESET cycle, by tying the $\overline{XO}$/($\overline{HF}$) pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$/($\overline{RT}$) pin grounded. The remaining devices in the chain will have $\overline{FL}$/($\overline{RT}$) tied HIGH. During RESET cycle, $\overline{XO}$/($\overline{HF}$) of each device is held HIGH, disabling reads and writes to all FIFOs, except the first load device. When the last physical location of the first device is written, the $\overline{XO}$/($\overline{HF}$) pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9020. The writes will continue to go to the second device until last location WRITE. Then it will "pass" the write pointer to the third device.

The full condition of the entire FIFO array is signaled by "OR-ing" all the $\overline{FF}$ pins. On the last physical READ of the first device, its $\overline{XO}$/($\overline{HF}$) will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. An empty condition is signaled by OR-ing all of the $\overline{EF}$ pins. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{\text{RS}}$	$\overline{\text{RT}}$	$\overline{\text{XI}}$	**Read Pointer**	**Write Pointer**	$\overline{\text{EF}}$	$\overline{\text{FF}}$	$\overline{\text{HF}}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{\text{RS}}$	$\overline{\text{FL}}$	$\overline{\text{XI}}$	**Read Pointer**	**Write Pointer**	$\overline{\text{EF}}$	$\overline{\text{FF}}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{\text{XO}}$ of previous device.
$\overline{\text{RS}}$ = Reset Input, $\overline{\text{FL}}$/$\overline{\text{RT}}$/DIR= First Load/Retransmit, $\overline{\text{EF}}$ = Empty Flag Output, $\overline{\text{FF}}$ = Full Flag Output, $\overline{\text{XI}}$ = Expansion Input, $\overline{\text{HF}}$ = Half-Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -0.5V to +7.0V
Operating Temperature T_A (ambient) .... 0°C to 70°C
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

			MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{W}$, $\overline{R} \le V_{IL}$; V_{CC} = MAX Outputs Open	I_{CC}	140	130	120	100	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R} \ge V_{IH}$; V_{CC} = MAX	I_{SB1}	15	15	15	15	mA	
	$\overline{W}$, $\overline{R} \ge V_{CC}$ -0.2; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2 $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	8	pF	4
Output Capacitance		C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Shift frequency	Fs		40		33.3		28.5		22.2	MHz	
Access time	^{t}A		15		20		25		35	ns	
READ cycle time	^{t}RC	25		30		35		45		ns	
READ recovery time	^{t}RR	10		10		10		10		ns	
READ pulse width	^{t}RPW	15		20		25		35		ns	6
READ LOW to Low-Z	^{t}RLZ	5		5		5		5		ns	
READ HIGH to High-Z	^{t}RHZ		15		15		18		20	ns	
Data hold from $\overline{\text{R}}$ HIGH	^{t}OH	5		5		5		5		ns	
WRITE cycle time	^{t}WC	25		30		35		45		ns	
WRITE pulse width	^{t}WPW	15		20		25		35		ns	6
WRITE recovery time	^{t}WR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^{t}WLZ	5		5		5		5		ns	5
Data setup time	^{t}DS	10		12		15		18		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
RESET cycle time	^{t}RSC	25		30		35		45		ns	
RESET pulse width	^{t}RSP	15		20		25		35		ns	6
RESET recovery time	^{t}RSR	10		10		10		10		ns	
READ HIGH to Reset HIGH	^{t}RRS	15		20		25		35		ns	
WRITE HIGH to Reset HIGH	^{t}WRS	15		20		25		35		ns	
RETRANSMIT cycle time	^{t}RTC	25		30		35		45		ns	
RETRANSMIT pulse width	^{t}RT	15		20		25		35		ns	
RETRANSMIT recovery time	^{t}RTR	10		10		10		12		ns	
RETRANSMIT setup time	^{t}RTS	15		20		25		35		ns	
RESET to $\overline{\text{AEF}}$, $\overline{\text{EF}}$ LOW	^{t}EFL		25		30		35		45	ns	
RESET to $\overline{\text{AFF}}$, $\overline{\text{HF}}$, $\overline{\text{FF}}$ HIGH	^{t}HFH, ^{t}FFH		25		30		35		45	ns	
READ LOW to $\overline{\text{EF}}$ LOW	^{t}REF		20		20		25		30	ns	
READ HIGH to $\overline{\text{FF}}$ HIGH	^{t}RFF		20		20		25		30	ns	
WRITE LOW to $\overline{\text{FF}}$ LOW	^{t}WFF		20		20		25		30	ns	
WRITE HIGH to $\overline{\text{EF}}$ HIGH	^{t}WEF		20		20		25		30	ns	
WRITE LOW to $\overline{\text{HF}}$ LOW	^{t}WHF		25		30		35		45	ns	
READ HIGH to $\overline{\text{HF}}$ HIGH	^{t}RHF		25		30		35		45	ns	
READ HIGH after $\overline{\text{EF}}$ HIGH	^{t}RPE	15		20		25		35		ns	5
WRITE HIGH after $\overline{\text{FF}}$ HIGH	^{t}WPF	15		20		25		35		ns	5
READ/WRITE to $\overline{\text{XO}}$ LOW	^{t}XOL		20		20		25		35	ns	
READ/WRITE to $\overline{\text{XO}}$ HIGH	^{t}XOH		20		20		25		35	ns	
$\overline{\text{XI}}$ pulse width	^{t}XIP	15		20		25		35		ns	
$\overline{\text{XI}}$ setup time	^{t}XIS	10		12		15		15		ns	
$\overline{\text{XI}}$ recovery time	^{t}XIR	10		10		10		10		ns	

NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Flow-through mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

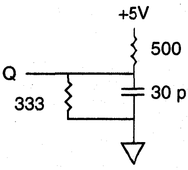
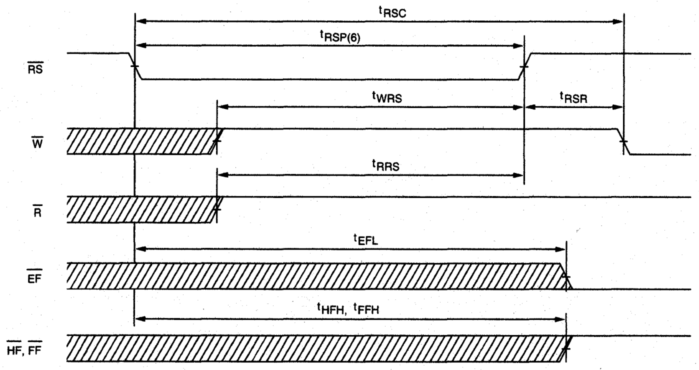
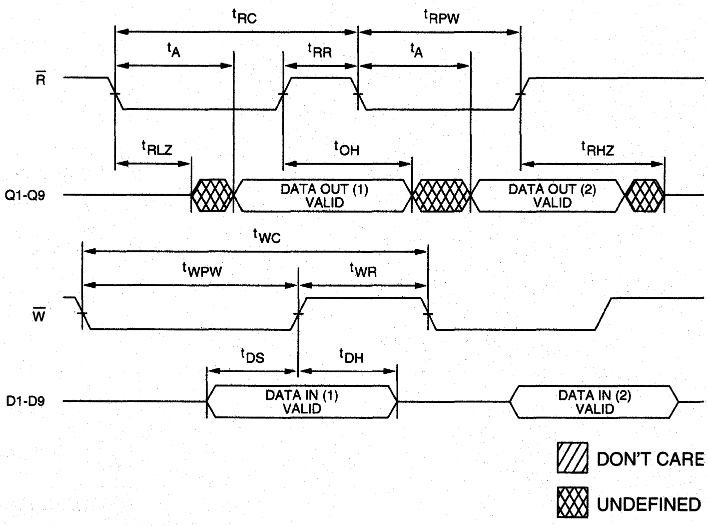


Fig. 2
OUTPUT LOAD EQUIVALENT

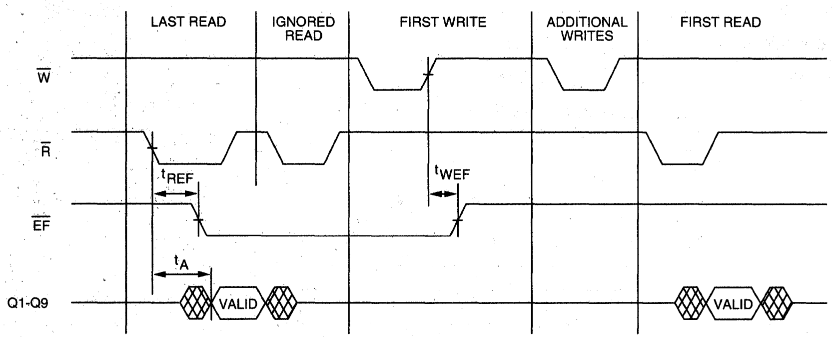
RESET



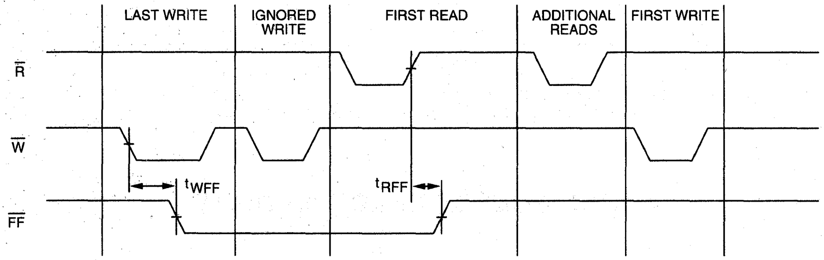
ASYNCHRONOUS READ AND WRITE



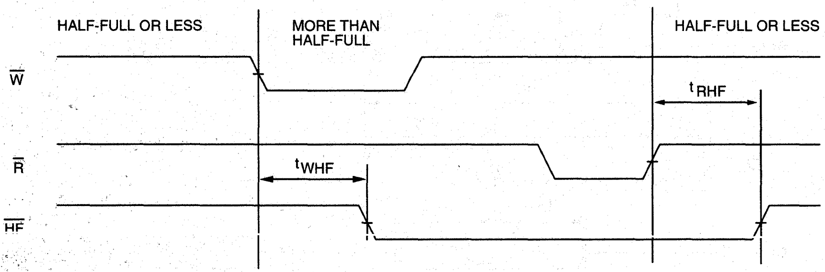
EMPTY FLAG



FULL FLAG



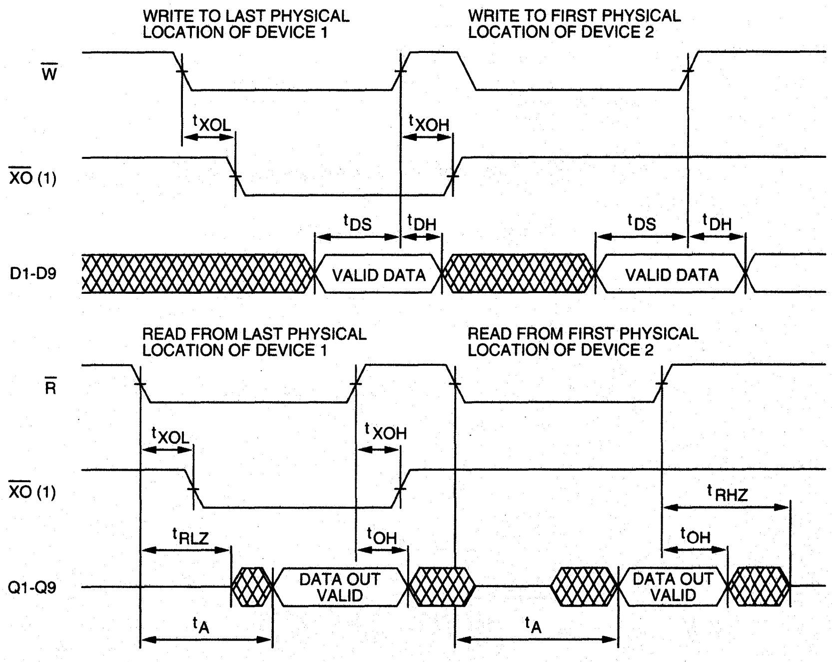
HALF-FULL FLAG



▨ DON'T CARE

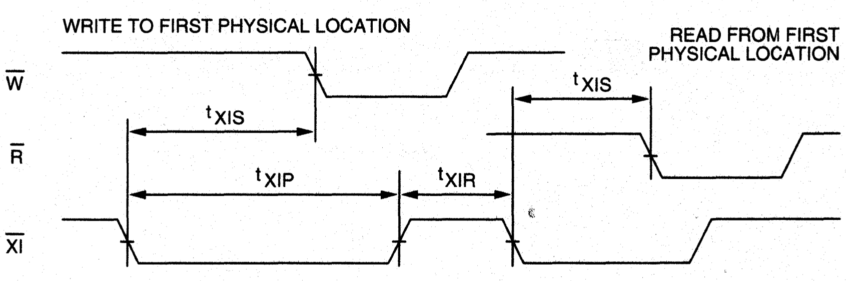
▩ UNDEFINED

EXPANSION MODE ($\overline{XO}$)



NOTE: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

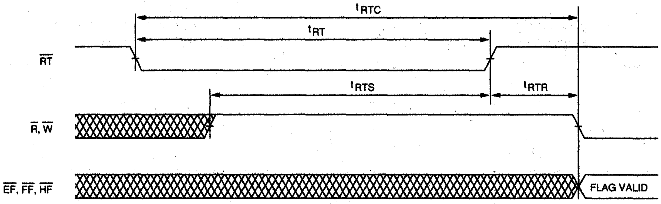
EXPANSION MODE ($\overline{XI}$)



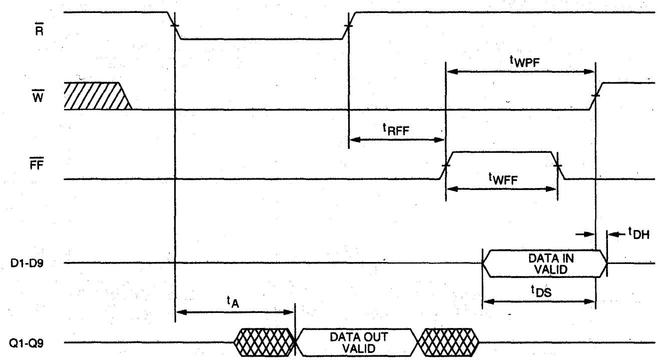
▨ DON'T CARE

▦ UNDEFINED

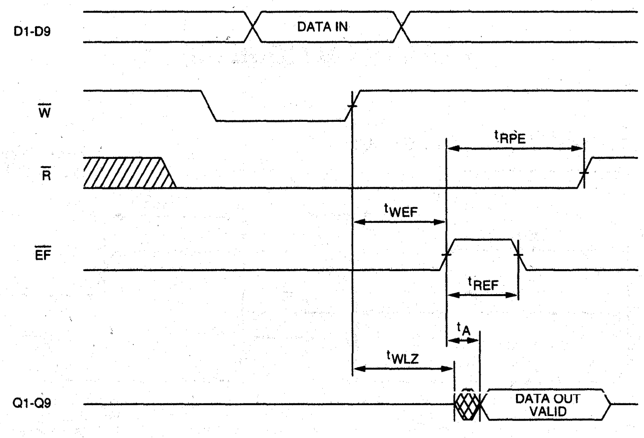
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



▨ DON'T CARE

▩ UNDEFINED

Micron Technology, Inc., reserves the right to change products or specifications without notice.

FIFO

2K x 9 FIFO

WITH PROGRAMMABLE FLAGS

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typical (standby); 350mW typical (active)
- TTL compatible inputs and outputs
- Asynchronous READ and WRITE
- Two fully configurable Almost-Full and Almost-Empty Flags
- Programmable Half-Full Flag or Full/Empty Flag option eliminates external counter requirement
- Register loading via the input or output pins
- Auto-retransmit capability in SINGLE DEVICE mode
- Fully expandable by width and depth
- Pin and function compatible with standard FIFOs

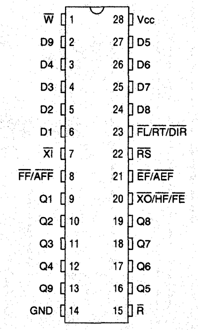
OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
PLCC	EJ
Plastic SOJ	DJ

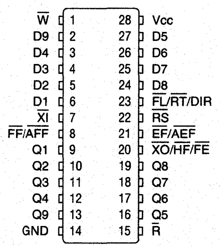
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***

PIN ASSIGNMENT (Top View)

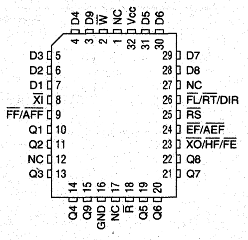
28-Pin DIP
(A-9, A-11)



28-Pin SOJ
(E-8)



32-Pin PLCC
(D-2)



GENERAL DESCRIPTION

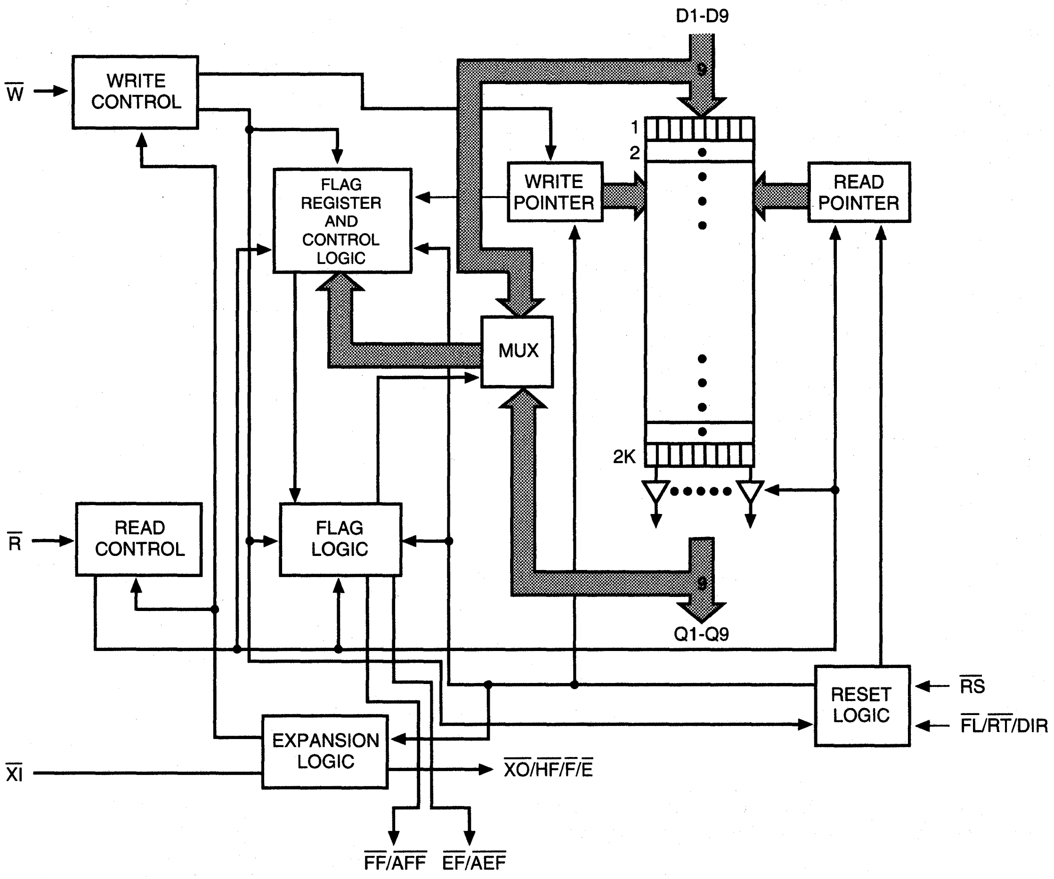
The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual-port, six-transistor memory cell with resistor loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates.

When not configured, the MT52C9022 defaults to a standard FIFO with empty ($\overline{EF}$), full ($\overline{FF}$) and half-full ($\overline{HF}$) flag pins. The MT52C9022 can be configured for programmable flags by loading the internal flag registers (as described under "Register Load Mode" on page 5-73). In configured mode, up to three flags are provided. The first two are the almost-empty flag ($\overline{AEF}$) and the almost-full flag ($\overline{AFF}$) with independently programmable offsets. The third one is either an $\overline{HF}$ or a full and empty ($\overline{FE}$) flag, depending on the bit configuration of the registers. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. The MT52C9022 is speed, function and pin compatible with lower density FIFOs from Micron.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: This pin is used to reset the device and load internal flag registers. During device reset, all internal pointers and registers are cleared.
2	1	$\overline{W}$	Input	Write: A LOW on this pin loads data into the device. The internal write pointer is incremented after the rising edge of the write input.
18	15	$\overline{R}$	Input	Read: A LOW on this pin puts the oldest valid data byte in the memory array on the output bus. The internal read pointer is incremented at the rising edge of the read signal. Outputs are in High-Z when this pin is HIGH.
8	7	$\overline{XI}$	Input	Expansion-In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$) of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$/DIR	Input	First Load/Retransmit/Direction: When in SINGLE DEVICE mode, this pin can be used to initiate a reread of the previously read data. When in REGISTER LOAD mode, the pin is used for register loading direction. When it is LOW, registers are loaded through the data output pins. When it is HIGH, registers are loaded through the data input pins. In DEPTH EXPANSION mode, this pin should be tied LOW if the device is the first one in the chain and tied HIGH if it is not the first one.
7, 6, 5, 4, 31, 30 29, 28, 3	6, 5, 4, 3, 27 26, 25, 24, 2	D1-D9	Input	Data Inputs: Data on these lines are stored in the memory array or flag registers during array WRITE or register programming, respectively.
24	21	$\overline{EF/AEF}$	Output	Empty Flag/Almost-Empty Flag: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is an Empty Flag output. When in CONFIGURED mode, it is an Almost-Empty Flag output. This pin is active LOW.
9	8	$\overline{FF/AFF}$	Output	Full Flag/Almost-Full Flags: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is a Full Flag output. When in CONFIGURED mode, it is an Almost-Full Flag output. This pin is active LOW.
23	20	$\overline{XO/HF/FE}$	Output	Expansion Out/Half Full/Full/Empty: This pin's function is determined by its operation mode. When in SINGLE DEVICE mode, this pin is either HF Flag or a Full/Empty Flag, depending on the state of the most significant bit of Almost-Full Flag Register. The pin is an $\overline{XO}$ output when the part is in DEPTH EXPANSION mode. This pin defaults to $\overline{XO/HF}$ in NONCONFIGURED mode.
10, 11, 13, 14 19, 20, 21, 22,15	9, 10, 11, 12, 16 17, 18, 19, 13	Q1-Q9	I/O	Data Output: These pins may be used for data retrieval. The pins become inputs during register loading with DIR input HIGH. The outputs are disabled (High-Z) during device idle ($\overline{R}$ = HIGH).
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	GND	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9022 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For multiple-function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing half-full flags, the* $\overline{XO}/\overline{HF}/\overline{FE}$ *pin will be shown as* $(\overline{XO})/\overline{HF}/(\overline{FE})$.

RESET

After Vcc is stable, Reset ($\overline{RS}$) must be taken LOW with both $\overline{R}$ and $\overline{W}$ HIGH to initialize the read and write pointers and flags. This also clears all internal registers. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is tied LOW. If $\overline{XI}$ is connected to $\overline{XO}/(\overline{HF})$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW and if the FIFO is not full. The WRITE cycle is initiated by the falling edge of $\overline{W}$. Data on the D1-D9 pins are latched on the rising edge. If the location to be written is the last empty location in the FIFO, $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While the $\overline{FF}$ is asserted, all writes are inhibited and previously stored data are unaffected. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^{t}RLZ after the falling edge of $\overline{R}$. Valid data will appear ^{t}A after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is full and a READ is initiated, the $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the expanded mode, the last location read from a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9022 allows the receiving device to request that data just read from the FIFO be repeated, when less than 2047 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}/(\text{DIR})$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may start reading the data from the beginning of the FIFO ^{t}RTR after $(\overline{FL})/\overline{RT}/(\text{DIR})$ is taken HIGH. Some or all flags may be affected depending on the location of the read and write pointers before and after the retransmit.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{W}$, and access time is measured from the rising edge of the empty flag.

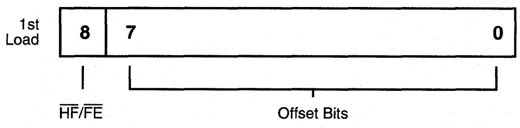
REGISTER LOAD MODE

This mode of operation is used to reset the device and program the internal flag registers. This yields an almost full and an almost-empty flag (DIP package pins 8 and 21 respectively) and a half-full or $\overline{F/E}$ flag (DIP package pin 20).

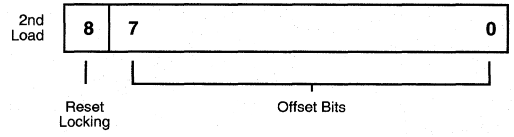
Two 9-bit internal registers have been provided for flag configuration. One is the almost-full flag register (AFFR) and the other is the almost-empty flag register (AEFR). Bit configurations of the two registers are shown below.

REGISTER SET FOR MT52C9022

Almost Full Flag Register (AFFR)



Almost Empty Flag Register (AEFR)



Note that bits 0-7 are used for offset setting. The offset value ranges from 1 to 255 words. Each offset value corresponds to a 2-byte increment. This provides a maximum offset of 510 bytes.

Bits 6 and 7 are reserved for future offset expansion. Bit 8 of the AFFR is used for configuration of $\overline{HF}/\overline{FE}$ pin. When this bit is set LOW, the HF/$\overline{FE}$ pin is configured as an $\overline{HF}$ flag output. When it is set HIGH, the HF/$\overline{FE}$ is configured as an $\overline{F/E}$ flag output.

Bit 8 of the AEFR is used for reset locking. When this bit is set LOW, subsequent device RESET or REGISTER LOADING cycles reset the device. When the bit is programmed HIGH, subsequent RESET cycles are ignored. In this mode, the flag registers can be reconfigured without device reset. The part can be reset by cycling power to the device or by writing zero (0) into bit 8 of the AEFR register followed by a DEVICE RESET or REGISTER LOAD.

Flag registers are loaded by bringing $\overline{RS}$ LOW followed by the $\overline{R}$ input. The $\overline{R}$ pin should be brought LOW ^{t}RS after the $\overline{RS}$ becomes LOW. The registers may be loaded via the input pins or the output pins depending on the status of the DIR control input. Data is latched into the registers at the rising edge of the $\overline{W}$ control pin. The first WRITE loads the AFFR while the second WRITE loads the AEFR. This loading order is fixed.

BIDIRECTIONAL MODE

Applications requiring data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by using two MT52C9022s. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both depth expansion and width expansion may be used in this mode.

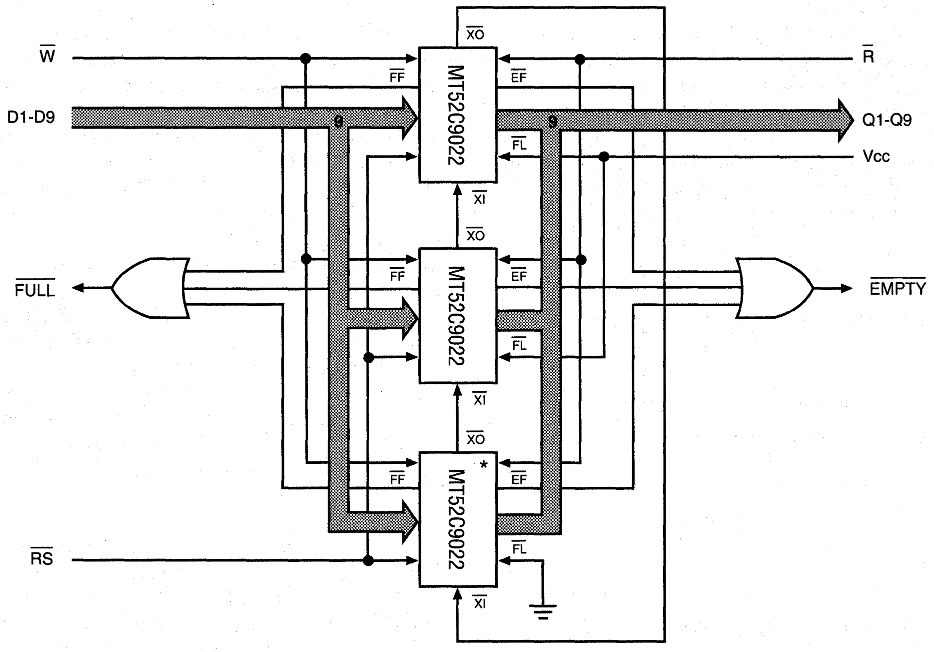
FLAG TIMING

A total of three flag outputs are provided in either CONFIGURED or NONCONFIGURED mode. In the NONCONFIGURED mode, the three flags are $\overline{HF}$ flag, $\overline{EF}$ and $\overline{FF}$. The $\overline{HF}$ flag goes active when more than half the FIFO if full. The flag goes inactive when the FIFO is half full or less.

The full and empty flags are asserted when the last byte is written to or read out of the FIFO, respectively. They are deasserted when the first byte is loaded into an empty FIFO or read out of a full FIFO, respectively. All three flag outputs are active LOW.

When the device is programmed, the $\overline{AFF}$ and $\overline{AEF}$ go active after a READ/WRITE cycle initiation of the location corresponding to the programmed offset value. For example, if the AEFR is programmed with a 10-byte offset (loading a Hex value of 05), the $\overline{AEF}$ flag goes active while reading the 10th location before the FIFO is empty. The flag goes inactive when there are 10 or more bytes left in the FIFO. The assertion timing and deassertion timing of the $\overline{AFF}$ are the same.

The third flag in the PROGRAM mode is either $\overline{HF}$ or $\overline{F/E}$ flag depending on the state of the highest bit of the AFFR. If the device is programmed for $\overline{HF}$ flag, it functions like the $\overline{HF}$ flag in NONPROGRAMMED mode. If the device is configured for $\overline{F/E}$ flag, the pin will be active (LOW) when the FIFO is either empty or full. The condition of the FIFO is determined by the state of $\overline{F/E}$ together with states of $\overline{AFF}$ and $\overline{AEF}$ (example: if $\overline{F/E}$ is LOW and $\overline{AFF}$ is LOW but $\overline{AEF}$ is HIGH, the FIFO is full).



* FIRST DEVICE LOADED

Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{\text{W}}$, $\overline{\text{R}}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9022s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{\text{XI}}$, $\overline{\text{XO}}$/($\overline{\text{HF}}$/$\overline{\text{FE}}$) and $\overline{\text{FL}}$/($\overline{\text{RT}}$/DIR). Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered by tying the $\overline{\text{XO}}$/($\overline{\text{HF}}$/$\overline{\text{FE}}$) pin of each device to the $\overline{\text{XI}}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{\text{FL}}$/($\overline{\text{RT}}$/DIR) pin grounded. The remaining devices in the chain will have $\overline{\text{FL}}$/($\overline{\text{RT}}$/DIR) tied HIGH. Upon a reset, reads and writes to all FIFOs are disabled, except the first load device. When the last physical location of the first device is written, the $\overline{\text{XO}}$/($\overline{\text{HF}}$) pin will pulse LOW on the falling edge of $\overline{\text{W}}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9022. The writes will continue to go to the second device until last location write. Then it will "pass" the write pointer to the third device. The full condition of the entire FIFO array is signaled when all the $\overline{\text{FF}}$/($\overline{\text{AFF}}$) pins are LOW.

On the last physical READ of the first device, its $\overline{\text{XO}}$ ($\overline{\text{HF}}$) will pulse again. On the falling edge of $\overline{\text{R}}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The READ pointer never overtakes the write pointer. On the last READ, an empty condition is signaled by all of the $\overline{\text{EF}}$ pins being LOW. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{\text{RS}}$	$\overline{\text{RT}}$	$\overline{\text{XI}}$	**Read Pointer**	**Write Pointer**	$\overline{\text{EF}}$	$\overline{\text{FF}}$	$\overline{\text{HF}}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{\text{RS}}$	$\overline{\text{FL}}$	$\overline{\text{XI}}$	**Read Pointer**	**Write Pointer**	$\overline{\text{EF}}$	$\overline{\text{FF}}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{\text{XO}}$ of previous device.
$\overline{\text{RS}}$ = Reset Input, $\overline{\text{FL}}/\overline{\text{RT}}$/DIR = First Load/Retransmit, $\overline{\text{EF}}$ = Empty Flag Output, $\overline{\text{FF}}$ = Full Flag Output, $\overline{\text{XI}}$ = Expansion Input, $\overline{\text{HF}}$ = Half-Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} .... -0.5V to +7.0V
Operating Temperature T_A (ambient) .... 0°C to 70°C
Storage Temperature (Plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R} \le V_{IL}$; V_{CC} = MAX f = MAX = $1/{}^tRC$ Outputs Open	I_{CC}	140	130	120	100	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R} \ge V_{IH}$; V_{CC} = MAX f = MAX = $1/{}^tRC$	I_{SB1}	15	15	15	15	mA	
	$\overline{W}$, $\overline{R} \ge V_{CC}$ -0.2; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2 $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

(V_{IN} = 0V; V_{OUT} = 0V)

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	8	pF	4
Output Capacitance		C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured and nonconfigured modes) (0°C $\leq T_A \leq$ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Shift frequency	^{t}RF		40		33.3		28.5		22.2	MHz	
READ cycle time	^{t}RC	25		30		35		45		ns	
Access time	^{t}A		15		20		25		35	ns	6
READ recovery time	^{t}RR	10		10		10		10		ns	
READ pulse width	^{t}RPW	15		20		25		35		ns	
READ LOW to Low-Z	^{t}RLZ	5		5		5		5		ns	7
READ HIGH to High-Z	^{t}RHZ		15		15		18		20	ns	7
Data HOLD from $\overline{R}$ HIGH	^{t}OH	5		5		5		5		ns	
WRITE Cycle											
WRITE cycle time	^{t}WC	25		30		35		45		ns	
WRITE pulse width	^{t}WPW	15		20		25		35		ns	6
WRITE recovery time	^{t}WR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^{t}WLZ	5		5		5		5		ns	5, 7
Data setup time	^{t}DS	10		12		15		18		ns	
Data hold time	^{t}DH	0		0		0		0		ns	
RETRANSMIT Cycle											
RESTRANSMIT cycle time	^{t}RTC	25		30		35		45		ns	
RESTRANSMIT pulse width	^{t}RT	15		20		25		35		ns	
RESTRANSMIT recovery time	^{t}RTR	10		10		10		12		ns	
RESTRANSMIT setup time	^{t}RTS	15		20		25		35		ns	
RESET Cycle											
RESET cycle time (no register programming)	^{t}RSC	25		30		35		45		ns	
RESET pulse width	^{t}RSP	15		20		25		35		ns	6
RESET recovery time	^{t}RSR	10		10		10		10		ns	
$\overline{RS}$ LOW to $\overline{R}$ LOW	^{t}RS	15		20		25		35		ns	
RESET and register programming cycle time	^{t}RSPC	85		100		115		145		ns	
$\overline{R}$ LOW to DIR valid (register load cycle)	^{t}RDV	5		5		5		5		ns	
$\overline{R}$ LOW to register load	^{t}RW	10		10		10		10		ns	
$\overline{W}$ HIGH to $\overline{RS}$ LOW	^{t}WRS	0		0		0		0		ns	
$\overline{R}$ HIGH to $\overline{RS}$ LOW	^{t}RRS	0		0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured mode only) (T_A = 0°C to 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Mode Timing											
$\overline{\text{R/W}}$ to $\overline{\text{XO}}$ LOW	^{t}XOL		20		20		25		35	ns	
$\overline{\text{R/W}}$ to $\overline{\text{XO}}$ HIGH	^{t}XOH		20		20		25		35	ns	
$\overline{\text{XI}}$ pulse width	^{t}XIP	15		20		25		35		ns	
$\overline{\text{XI}}$ setup time to $\overline{\text{R/W}}$	^{t}XIS	10		12		15		15		ns	
$\overline{\text{XI}}$ recovery time	^{t}XIR	10		10		10		10		ns	
Flags Timing											
$\overline{\text{W}}$ HIGH to Flags Valid	^{t}WFV		15		15		15		15	ns	
$\overline{\text{RS}}$ to $\overline{\text{AEF}}$, $\overline{\text{EF}}$ LOW	^{t}EFL		25		30		35		45	ns	
$\overline{\text{R}}$ LOW to $\overline{\text{EF}}$ LOW	^{t}REF		20		20		25		30	ns	
$\overline{\text{W}}$ HIGH to $\overline{\text{EF}}$ HIGH	^{t}WEF		20		20		25		30	ns	
$\overline{\text{R}}$ HIGH after $\overline{\text{EF}}$ HIGH	^{t}RPE	15		20		25		35		ns	5
$\overline{\text{RS}}$ to $\overline{\text{AFF}}$, $\overline{\text{HF}}$, $\overline{\text{FF}}$ HIGH	^{t}HFH, ^{t}FFH		25		30		35		45	ns	
$\overline{\text{R}}$ HIGH to $\overline{\text{FF}}$ HIGH	^{t}RFF		15		20		25		30	ns	
$\overline{\text{W}}$ LOW to $\overline{\text{FF}}$ LOW	^{t}WFF		20		20		25		30	ns	
$\overline{\text{W}}$ HIGH after $\overline{\text{FF}}$ HIGH	^{t}WPF	15		20		25		35		ns	5
$\overline{\text{W}}$ LOW to $\overline{\text{HF}}$ LOW	^{t}WHF		25		30		35		45	ns	
$\overline{\text{R}}$ HIGH to $\overline{\text{HF}}$ HIGH	^{t}RHF		25		30		35		45	ns	
$\overline{\text{R}}$ HIGH to $\overline{\text{AFF}}$ HIGH	^{t}RAFF		25		30		35		45	ns	
$\overline{\text{W}}$ LOW to $\overline{\text{AFF}}$ LOW	^{t}WAFF		25		30		35		45	ns	
$\overline{\text{R}}$ LOW to $\overline{\text{AEF}}$ LOW	^{t}RAEF		25		30		35		45	ns	
$\overline{\text{W}}$ HIGH to $\overline{\text{AEF}}$ HIGH	^{t}WAEF		25		30		35		45	ns	

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

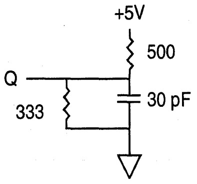
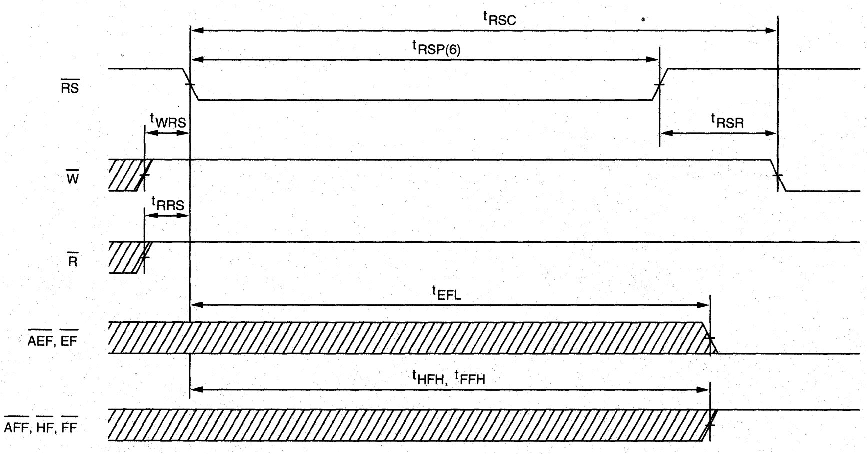


Figure 2
OUTPUT LOAD EQUIVALENT

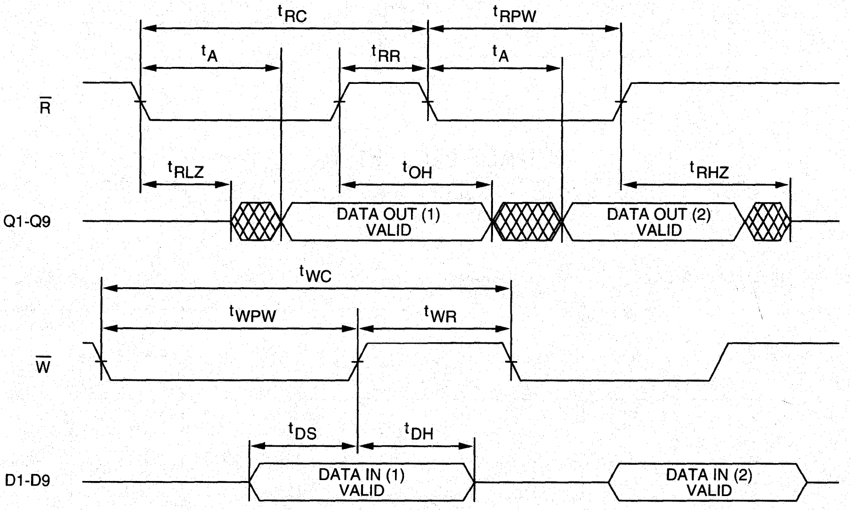
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.
7. Values guaranteed by design, not currently tested.
8. $\overline{\text{R}}$ and DIR signals must go inactive (HIGH) coincident with $\overline{\text{RS}}$ going inactive (HIGH).
9. DIR must become valid before $\overline{\text{W}}$ goes active (LOW).

RESET
(WITH NO REGISTER PROGRAMMING)



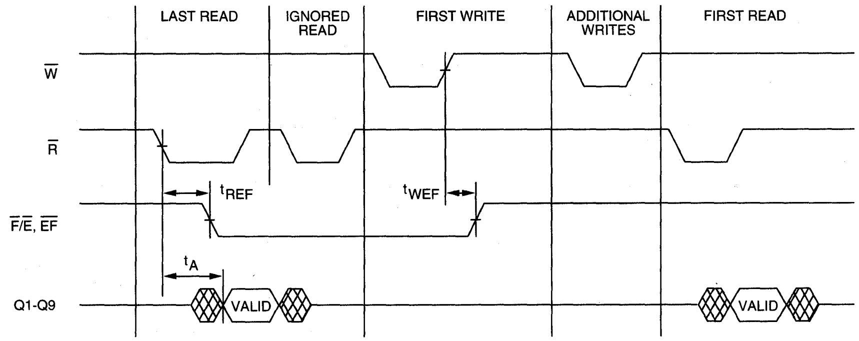
ASYNCHRONOUS READ AND WRITE



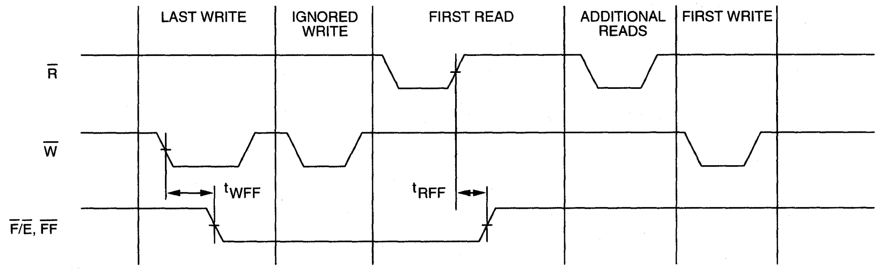
▨ DON'T CARE

▩ UNDEFINED

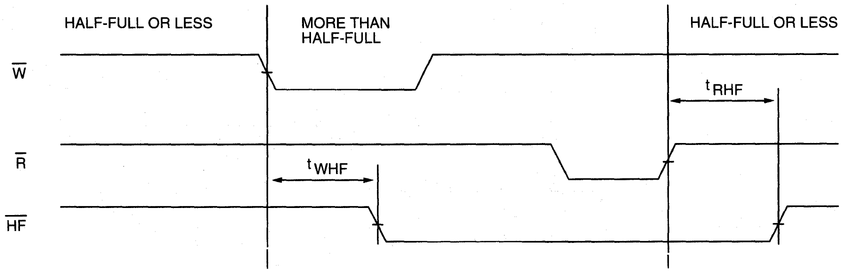
EMPTY FLAG



FULL FLAG



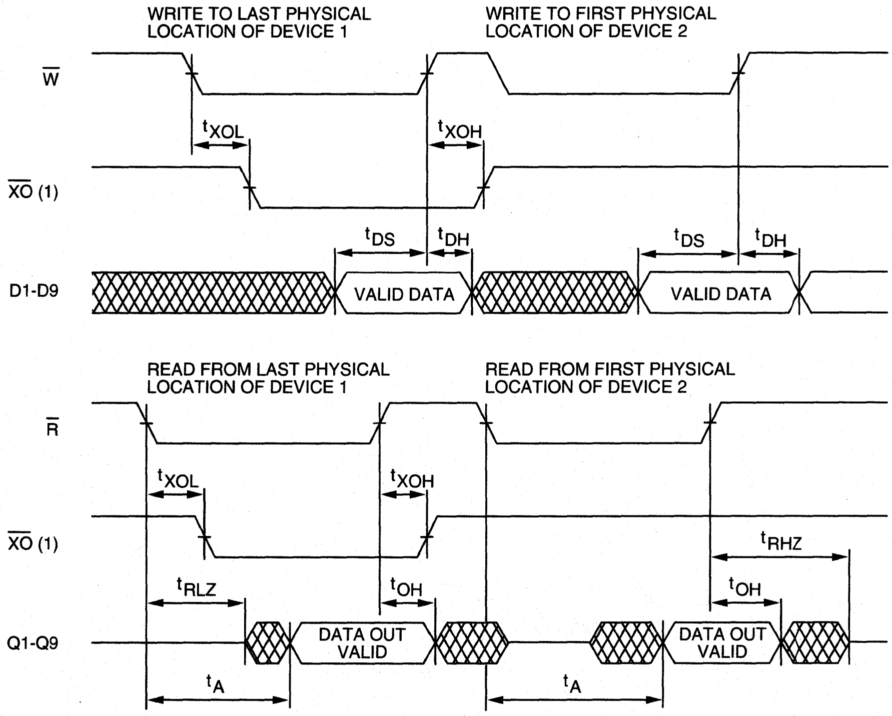
HALF-FULL FLAG
(FOR CONFIGURED AND NONCONFIGURED MODES)



▨ DON'T CARE

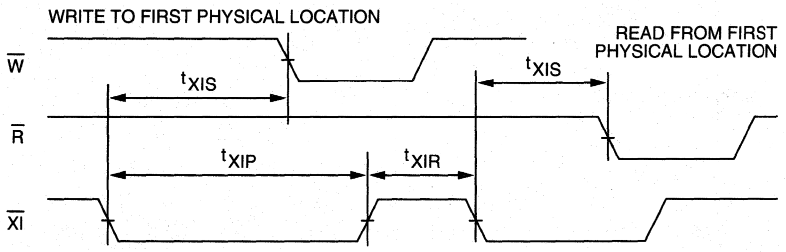
▩ UNDEFINED

EXPANSION MODE ($\overline{XO}$)



NOTE: 1. $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

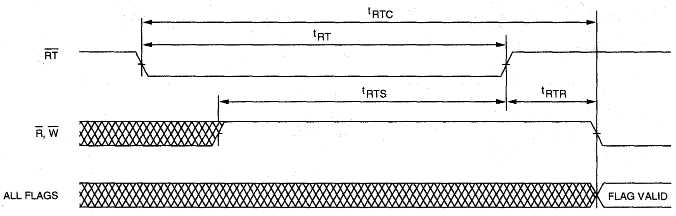
EXPANSION MODE ($\overline{XI}$)



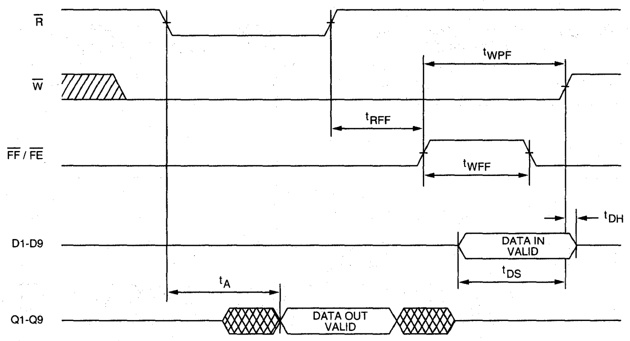
▨ DON'T CARE

▩ UNDEFINED

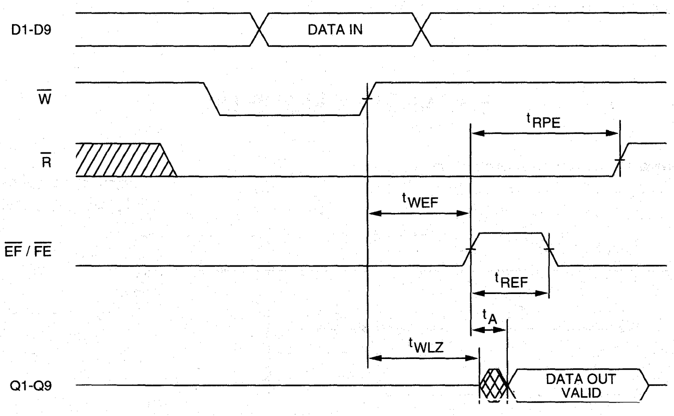
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



▨ DON'T CARE

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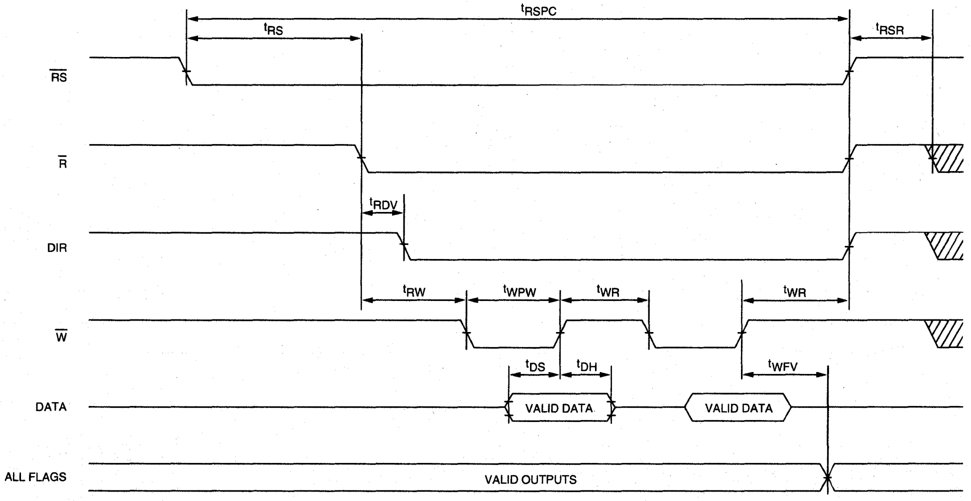
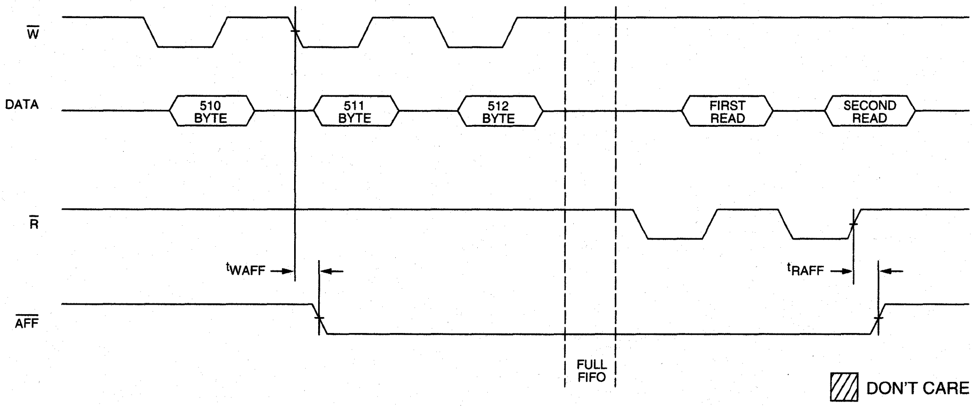
RESET/REGISTER PROGRAMMING CYCLE TIME[8, 9]



ALMOST-FULL FLAG (2-BYTE OFFSET)

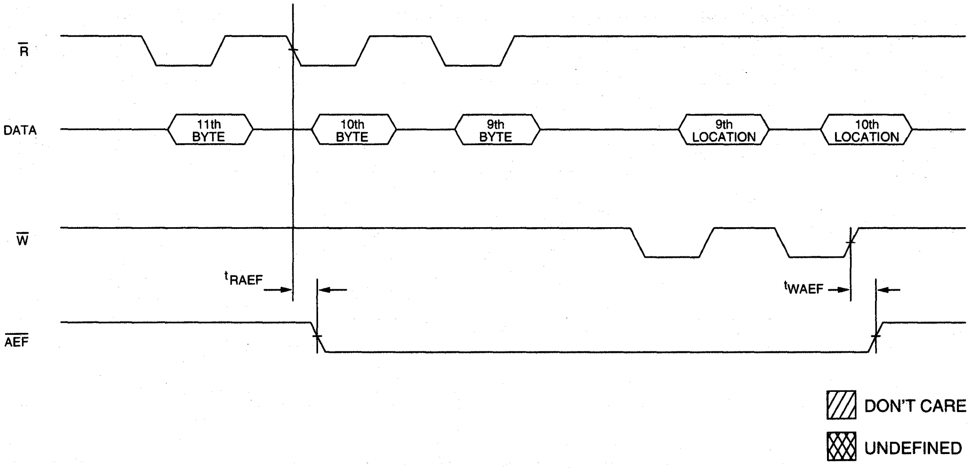


▨ DON'T CARE

▩ UNDEFINED

Micron Technology, Inc., reserves the right to change products or specifications without notice.

ALMOST-EMPTY FLAG (10-BYTE OFFSET)



APPLICATION/TECHNICAL NOTE SELECTION GUIDE

MICRON
TECHNOLOGY, INC.

TN-00-01

TECHNICAL NOTE

MOISTURE ABSORPTION IN PLASTIC PACKAGES

INTRODUCTION

All plastic integrated circuit packages have a tendency to absorb moisture. This moisture can vaporize when subjected to the heat associated with solder reflow operations when surface-mounting the devices. Vaporization creates internal stresses that can cause the plastic molding compound to crack. Cracks in the package allow contamination to penetrate to the die and potentially reduce the reliability of the semiconductor device. The cracking process associated with surface-mountable devices is commonly referred to as the "popcorn effect."

Cracks in the plastic pose several reliability concerns. The moisture path to the die is shortened, allowing ion migration or corrosion to occur more readily. Minor cracks, that might not be harmful initially, could propagate with time, resulting in a longer-term functional failure in the field.

Since plastic packages absorb moisture, care must be taken to prevent exposure for any long period prior to surface-mounting the devices on the printed circuit board. If exposed to excessive moisture, the devices should be baked to remove moisture prior to solder reflow operations.

This technical note describes the shipping procedures that ensure Micron customers will receive memory devices that do not exhibit the "popcorn effect." It also discusses Micron's recommendations for baking the devices if they are exposed to excessive moisture.

ABSORPTION CHARACTERISTICS

Micron's extensive testing empirically characterizes the moisture absorption characteristics of plastic packages. As the plastic takes on moisture, the weight of the device increases. Micron employs a standard procedure for weighing the device before and after it is exposed to moisture. We calculate the percentage of weight gain to determine the relative efficiency of different packaging techniques used for shipping devices.

MICRON PROCEDURES

Micron has eliminated any chance of having "popcorn" failures with surface-mount packages by shipping all of our surface-mount devices in sealed bags containing a desiccant. Devices stored in these bags show no measurable weight gain when subjected to a high humidity environment for long time periods.

DEVICE STORAGE

To prevent device failure due to the "popcorn effect," store plastic surface-mount packages carefully before PCB assembly. Micron has run tests on devices that have been exposed to 50 percent humidity outside of their shipping containers for time intervals from six months to one year and no failures have been recorded.

Any concerns about the moisture absorption can be eliminated by storing the devices in Micron's shipping bags. We designed these containers to prevent the passage of water vapor for long periods of time.

DEVICE BAKING

If devices have been removed from their shipping containers and exposed to high levels of moisture, Micron recommends a device bake-out procedure be performed before surface mounting. This bake-out may be accomplished by placing the parts in a tray and baking in an oven for 160 hours at 40° C. Any moisture is driven out of the devices during the exposure to the heat.

Moisture may be removed faster by baking at 100° C for 24 hours.

SUMMARY

1. All plastic packages absorb moisture when exposed to high levels of humidity for long time intervals.
2. Micron devices have not exhibited any "popcorn effect" when exposed to 50 percent humidity for long time periods.
3. Micron ships all surface-mount packages in containers that prevent absorption of moisture.
4. If devices have been removed from their shipping containers and exposed to excessive moisture, they should be baked before being surface-mounted.

REFERENCES

"Moisture Absorption and Mechanical Performance of Surface Mountable Plastic Packages": Bhattacharyya, B. K. : et. al. : 1988 Proceedings of the 38th Electronics Components Conference.

"Analysis of Package Cracking During Reflow Soldering Process": Kitano, M., et. al. : 26th Annual Proceeding, Reliability Physics, 1988.

"Moisture Induced Package Cracking in Plastic Encapsulated Surface Mounted Components During Solder Reflow Process": Lin, R., et. al. : 26th Annual Proceeding, Reliability Physics, 1988.

NEW ■ APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

TAPE AND REEL PROCEDURES

GENERAL DESCRIPTION

Tape and reel is becoming the packaging and shipment method of choice for Micron's surface-mounted memory devices. Tape and reel minimizes the handling of components by directly interfacing with automatic pick-and-place machines.

Micron supports the Electronic Industries Association's (EIA) standardization of tape and reel specifications number 481A. The intent of this technical note is to describe Micron's status in support of the EIA standard.

Table 1
MICRON TAPE SIZES AND DEVICES PER REEL

COMPONENT	TAPE WIDTH (W) mm	PITCH (P) mm	DEVICES PER 13-INCH REEL
PLCC			
18 Pin	24	12	1,000
52 Pin	32	16	500
SOJ (300 mil)			
20/26 Pin	24	12	1,000
24 Pin	24	12	1,000
28 Pin	24	12	1,000
SOJ (400 mil)			
28 Pin	32	16	500
32 Pin	44	16	500
40 Pin	44	16	500

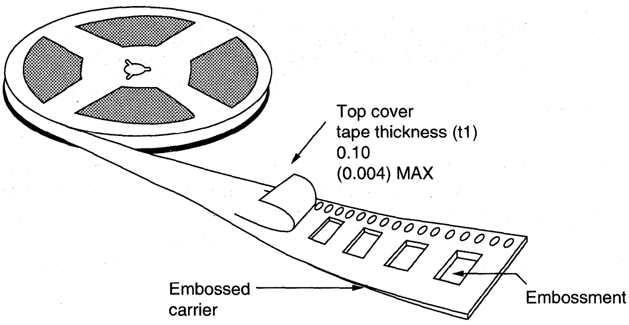


Figure 1
REEL

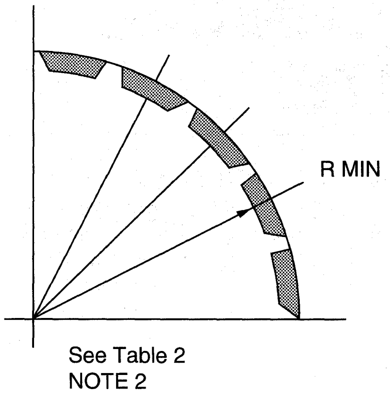
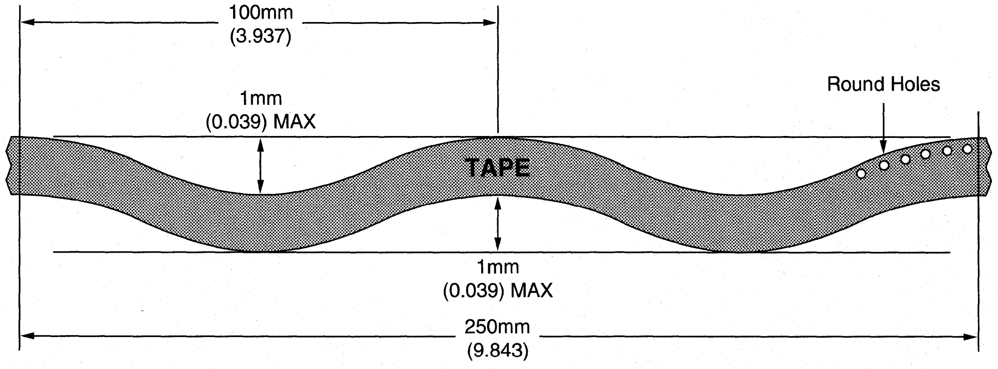


Figure 2
BENDING RADIUS



Allowable camber to be 1mm/100mm nonaccumulative over 250mm.

Figure 3
CAMBER (TOP VIEW)

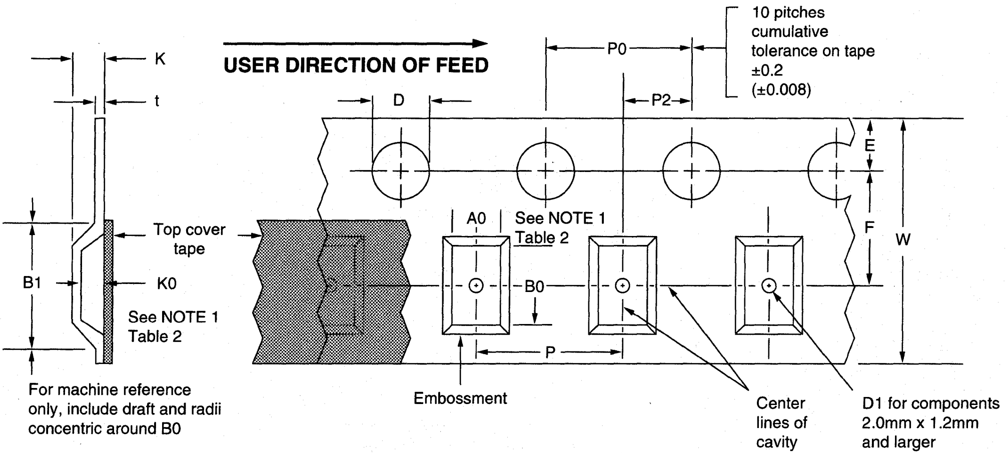


Figure 4
EMBOSSED CARRIER DIMENSIONS
(24mm Tape Only)

Table 2
24mm EMBOSSED TAPE DIMENSIONS[3]

TAPE SIZE	D	E	P0	t (MAX)	A0, B0, K0
24mm	$1.5^{+0.10}_{-0.00}$ (0.59) $^{+0.004}_{-0.000}$	1.75 (0.069 ±0.004)	4 (0.157 ±0.004)	0.400 (0.16)	NOTE 1

TAPE SIZE	B1 (MAX)	D1 (MIN)	F	K (MAX)	P2	R (MIN)	W
24mm	20.1 (0.791)	1.5 (0.059)	11.5 ±0.10 (0.453 ±0.004)	6.5 (0.256)	2 ±0.10 (0.079 ±0.004)	50 (1.969)	24 ±0.30 (0.945 ±0.012)

TAPE SIZE	P					
	4±0.10 (0.157±0.004)	**8±0.10 (0.315±0.004)**	**12±0.10 (0.472±0.004)**	**16±0.10 (0.630±0.004)**	**20±0.10 (0.787±0.004)**	**24±0.10 (0.945±0.004)**
24mm			x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters (inches).

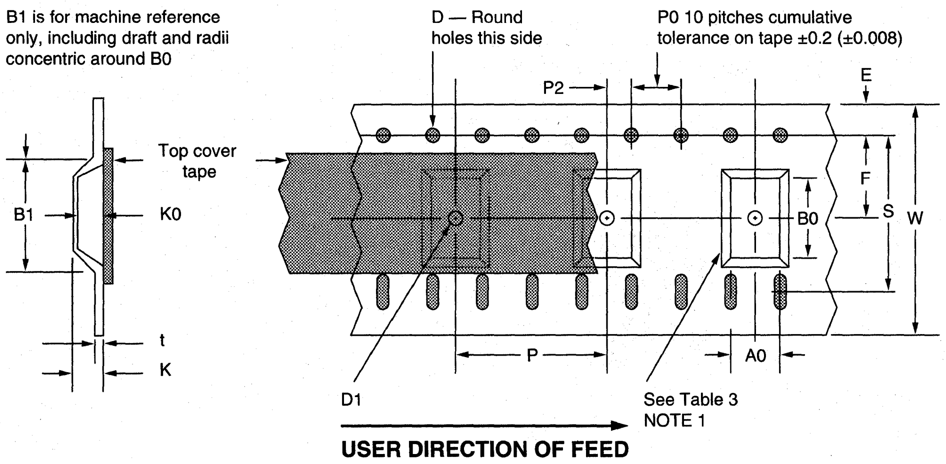


Figure 5
EMBOSSED CARRIER DIMENSIONS
(32 and 44mm Tape Only)

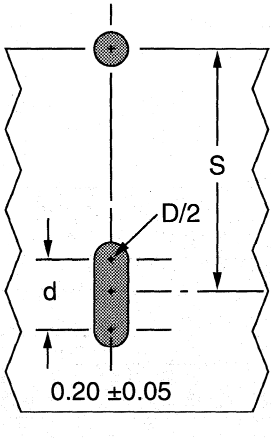


Figure 6
DETAIL ELONGATED HOLE

Table 3
32 AND 44mm EMBOSSED TAPE[3]

TAPE SIZE	D	D1 (MIN)	E	K (MAX)	P0	t (MAX)	A0, B0, K0
32 and 44mm	$1.5^{+0.10}_{+0.00}$ $(0.059)^{+0.004}_{+0.000}$	2 (0.079)	1.75 ±0.10 (0.069 ±0.004)	10 (0.394)	4 ±0.10 (0.156 ±0.004)	0.500 (0.20)	NOTE 1

TAPE SIZE	B1 (MAX)	F	P2	S	W	R (MIN)
32mm	23 (0.906)	14.2 ±0.10 (0.559 ±0.004)	2 ±0.10 (0.079 ±0.004)	28.4 ±0.10 (1.118 ±0.004)	32 ±0.30 (1.26 ±0.012)	50 (1.973)
44mm	35 (1.378)	20.2 ±0.15 (0.795 ±0.006)	2 ±0.15 (0.079 ±0.006)	40.4 ±0.10 (1.591 ±0.004)	44.8 ±0.30 (1.732 ±0.12)	50 (1.973)

TAPE SIZE	P							
	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)	28 ±0.10 (1.102 ±0.004)	32 ±0.10 (1.26 ±0.004)	36 ±0.10 (1.417 ±0.004)	40 ±0.10 (1.575 ±0.004)	44 ±0.10 (1.732 ±0.004)
32mm	x	x	x	x	x			
44mm			x	x	x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters (inches).

MICRON
TECHNOLOGY, INC.

TN-05-02

TECHNICAL NOTE

SRAM BUS CONTENTION DESIGN CONSIDERATIONS

INTRODUCTION

High-speed SRAM memory systems normally share a common data bus with other memory devices, processors and memory management or caching devices. All of these devices are required to control data bus at one time or another. Turning off a device that is driving the bus before a new device takes control of the bus can be a difficult design problem when these systems are operating at minimum cycle times.

When two or more devices are driving the bus at the same time, a conflict known as "bus contention" occurs. This technical note discusses bus contention design issues and points out features in the design of Micron's fast SRAMs to help minimize bus contention problems.

BUS CONTENTION EFFECTS

System-design problems caused by bus contention are difficult to analyze. The effects are transient, normally not longer than 5ns. The most visible result of bus contention is observed as noise on power-supply lines and data lines connecting the contending devices. While these conflicts are not destructive, they potentially reduce long-term system reliability. However, in most cases, they do not affect system performance when all the active components are MOS.

MOS devices are inherently self-current limiting. As the current through a MOS transistor increases, the transistor heats up and its gain decreases. Bipolar transistors have the opposite behavior. When a bipolar transistor's temperature

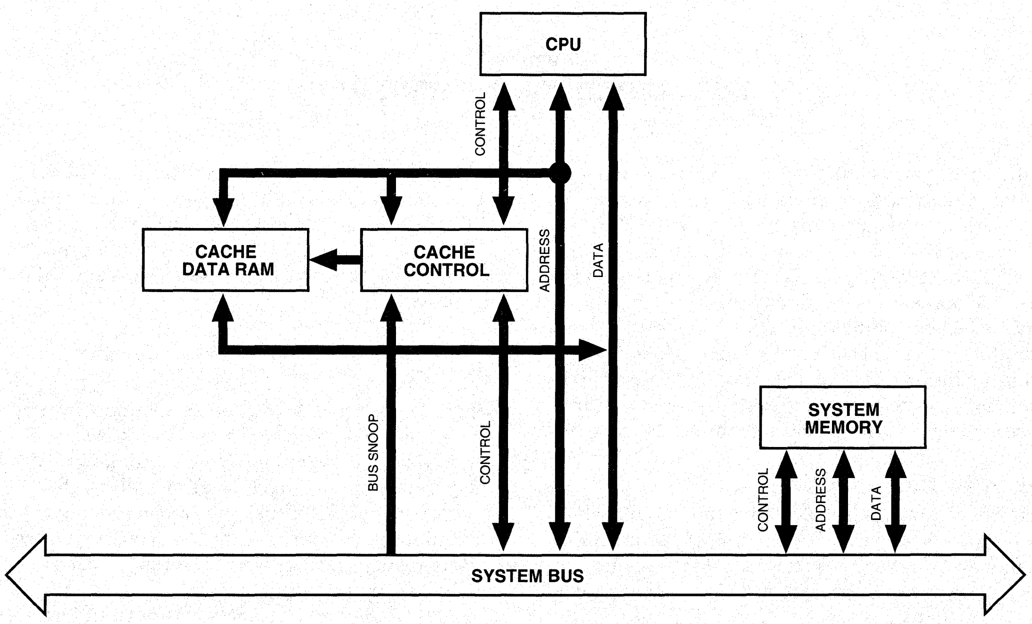


Figure 1
BLOCK DIAGRAM OF A CACHE MEMORY SYSTEM

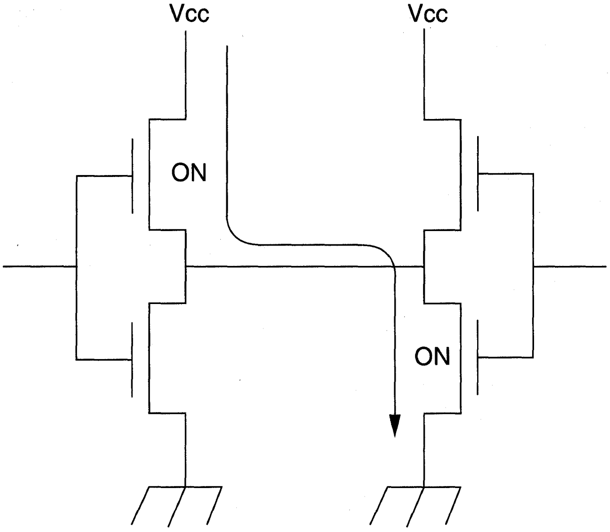


Figure 2
BUS CONTENTION CURRENT PATH

is elevated, the gain of the device increases, making it possible for the current through the transistor to increase to a destructive level. This phenomenon is known as "thermal runaway." If CMOS SRAMs share any data lines with bipolar or BiCMOS output devices, the system should be designed to eliminate any possibility of bus contention.

Figure 2 is a schematic diagram of two contending SRAM output buffers. A high current path has been created by two SRAM output buffers. The current is flowing between the "on" transistor connected to Vcc in the buffer on the left and the transistor connected to ground in the buffer on the right.

SRAM SPECIFICATIONS

The critical parameters for calculating the amount of bus contention for a high-speed SRAM system design is the time it takes for a device to go to Low impedance (logic 1 or 0) on its output versus the time required for a contending output to go to high impedance. A typical SRAM has three control signals; chip enable (CE), write enable (WE) and output enable (OE). ^{t}LZCE, ^{t}LZWE and ^{t}LZOE are the times it takes for the outputs to become active or low impedance upon the assertion of CE, WE and OE. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are the times required for the outputs to become inactive or high impedance after CE, WE and OE are removed. These times are shown in the READ and WRITE cycle timing diagram (Figure 3). A preliminary review of a fast SRAM data sheet would imply that the worst case for bus contention could be calculated from the equation:

$$^tC = {}^tHZ\ (MAX) - {}^tLZ\ (MIN)$$

where ^{t}C is equal to the bus-contention overlap time. For an output enable change in an SRAM rated at 20ns access time, ^{t}HZ = 7ns and ^{t}LZ = 2ns; therefore ^{t}C = 5ns. If this calculation is correct, there would be a serious bus contention problem. Thus, for a system running with a 20ns cycle, almost 25 percent of the total cycle would be lost to bus contention and there would be a large increase in power dissipation in the output buffers.

Happily, the previous analysis is not valid because ^{t}HZ maximum occurs at completely different test conditions than ^{t}LZ minimum. ^{t}HZ maximum is worst-case at the highest operating temperature and the lowest power-supply voltage. On a commercial data sheet, this would be at 70° C and 4.5V. ^{t}LZ minimum is specified at the lowest operating

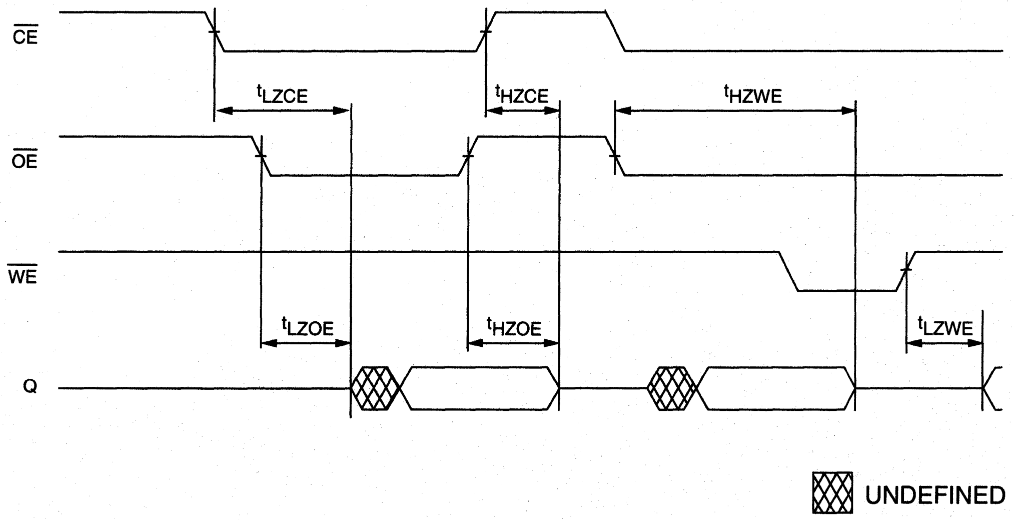


Figure 3
READ AND WRITE CYCLE TIMING

temperature and the highest voltage. Again, on the commercial data sheet, this would be 0° C and 5.5V. It is not possible for two SRAMs on the same board to be at such diverse temperatures and voltages. In a "real world" system — that is, one with an equal operating environment for temperature and power supply voltage — ${}^{t}HZ$ - ${}^{t}LZ$ is approximately 0.2ns.

Futhermore, Micron fast SRAMs have been designed to insure the outputs always turn off faster than the they turn on when operating at the same voltage and temperature: ${}^{t}HZ < {}^{t}LZ$. Since the devices will normally be mounted on the same board, the bus contention associated with the SRAM control signals has been minimized.

Care must be taken when mutiple vendors' SRAMs share the bus. An analysis of the output turn-off time must be done under the same operating and temperature conditions to insure that bus contention between the devices is minimized.

MICRON TECHNOLOGY, INC. **TN-05-03**

TECHNICAL NOTE

SRAM CAPACITIVE LOADING

INTRODUCTION

Many high-speed 16-bit and 32-bit microprocessor systems require fast SRAMs. SRAMs are used either in main memory or caching subsystems. In either case, the SRAMs are typically required to interface with a system bus that is shared by one or more microprocessors, several I/O devices and other types of memory (ROM, EPROM, etc.).

Even though transceivers and/or buffers interface with the actual bus, SRAMs are typically required to drive loads larger than what is specified in the data sheet timing parameters. Hence, the access time must be derated to reflect the actual performance of the SRAM under these circumstances.

SIMILARITY BETWEEN SRAM FAMILIES

Micron's 16K, 64K, 256K and 1 Meg SRAM families all have the same size output transistors and output architecture. Hence, all devices will have the same drive characteristics. The actual data presented in this technical note are derived from the 256K SRAM family.

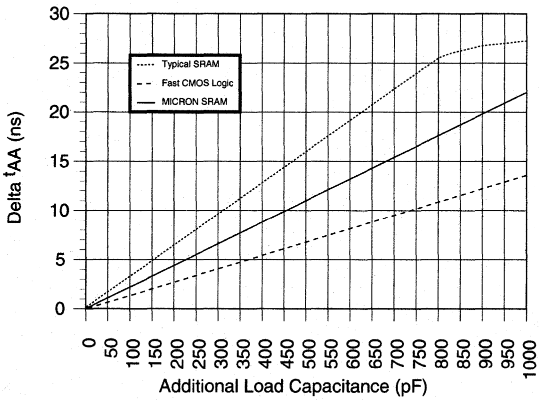


Figure 1
INCREASED ACCESS TIME vs. ADDITIONAL OUTPUT LOADING

COMPARISON OF DEVICES

Figure 1 compares the effects of capacitive loading on the Micron SRAM family with SRAMs from a typical memory supplier and discrete CMOS logic, designed to drive heavy loads. The graph illustrates the additional access time required to drive various capacitive loads.

As expected, the Micron SRAM family does not drive heavy loads as well as the discrete CMOS logic, but does drive faster than the typical SRAM from other suppliers.

The graph line which represents the Micron SRAM family is based on data gathered on the Micron 256K SRAM. Access time measurements were taken with the SRAM subjected to various capacitive loads. In the range covered, the change in access time was seen to be a linear function of the capacitive load. The following equation may be used to determine the access time required for a specific load.

$$T_{AA}(\text{actual}) = T_{AA}(\text{data sheet}) + T_{AA}(\text{additional})$$

$$T_{AA}(\text{additional})\ (\text{ns}) = .022\ (\text{ns/pF})\ C_a$$

This applies where C_a is the additional capacitive load expressed in picofarads (pF). For example, the access time needed for a 100pF total capacitive load is:

$$\begin{aligned}&T_{AA}(\text{actual}) = 20\text{ns} + T_{AA}(\text{additional}) =\\&20\text{ns} + .022 * (\text{total load - rated load}) =\\&20\text{ns} + .022\text{ns/pF} * (100\text{pF} - 30\text{pF}) =\\&20\text{ns} + 1.5\text{ns} = 21.5\text{ns}\end{aligned}$$

SUMMARY

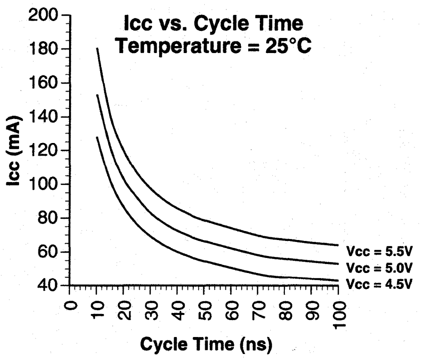
The SRAM timing specifications of all major vendors are based upon an industry standard capacitive load of 30pF. In most applications, the SRAMs are required to drive much larger capacitive loads. In addition, today's designs are implemented around higher frequencies. This requires the system timing to be more precise; hence, loading becomes a more important issue. Understanding how the SRAM will perform under specific loading conditions may result in a more reliable design.

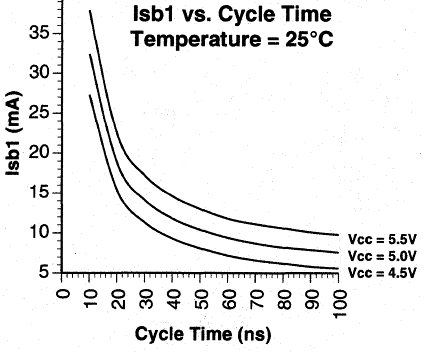
TECHNICAL NOTE

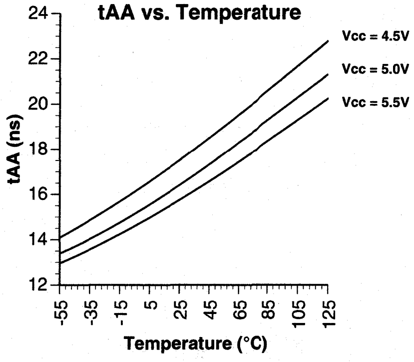
1 MEG FAST SRAM TYPICAL OPERATING CURVES

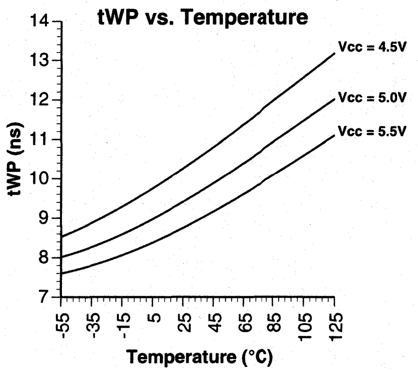
INTRODUCTION

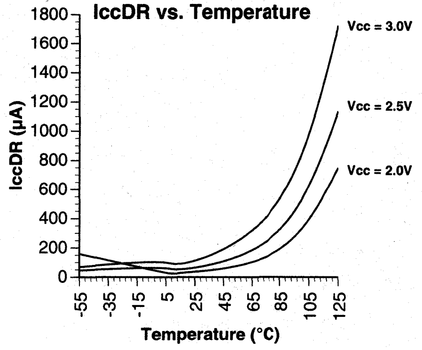
These curves represent the typical operating characteristics of Micron's 1 Meg, 25ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.

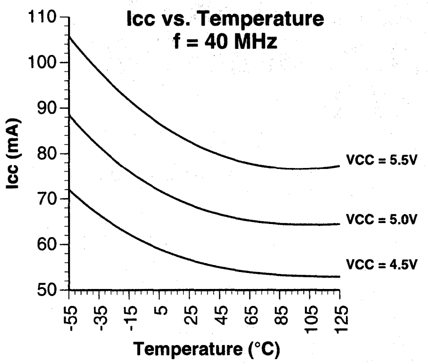


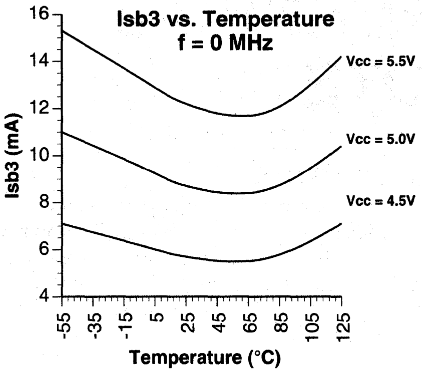


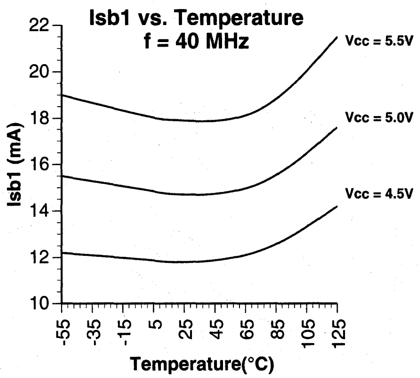


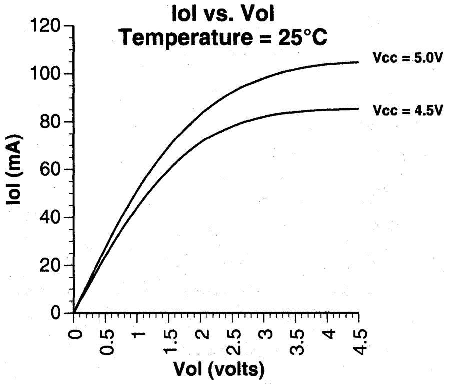


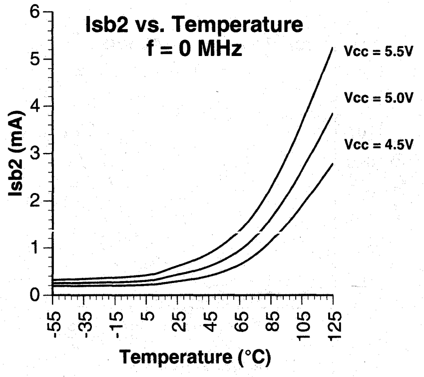


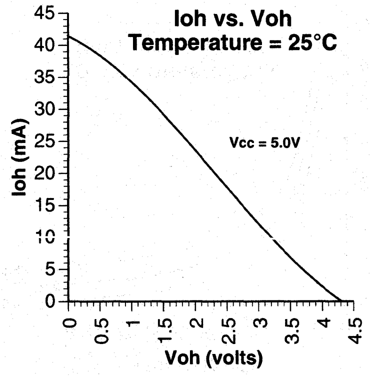

Icc vs. Temperature
f = 40 MHz
Icc (mA)
110
100
90
80
70
60
50
VCC = 5.5V
VCC = 5.0V
VCC = 4.5V
-55
-35
-15
5
25
45
65
85
105
125
Temperature (°C)


Isb3 vs. Temperature
f = 0 MHz
Isb3 (mA)
16
14
12
10
8
6
4
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
-55
-35
-15
5
25
45
65
85
105
125
Temperature (°C)


Isb1 vs. Temperature
f = 40 MHz
Isb1 (mA)
22
20
18
16
14
12
10
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
-55
-35
-15
5
25
45
65
85
105
125
Temperature(°C)


Iol vs. Vol
Temperature = 25°C
Iol (mA)
120
100
80
60
40
20
0
Vcc = 5.0V
Vcc = 4.5V
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
Vol (volts)


Isb2 vs. Temperature
f = 0 MHz
Isb2 (mA)
6
5
4
3
2
1
0
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
-55
-35
-15
5
25
45
65
85
105
125
Temperature (°C)


Ioh vs. Voh
Temperature = 25°C
Ioh (mA)
45
40
35
30
25
20
15
10
5
0
Vcc = 5.0V
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
Voh (volts)

MICRON TECHNOLOGY, INC.

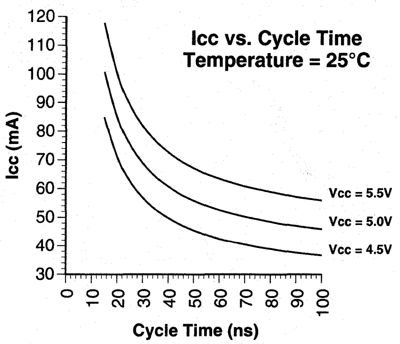
TN-05-07

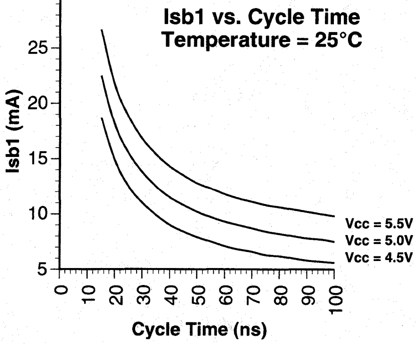
TECHNICAL NOTE

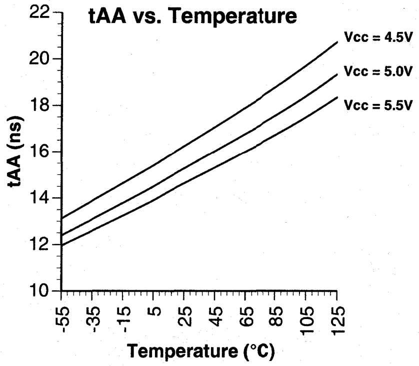
256K FAST SRAM TYPICAL OPERATING CURVES

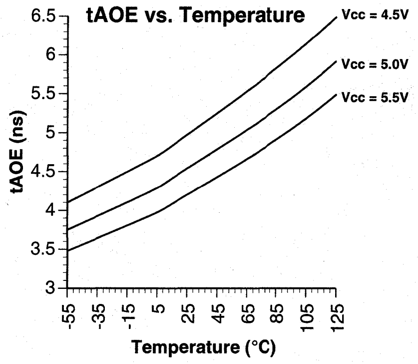
INTRODUCTION

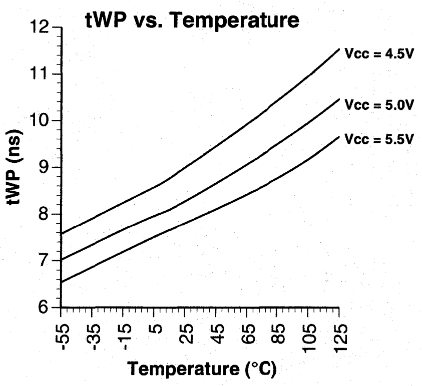
These curves represent the typical operating characteristics of Micron's 256K, 20ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.



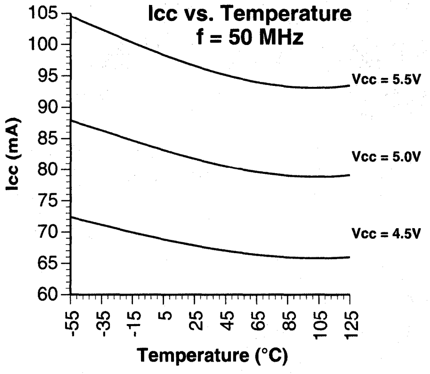


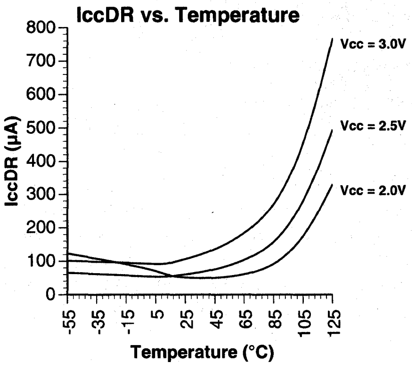


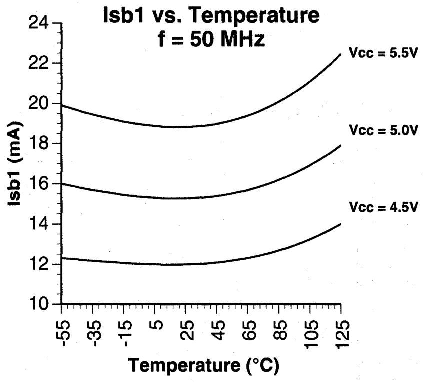


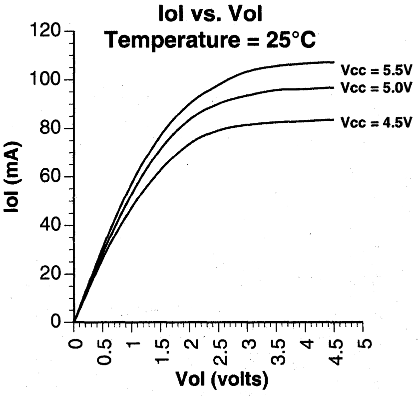


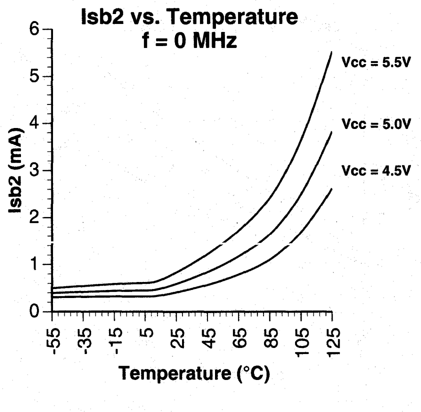
APPLICATION/TECHNICAL NOTE

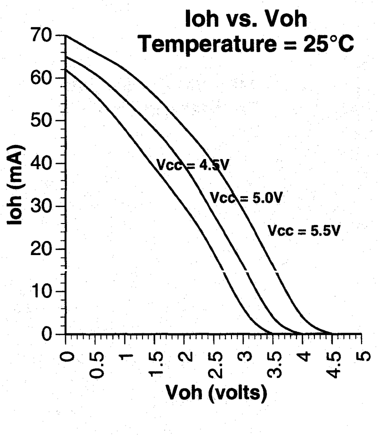

Icc vs. Temperature
f = 50 MHz
Icc (mA)
105
100
95
90
85
80
75
70
65
60
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
-55
-35
-15
5
25
45
65
85
105
125
Temperature (°C)


IccDR vs. Temperature
IccDR (µA)
800
700
600
500
400
300
200
100
0
Vcc = 3.0V
Vcc = 2.5V
Vcc = 2.0V
-55
-35
-15
5
25
45
65
85
105
125
Temperature (°C)


Isb1 vs. Temperature
f = 50 MHz
Isb1 (mA)
24
22
20
18
16
14
12
10
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
-55
-35
-15
5
25
45
65
85
105
125
Temperature (°C)


Iol vs. Vol
Temperature = 25°C
Iol (mA)
120
100
80
60
40
20
0
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Vol (volts)


Isb2 vs. Temperature
f = 0 MHz
Isb2 (mA)
6
5
4
3
2
1
0
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
-55
-35
-15
5
25
45
65
85
105
125
Temperature (°C)

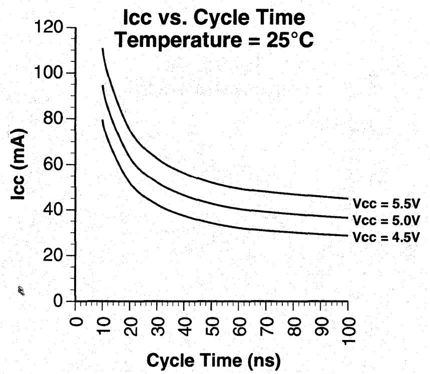

Ioh vs. Voh
Temperature = 25°C
Ioh (mA)
70
60
50
40
30
20
10
0
Vcc = 4.5V
Vcc = 5.0V
Vcc = 5.5V
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Voh (volts)

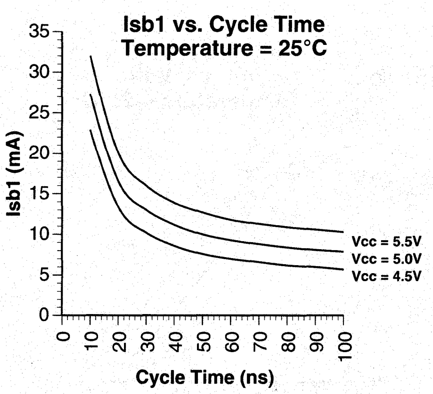
TECHNICAL NOTE

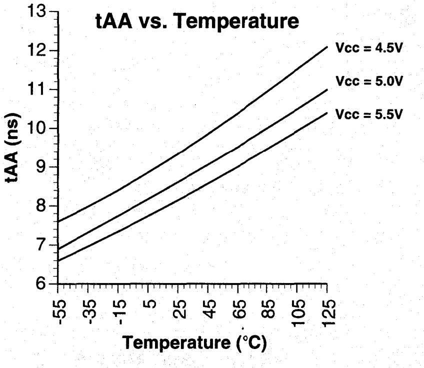
64K FAST SRAM TYPICAL OPERATING CURVES

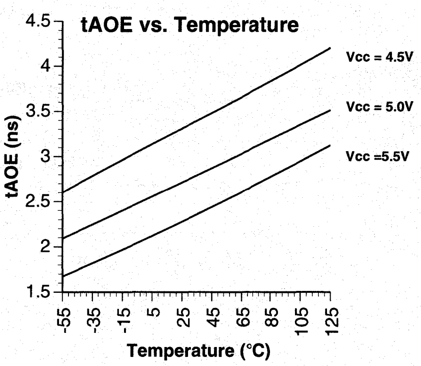
INTRODUCTION

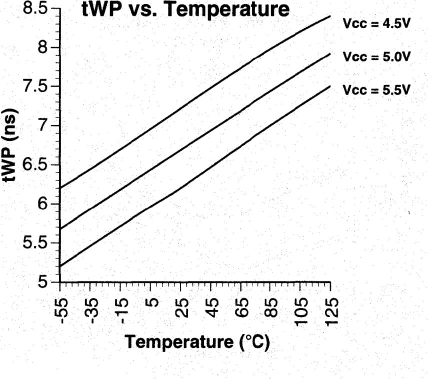
These curves represent the typical operating characteristics of Micron's 64K, 12ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.

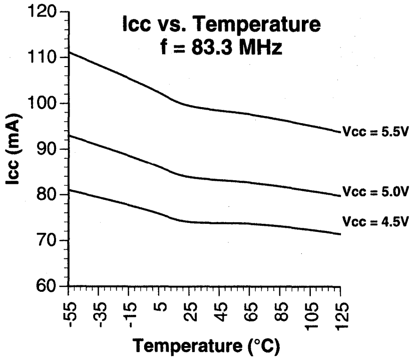


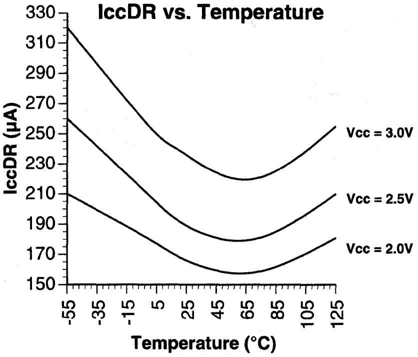


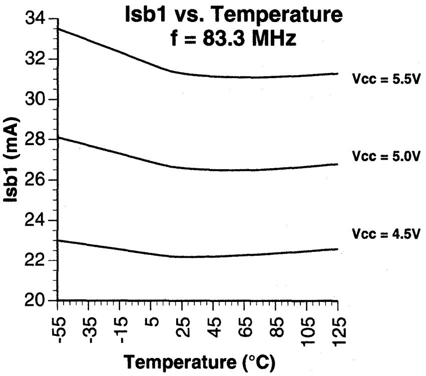


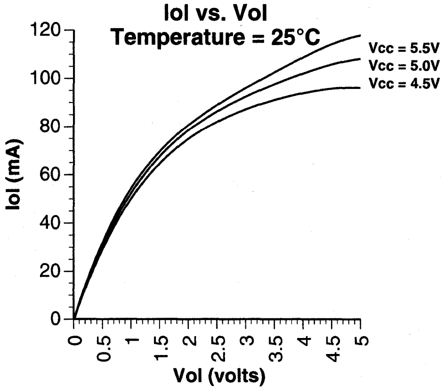


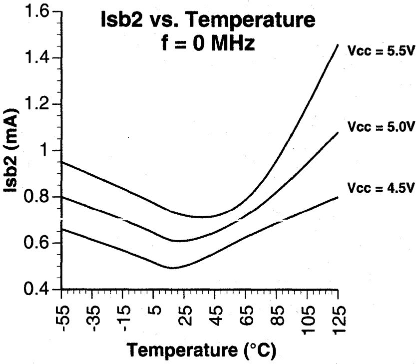


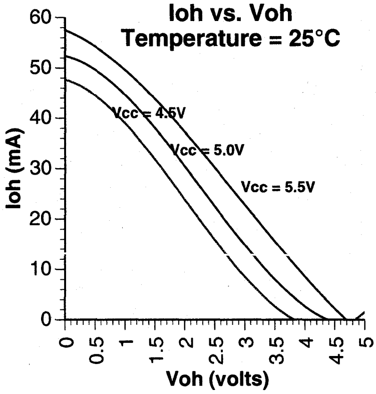

Icc vs. Temperature
f = 83.3 MHz


IccDR vs. Temperature


Isb1 vs. Temperature
f = 83.3 MHz


Iol vs. Vol
Temperature = 25°C


Isb2 vs. Temperature
f = 0 MHz


Ioh vs. Voh
Temperature = 25°C

TECHNICAL NOTE

128K x 8 SRAM CHIP ENABLE OPTIONS

INTRODUCTION

There are two standard pin configurations for the 128K x 8 SRAM. One version has a single chip enable ($\overline{\text{CE}}$), Figure 1. The other has two chip enables, $\overline{\text{CE1}}$ and CE2, Figure 2. These two configurations result from the original JEDEC Standard No. 21-C, page 3.7.5-11, that allows pin 30 (CE2) to be either a chip enable or a no connect (NC).

This technical note describes a method for designing a system to accept either part for a single chip enable system. It also shows the advantages of using the dual chip enable version to eliminate decoder logic in larger memory system designs.

Micron produces both versions of the 128K x 8 SRAM. The MT5C1008 has two chip enables and the MT5C1009 has one chip enable. The single chip enable version is usually used to replace modules in existing designs.

PC BOARD DESIGN CONSIDERATIONS

When a printed circuit board is designed for a one chip enable application, it is possible to wire the board so it can use both the single chip enable and the dual chip enable 128K x 8 SRAMs. To allow the PC board to accept either SRAM, pin 30 must be connected to Vcc. For a dual chip enable SRAM, CE2 is always asserted since it is wired directly to Vcc. This allows the device to be controlled by $\overline{\text{CE1}}$.

The single chip enable device has a NC on pin 30. Vcc wired to this pin does not affect the operation of the SRAM in any way.

TWO CHIP ENABLE DESIGNS

The MT5C1008 with dual chip enables can be used to increase memory depth without adding additional logic gates. An example of this design technique is shown in Figure 3. Two MT5C1008 devices are connected together to form a 256K x 8 memory without using any "glue logic."

If a single chip enable device is used in this design, an inverter would be needed on the A17 address line between the two devices. The addition of this inverter adds a gate delay directly in the access time path of the memory system. This also adds 4 to 8ns to the access time of the SRAMs.

On the dual chip enable device, one enable is asserted when the input is LOW ($\overline{\text{CE1}}$) and the other chip enable (CE2) is asserted when the input is HIGH. This allows the system designer to wire directly from an address to the SRAMs without adding an inverter.

PIN ASSIGNMENT (Top View)

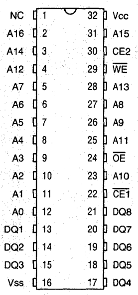


Figure 1
MT5C1008

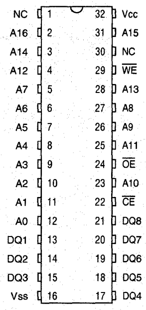


Figure 2
MT5C1009

As shown in Figure 3, $\overline{\text{CE1}}$ is connected to ground on the first SRAM and CE2 is connected to Vcc on the second SRAM. The input/output pins from both SRAMs are wired together to form a high-speed 256K x 8 SRAM system.

SUMMARY

Micron produces two versions of the 128K x 8 SRAM. The MT5C1008 has two chip enables and the MT5C1009 has one chip enable. In new designs, the MT5C1008 optimizes system performance at a lower cost. The MT5C1009 reduces power and cost and improves reliability of systems designed with 128K x 8 SRAM modules.

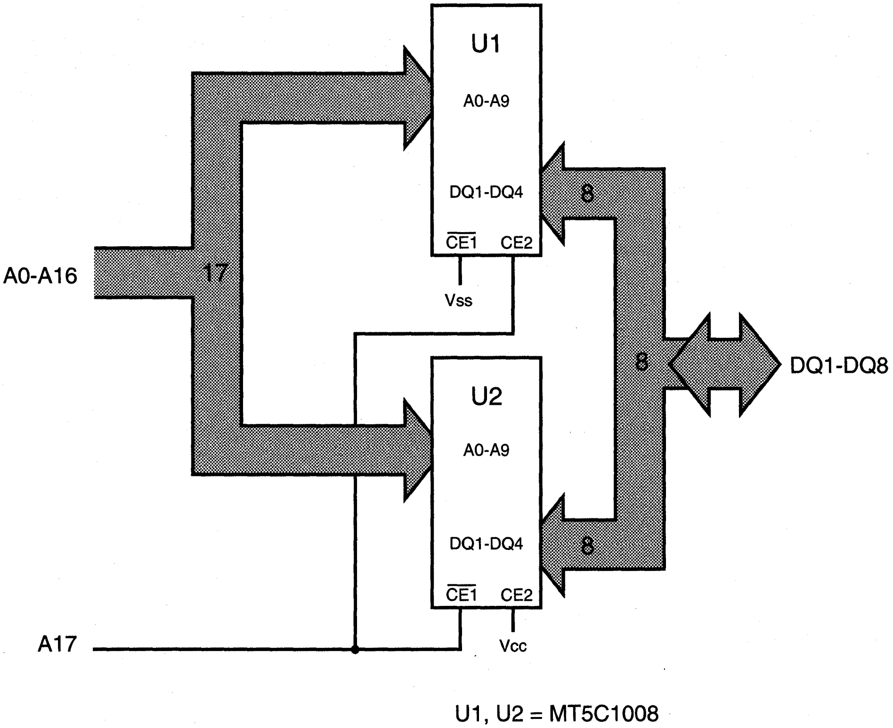


Figure 3
256K x 8 SRAM SYSTEM

MICRON TECHNOLOGY, INC. **AN-56-01**

APPLICATION NOTE

MT56C0816 CACHE DATA SRAM FAMILY

INTRODUCTION

The Micron MT56C0816 Cache Data SRAM family was developed in response to a need for compact cache subsystems for the Intel™ 80386 microprocessor. Applications using the 80386 demand maximum performance, and DRAM technology cannot meet the fast access times required for zero-wait-state operation. Statistics show that a small cache subsystem allows the majority of 80386 memory accesses to be completed within the 80386 cycle time. This eliminates the need for wait states[1] to be added to the memory cycle, allowing the 80386 to operate at its maximum performance level. The cache can be designed using fast commodity SRAMs.

However, the Micron Cache Data SRAM allows cache subsystem designs requiring less space, using less power and offering greater reliability than the fast SRAM implementation. Design and debug times are also reduced, because the Micron MT56C0816 is designed to connect directly to off-the-shelf 80386 cache controllers.

This application note explores why caching is needed. It then discusses how a cache subsystem works, what influences the performance of the cache, and how different cache organizations and architectures compare.

In addition, this application note looks at the most popular off-the-shelf controllers available to implement a cache subsystem. It compares several fast SRAM and cache data SRAM implementations with those controllers. Finally, a summary of the cache data SRAM advantages is shown.

BACKGROUND

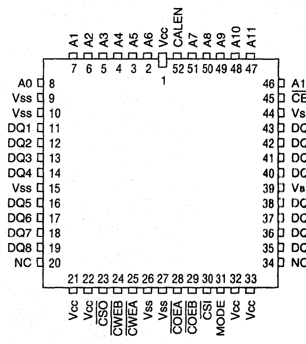
Microprocessors have typically interfaced directly to DRAM (dynamic random-access memory) main memory due to their relatively slow clock speeds and multiple clock instruction cycles. But over the past few years, complex-instruction-set computer (CISC) microprocessors have driven the clock frequencies into the 20, 25 and 33 megahertz (MHz) range. The two most dominant CISC architectures are the 80X86 and 680X0. The number of clock cycles needed to execute a specific instruction has steadily decreased and is now approaching a single clock cycle for many instructions.

The introduction of reduced-instruction-set computer (RISC) architectures has fueled the quest for higher clock frequencies and reduced clock cycles for each instruction executed. Some of the predominant RISC architectures include SPARC™, 80960, R3000, 29000 and 88000. RISC architectures requiring the absolute minimum number of clock cycles for each instruction are not only approaching single clock execution, but in some cases are able to sustain multiple instruction execution in a single clock cycle. CISC microprocessors are not far behind, and the competition between the CISC and RISC camps is driving processor designers to continuously reach for maximum performance.

This new era of performance is placing heavy demands on memory subsystems that heretofore have been able to

MT56C0816
PIN ASSIGNMENT (Top View)

52-Pin PLCC
52-Pin PQFP



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[1] Wait states are one or more additional processor clock cycles added to the memory access cycle. These extra clock cycles keep the processor idling while memory has time to respond to the memory request. For a given processor's clock speed, the number of wait states needed to complete a memory access is directly related to how fast the memory can respond to a read or write request initiated by the microprocessor.

For example, the 80386 can complete a memory cycle in two clock periods. With a 25 MHz processor, this allows 80ns for the processor to output its address to the memory array. It also provides time for the decode circuitry to supply the necessary signals to the memory and enables the memory to respond once it has received the necessary signals. In typical applications, the speed of the memory array that is needed to avoid any wait states is 35ns.

keep pace. For example, an 80386 processor operating at 25 MHz requires a memory access time of close to 40ns if it is to operate at maximum performance (meaning no wait states):

2 x clock cycle time - address delay - data setup - decode logic and buffer delay = (2 * 40) - 21 - 7 - 10 = 42ns

Current DRAM access speeds are in the 70ns to 80ns access range. Even with faster access techniques such as FAST PAGE and STATIC COLUMN modes, the DRAM access time is not sufficient to meet zero-wait-state access times.

The alternative to adding wait states to the system and thus degrading performance is to design a system architecture that makes the memory appear faster to the CPU. Approaches that have been implemented include organizing the DRAM in multiple banks, adding some fast SRAM for specific code and data or caching.

The use of a cache is applicable in high-end systems as well as cost-conscious, medium-performance systems. At the high end, where the goal is to maximize performance on every processor cycle, the only alternative to cache is the use of very fast SRAMs as the main memory to achieve zero-wait-state performance. This is a very expensive solution. The medium performance systems must constantly balance performance and cost. A small cache in these systems can achieve much higher performance with a relatively small, incremental cost.

CACHE OVERVIEW

WHAT IS A CACHE

A cache is small, fast, local storage for frequently accessed code and data. It consists of high-speed memory (usually SRAM) that resides between the CPU and the main memory (usually DRAM) in a processor system. Figure 1 illustrates a typical block diagram of an 80386-based cache system.

The cache increases the effective speed of the main memory by responding quickly with a copy of the most frequently used items in main memory. The cache control logic checks the address of each memory access and, if it is present in the cache, allows the cache to respond instead of main memory. Accesses to the cache are much faster (typically zero wait states) than accesses to main memory. The more accesses that are made to the cache, the better the overall system performance. Hence the goal in designing a cache is to maximize accesses to the cache (known as the cache hit rate).

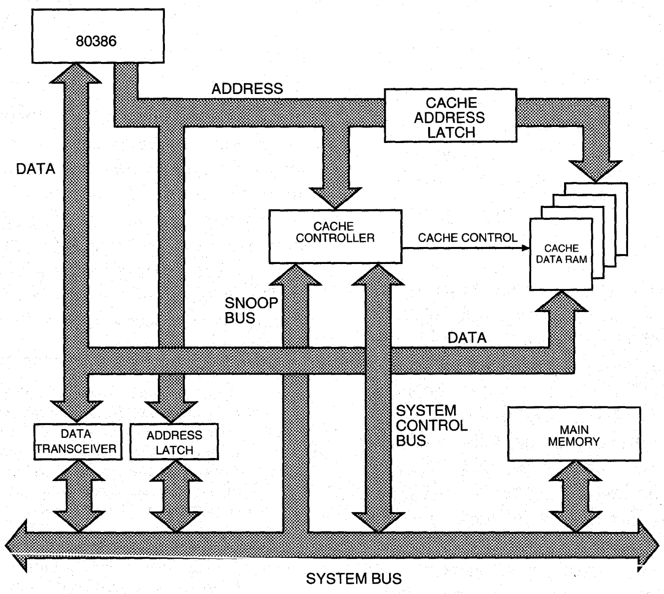


Figure 1
TYPICAL 80386-BASED CACHE SYSTEM

WHY A CACHE WORKS

The theory of a cache is based on two attributes of computer programs: temporal locality and spacial locality. Temporal locality (locality of time) is an attribute exhibited by computer programs where the same addressed code and data are used repeatedly in a short time. This behavior is typified by program loops, a very prevalent programming structure. Spacial locality (locality of place) is a computer program attribute in which the next needed information is found near the information that was just accessed. This occurs in most programs since related data are stored together (data tables, arrays, etc.) and instructions (code) are typically executed in sequence.

In a cache design, main memory may be thought of as a collection of many small, uniform segments. The cache contains a copy of one or more of these small memory segments that have been used recently. When the processor executes a read from main memory, the cache control determines if that address is contained in one of the small memory segments that are currently resident in the cache memory. If so, the access is completed by the cache. If not, the access is completed by main memory and the memory segment that has just been accessed is placed into the cache for future use. The attribute of spacial locality implies that the information needed next will also be found in the same memory segment just accessed, which is now located in the cache. The attribute of temporal locality implies that the memory location, just accessed, will be used again in the near future.

Table 1

CACHE HIT RATES			
CACHE CONFIGURATION			
HIT RATE (%)*	SIZE (KB)	ASSOCIATIVITY	LINE SIZE (BYTES)
41	1	Direct	4
73	8	Direct	4
81	16	Direct	4
86	32	Direct	4
87	32	Two-way	4
88	64	Direct	4
89	64	Two-way	4
89	64	Four-way	4
89	128	Direct	4
89	128	Two-way	4
91	32	Direct	8
92	64	Direct	8
93	64	Two-way	8
93	128	Direct	8

* Rounded to the nearest whole percent.

PERFORMANCE FACTORS

The performance of the cache (and hence the system) is measured by the cache hit rate, which is the percentage of successful cache accesses. The cache hit rate is determined by specific demands of software being executed and by cache-management policies.

The design factors that influence cache hit rate are: total cache memory size, cache memory organization (associativity), and cache transfer block size. These factors are all interrelated and each needs attention to obtain the optimum cost-effective result. Each factor presents trade-offs of performance, complexity and cost. One factor may be decreased for cost reasons while another may be increased to improve performance. The same or better hit rate may still be obtained. However, the complexity might be increased also. The cache designer must carefully weigh each factor to achieve the best overall cost/performance/complexity ratio. Table 1 compares the cache hit rate of several cache sizes with varying associativity and line sizes.

COHERENCY

Since the cache is a temporary buffer for a section of main memory, the cache designer must take into consideration how to keep the data consistent between main memory and the cache. This is called cache coherency.

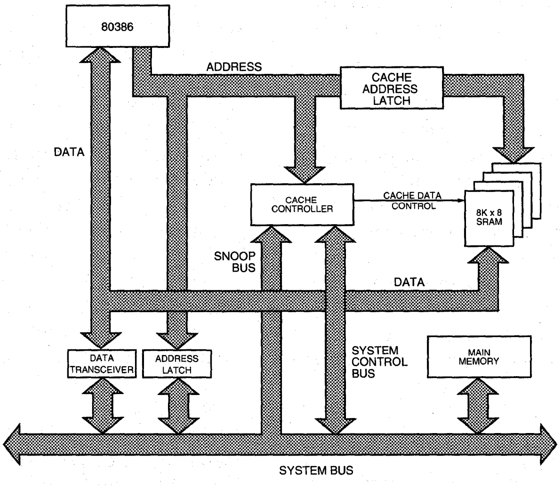
There are instances when an address in the cache might not contain the same information as the same address in main memory. One such situation occurs during a write cycle, where a cache data element is updated to a new value. Now the address in main memory and the same address in the cache have two different values, with the cache containing the newest value. The main memory needs to be updated to contain the same information. This is controlled by the write policy of the cache.

Another such instance occurs when another processor writes information to a main memory address that is also located in the cache. This situation is handled by "snooping". Snooping occurs when the main memory bus is always watched by the cache logic. If a write occurs to a main memory address identical to a cached address, that cache address is marked invalid. This guarantees that if that address is accessed, it will be updated as main memory is accessed for the requested data.

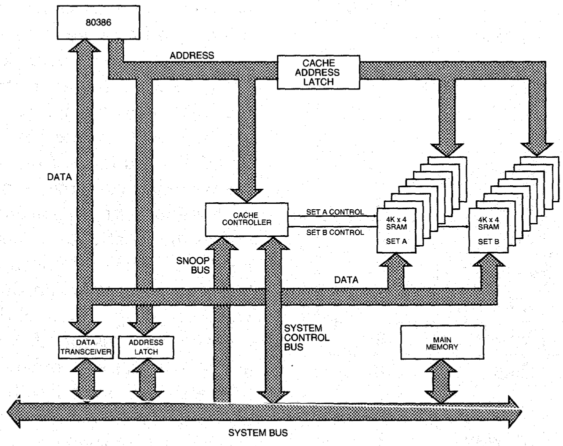
There are two types of cache write policies: write-through and copy-back. A write-through cache will write to both main memory and the cache on each write cycle whenever the addressed location is found to be resident in the cache.

This ensures that the cache and main memory are always coherent, but it requires more main memory accesses, thus increasing bus usage. This also decreases performance due to the large amount of accesses to slower main memory. The main memory accesses may be made more efficient with the addition of write buffers, but this also adds significant complexity and coherency problems in the buffers.

The copy-back policy writes only to the cache, if the address location is present (cache hit), and allows the CPU to proceed. This allows maximum system performance. However, the main memory still needs to be updated. The update of main memory occurs when the line that contains the write address in the cache is replaced by a new line. Main memory write updates occur far less often than the update policy of a write-through design. The copy-back policy also has its drawbacks. Instead of only replacing the data element (possibly one byte) that was written, all the bytes in the line are replaced. This may be as many as four, eight, 16 or more. This can result in a large time penalty when a copy-back occurs.



DIRECT-MAPPED BLOCK DIAGRAM



TWO-WAY-SET BLOCK DIAGRAM

Figure 2

CACHE CONTROLLERS

It quickly becomes apparent that all variables in cache design are interrelated and all have trade-offs. For most designs, especially those in the micro arena, caching represents a new realm. Unfortunately, designing a cache from scratch can add an enormous amount of time to the design. Fortunately, several companies have designed off-the-shelf cache controllers, which take into consideration all the trade-offs and performance factors. These controllers meet the majority of the needs of the 80386 cache market.

The three most popular 80386 cache controllers — Intel's 82385, Austek's A38202 and Chips & Technologies' 82C307 and Peak™ — were designed to interface with standard SRAMs as well as additional address latches and possible transceivers.

DIRECT-MAPPED VERSUS TWO-WAY-SET IMPLEMENTATION

The use of an off-the-shelf cache controller eliminates most of the decisions that would occur in a discrete design. The trade-offs that have been made include line size, write update policy, and in some cases, even the cache size and associativity. The majority of controllers allow the user to configure only the associativity (direct or two-way set) and the cache size. The controllers support, without additional logic, both the TWO-WAY-SET ASSOCIATIVE and DIRECT-MAPPED modes.

The trade-off between DIRECT-MAPPED and TWO-WAY-SET ASSOCIATIVE modes is typically one of increased hit rate versus added complexity. Since the controllers have integrated the complexity, it might seem that the only logical choice is to use the TWO-WAY-SET ASSOCIATIVE mode. Assuming a 32 kilobyte (KB) cache, the direct mode will require four 8K x 8 SRAMs (one bank of 8K x 32 bits) while two-way mode will require 16 4K x 4 SRAMs (two banks of 4K x 32 bits). Figure 2 contains typical block diagrams illustrating implementations of direct-mapped and two-way-set designs.

The trade-off, then, is in the additional SRAMs for two-way set. This is reflected as incremental cost, power and board space needed to achieve the higher hit rate obtained over the direct-mapped implementation. For the 32KB cache size, the additional hit rate of the two-way-set implementation makes it the best choice if the board space is available. In the medium-to-high-end performance market, the extra performance (see Table 1) delivered by the two-way-set design is worth the extra cost.

Table 2 compares the board real estate and power requirements of each configuration. The two-way-set implementation requires eight 74F245 transceivers to control the flow of data between each bank and the common data bus. Figure 3 illustrates the board space requirements of each implementation.

The assumptions used for the board space comparison were .050 inch chip-to-chip spacing and .050 inch outside border around the circuitry. The power comparison is based on a 25 MHz design assuming 10ns decoding delay. This gives the following equation for the cache 8K x 8 SRAM access time:

Cache SRAM available access time = 4 * 386CLK2 - 386 address delay - 386 ready setup - SRAM enable decode - 74F373 delay = (4 * 20ns) - 21ns - 9ns - 10ns - 9ns = 31ns.

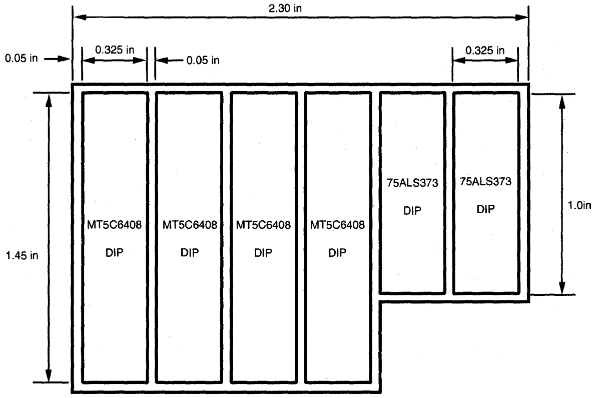
The 8K x 8 configuration would require SRAMs with an access time of 25ns. For the two-way-set configuration, an additional 6ns must be subtracted for the delay through the 74F245 transceivers. This barely provides 25ns for the 4K x 4 SRAM access time in this latter implementation. Any other delays that exist in the data access path must also be taken into consideration. In the case of the 4K x 4 SRAMs, a 20ns part will probably be required.

Table 2

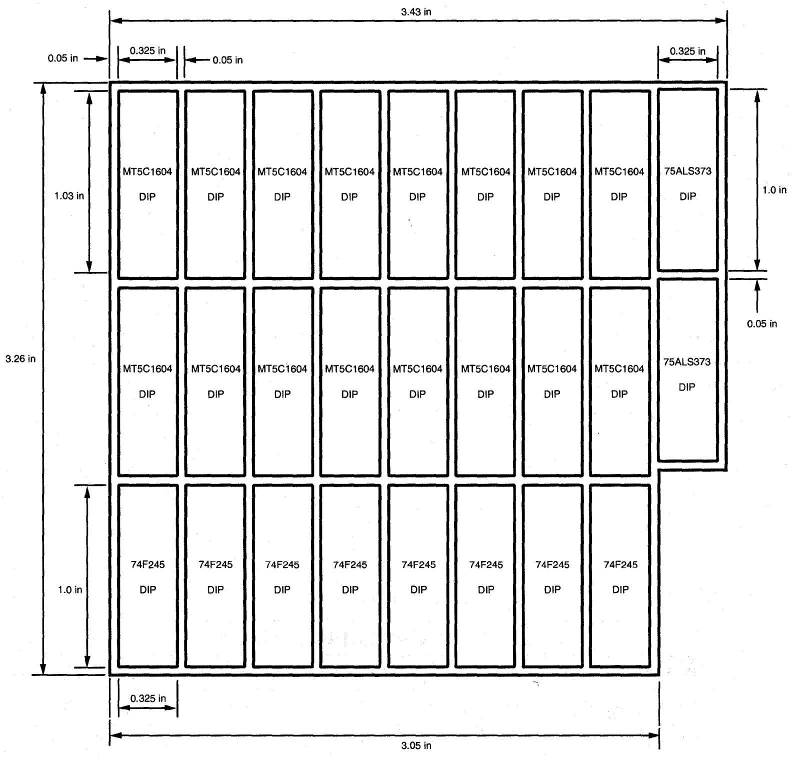
32KB CACHE CONFIGURATION COMPARISON

CONFIGURATION	SRAM	# SRAMs	AREA (in^2)	POWER (W)
Direct-Mapped	8K x 8	4	3.23	2.75
Two-Way-Set	4K x 4	16	10.57	10.55*

* The 4K x 4 configuration incorporates two banks of eight SRAMs each. One bank is active, while the other is in standby mode. This fact was used in the power calculations.



DIRECT-MAPPED SPACE REQUIREMENT USING 8K x 8 SRAMS



TWO-WAY-SET SPACE REQUIREMENT USING 4K x 4 SRAMS

Figure 3

MT56C0816 INTEGRATED CACHE SRAM

The MT56C0816 is an application-specific 8K x 16 SRAM designed for, but not limited to, cache data SRAM implementations. The MT56C0816 is designed to be used in either direct-mapped or two-way-set designs. It incorporates an on-chip address latch, on-chip multiplexing between the two SRAM banks (for two-way-set mode), fast output enable times and low-power consumption.

Almost all designs have used the MT56C0816 in the TWO-WAY-SET mode of operation. This is due to the fact that the MT56C0816 eliminates the major problems in implementing the TWO-WAY-SET mode architecture, namely the cost, space and power. Before the MT56C0816, a two-way-set implementation required three times the board space and four times the power of a direct-mode design when using standard SRAMs.

Due to the integration of on-chip address latches and multiplexors, often a lower-speed MT56C0816 can be used in place of a higher-speed, more costly standard SRAM. The advantages of the MT56C0816 don't stop here. It is widely second-sourced by other suppliers, the access time has been reduced to 20ns and it is available in the smaller PQFP package.

Table 3 compares the board space, power and access time requirements of standard SRAMs and both packages of the MT56C0816 in a 32KB cache design. The numbers presented are applicable to both direct-mapped and two-way-set implementations for the MT56C0816 and 4K x 4 SRAMs. The use of 8K x 8 SRAMs in a two-way configuration requires a minimum of 64KB in the cache and are not considered in the comparison. The same board area assumptions are used in Table 3 as in Table 2 regarding chip-to-chip and circuitry border spacing. The area values are normalized to the MT56C0816 in the PQFP package.

The SRAM access time and power considerations are based on a 33 MHz 80386 design assuming a 10ns enable decode time. The cache SRAM access time equation is as follows:

Cache SRAM access time = 4 * 386CLK2 - 386 address delay - 386 ready setup - SRAM enable decode - 74F373 delay = (4 * 15ns) - 15ns - 7ns - 10ns - 9ns = 19ns

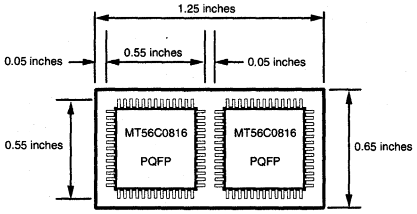
This will require 8K x 8 SRAMs with a 15ns access time. The 4K x 4 implementation requires that the transceiver delay time (6ns) also be subtracted, which leaves only 13ns. Hence, a 12ns part must be used.

Table 3

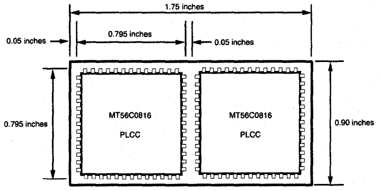
CACHE SRAM COMPARISON (33 MHz)

DEVICE	NUMBER OF DEVICES	PC BOARD AREA	POWER (W)	ACCESS SPEED (ns) REQUIRED
MT56C0816 PQFP	2	1.00	2.2	25
MT56C0816 PLCC	2	1.94	2.2	25
8K x 8 SOJ 74F373 SOIC	4 2	2.28	3.15	15
8K x 8 DIP 74F373 DIP	4 2	3.99	3.15	15
4K x 4 SOJ 74F373 SOIC 74F245 SOIC	16 2 8	8.58	12.15*	12
4K x 4 DIP 74F373 DIP 74F245 DIP	16 2 8	13.05	12.15*	12

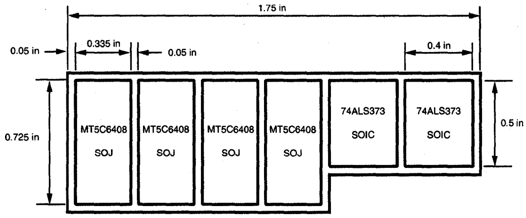
* The 4K x 4 configuration incorporates two banks of eight SRAMs each. One bank is active while the other is in standby mode. This fact was used in the power calculations.



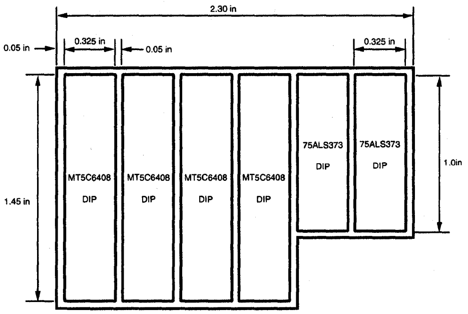
MT56C0816 PQFP



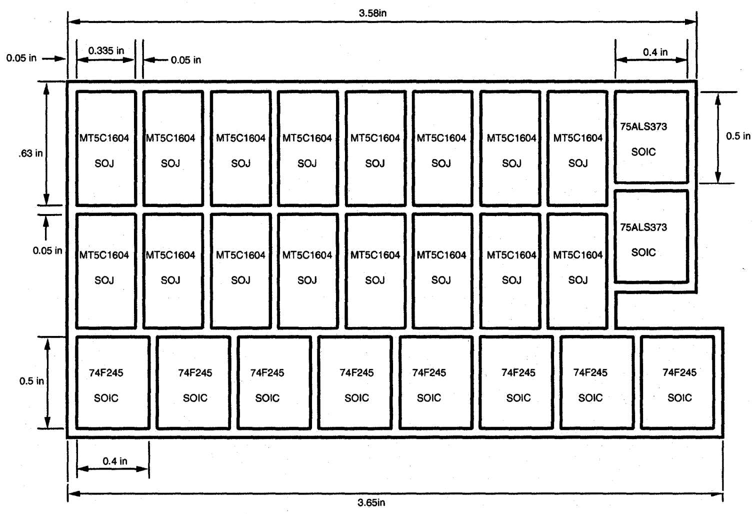
MT56C0816 PLCC



8K x 8 SOJ/SOIC

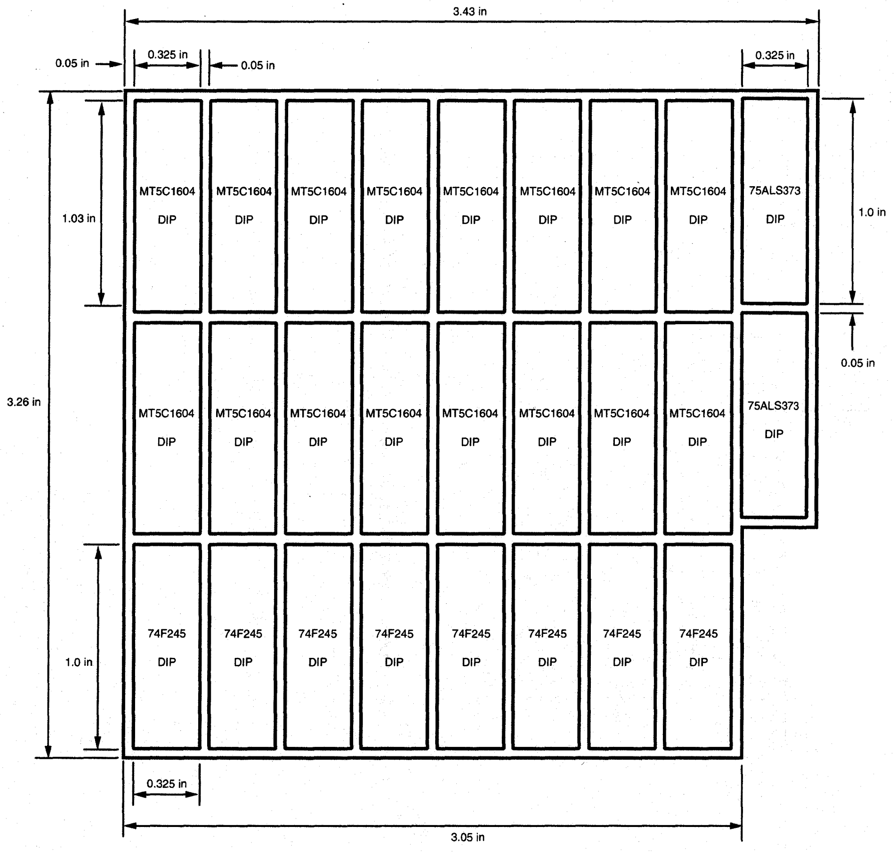


8K x 8 DIP



4K x 4 SOJ/SOIC

Figure 4



4K x 4 DIP

Figure 5

The MT56C0816 incorporates the address latch on-board and allows 9ns to be added back into the SRAM access time. This yields a 28ns access time for a MT56C0816 design, which is easily met by the 25ns part. This access time is applicable to both the direct mode and two-way set configurations since the data multiplexing is also on-chip.

Figures 4 and 5 illustrate the board space required by the MT56C0816 and the standard SRAM configurations that are summarized in Table 3.

OPTIMUM SYSTEM

The available, off-the-shelf cache controllers allow very quick and efficient cache subsystem designs for 80386-based systems. And an off-the-shelf controller teamed with the MT56C0816 maximizes the system performance/cost ratio. The MT56C0816 allows the controller to be employed in its highest performance mode, two-way-set associativity, without the disadvantages incurred using standard SRAMs.

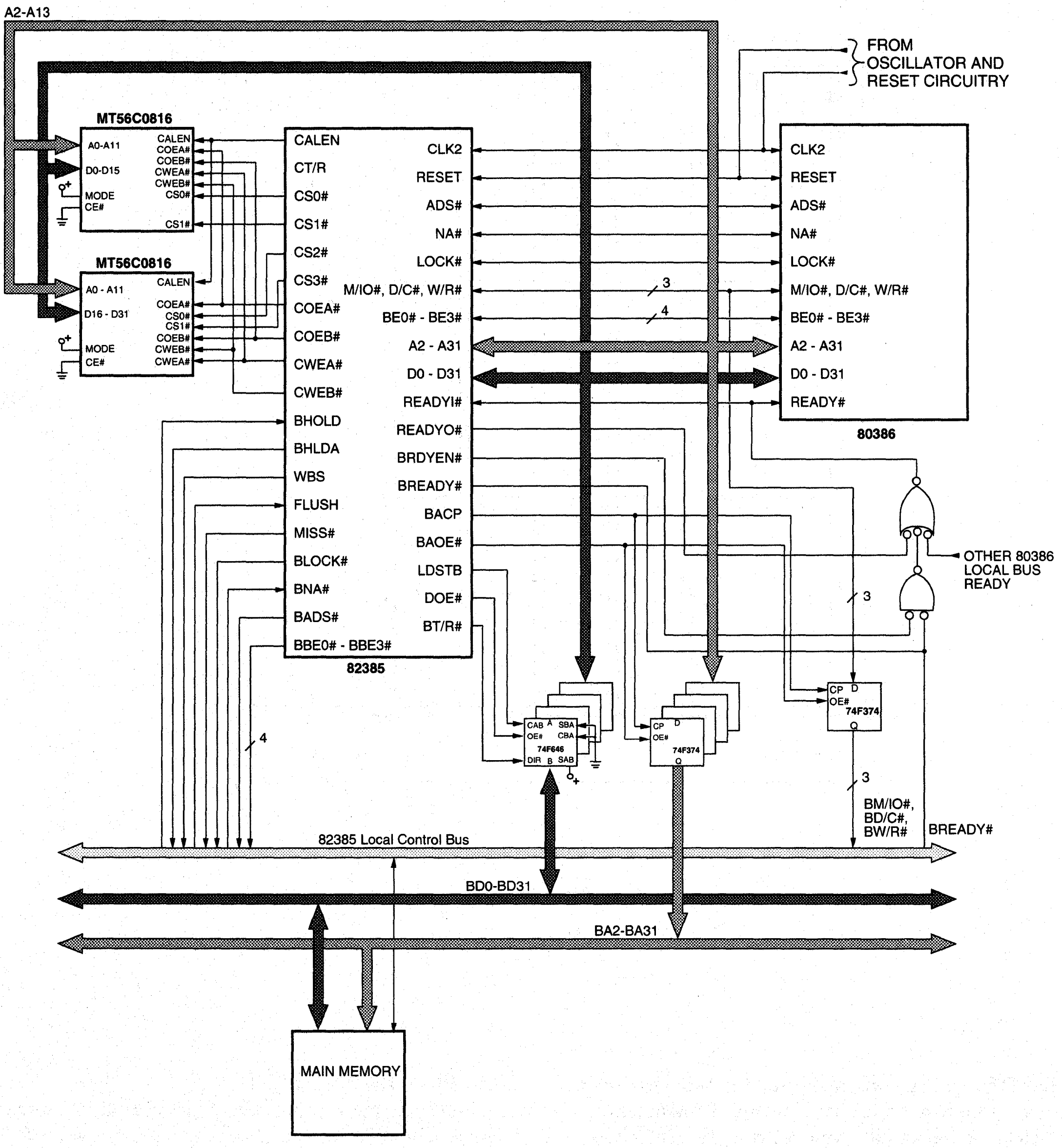

A2-A13
FROM
OSCILLATOR AND
RESET CIRCUITRY
MT56C0816
A0-A11
D0-D15
MODE
CE#
CALEN
COEA#
COEB#
CWEA#
CWEB#
CS0#
CS1#
MT56C0816
A0 - A11
D16 - D31
MODE
CE#
CALEN
COEA#
CS0#
CS1#
COEB#
CWEB#
CWEA#
CALEN
CT/R
CS0#
CS1#
CS2#
CS3#
COEA#
COEB#
CWEA#
CWEB#
BHOLD
BHLDA
WBS
FLUSH
MISS#
BLOCK#
BNA#
BADS#
BBE0# - BBE3#
CLK2
RESET
ADS#
NA#
LOCK#
M/IO#, D/C#, W/R#
BE0# - BE3#
A2 - A31
D0 - D31
READYI#
READYO#
BRDYEN#
BREADY#
BACP
BAOE#
LDSTB
DOE#
BT/R#
82385
3
4
CLK2
RESET
ADS#
NA#
LOCK#
M/IO#, D/C#, W/R#
BE0# - BE3#
A2 - A31
D0 - D31
READY#
80386
OTHER 80386
LOCAL BUS
READY
3
CAB
A
SBA
OE#
CBA
74F646
DIR
B
SAB
CP
D
OE#
74F374
Q
CP
D
OE#
74F374
Q
4
3
BM/IO#,
BD/C#,
BW/R#
BREADY#
82385 Local Control Bus
BD0-BD31
BA2-BA31
MAIN MEMORY

Figure 6

Table 4

MICRON CACHE SRAM FAMILY				
PART NUMBER	**DESCRIPTION**	**SPEED (ns)**	**PACKAGE**	**AVAILABILITY**
MT56C0816	Dual 4K x 16 or 8K x 16 Addresses 0 through 11 are latched	20, 25, 35	PLCC PQFP	Now
MT56C0818	Dual 4K x 18 or 8K x 18 Addresses 0 through 11 are latched	20, 25, 35	PLCC PQFP	Now
MT56C2818	Dual 4K x 18 or 8K x 18 80486 self-timed write; used on Intel Turbocache 486™ module	24, 28	PLCC PQFP	Now
MT56C3816	Dual 4K x 16 or 8K x 16 Addresses 0 through 12 are latched	20, 25, 35	PLCC PQFP	Now
MT56C3818	Dual 4K x 18 or 8K x 18 Addresses 0 through 12 are latched	20, 25, 35	PLCC PQFP	Now

A two-way-set design using the MT56C0816 requires only two parts versus 10 for an 8K x 8 SRAM implementation and 26 for a 4K x 4 implementation. A direct-mapped design using the MT56C0816 requires only two parts versus six for an 8K x 8 SRAM implementation and 26 for a 4K x 4 implementation. In addition to the board-space, power and integration advantages, the MT56C0816 offers a direct connection to the controllers. This means higher system reliability and easier design and debugging over the standard SRAM implementations. Figure 6 shows a detailed diagram of a system using the MT56C0816.

MORE SOLUTIONS

An entire family of cache-specific data SRAMs is available. Table 4 lists the members of the cache SRAM family.

In addition, Micron was the first to introduce the MT56C0816 both in a 20ns access speed and in the thin, small-outline PQFP package.

SPECIAL CONSIDERATIONS

The Micron MT56C0816 was designed for a specific generation of cache implementations for the 80386. That generation required a nonlatched A12 address and a faster A12 access time. Since then, designs employing certain off-the-shelf controllers are more efficiently implemented if address line A12 is latched on the cache data SRAM. These designs do not require the faster A12 access time. In order to keep pace with the everchanging design community, Micron introduced time-frame versions of the MT56C0816 and the MT56C0818 with address A12 latched. The part numbers of these new devices are MT56C3816 and MT56C3818 respectively.

The latched A12 version of the cache data SRAM can be appealing in 80386DX designs where the cache uses a two-way-set associative architecture and the cache size is 64KB or larger. The latched A12 parts are applicable for 80386SX designs where the cache is structured using a two-way-set associative organization and the cache size is 32KB or larger.

Designs using a direct-mapped architecture essentially use the cache data SRAM as an 8K x 16 SRAM and as such the latched version would be advantageous in all cases. Whether the latched or unlatched A12 version of the cache data SRAM is more advantageous depends entirely on the specifics of each individual design.

SUMMARY

The Micron MT56C0816 has been as important to 80386 caching solutions as the off-the-shelf controllers from Intel, Austek and Chips & Technologies. The direct connection of the MT56C0816 to controllers makes its implementation more appealing for the designer from both a design and debug standpoint. The reduced board space, power and comparable cost to commodity SRAM implementations are advantages that make the MT56C0816 the right choice for new designs.

Micron's MT56C0816 adds reliability to systems due to the reduced component count. It also offers other, less obvious cost advantages. For instance, reduced board space requirements directly affect board manufacturing costs and allow more components to be placed on the board. Better reliability means lower costs due to fewer returns and fewer board revisions. The MT56C0816 also minimizes inventory and assembly costs. Clearly the Micron MT56C0816 is a superior solution to standard SRAMs in cache designs.

OVERVIEW

At Micron, we emphasize superior product quality through our unmatched reliability system. We define product reliability as a product's ability to perform its intended functions and operate under specified environmental conditions for a specified length of time. This section contains a brief overview of some of the issues that affect the reliability of IC devices and briefly describes Micron's reliability program.

For a more in-depth discussion of reliability, please refer to Micron's Quality/Reliability Literature.

RELIABILITY GOALS

When we discuss reliability goals of semiconductor ICs, we typically refer to the traditional reliability curve of component life. The reliability curve, or "bathtub curve," appears below, where h(t) is the hazard rate or the probability of a component failing at t_0+1 in time if it has survived at time t_0.

Figure 1 shows that the significant portion of this curve is the random failure segment. The term "infant mortality" refers to those ICs that would fail early in their lives due to manufacturing defects. To screen out such failures, Micron evaluates all our products using intelligent burn-in. This unique AMBYX™ intelligent burn-in/test system, developed is described in the following section.

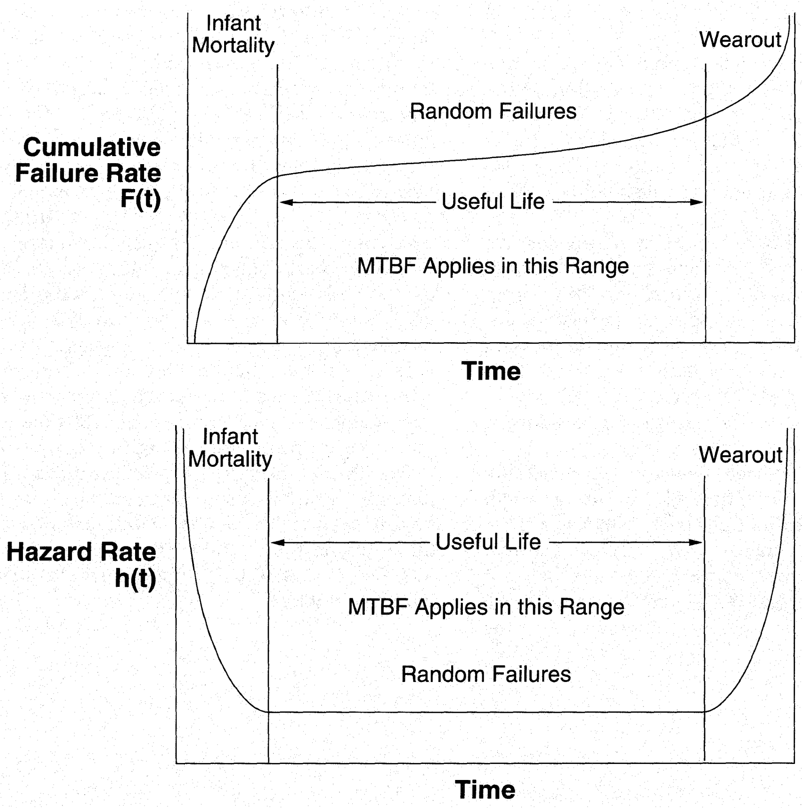


Figure 1
RELIABILITY CURVE

MICRON'S AMBYX™ INTELLIGENT BURN-IN AND TEST SYSTEM

Throughout the semiconductor industry, burn-in has been a crucial factor to increase memory products' reliability. Micron stresses our memory devices to simulate years of normal use. Then we document and analyze the results so that we can take any corrective action needed.

To effectively screen out infant mortalities, Micron believes it is critical to functionally test devices several times during the burn-in cycle without removing them from the burn-in oven. We were so convinced of the importance of highly refined burn-in that we searched for a system to meet this need. Because we found no system that met our requirements, we introduced the concept of "intelligent" burn-in and, in 1986, we developed the AMBYX™ intelligent burn-in and test system. Today, we use it to test every component and system-level product we make.

With the AMBYX, we can determine if the failure rate curves of *individual* product lots reach the random failure region of the bathtub curve by the end of the burn-in cycle. We subject product lots that do not exhibit a stable failure rate to additional burn-in. This burn-in flow also brings the slightest variation in a product's failure rate to our attention.

Since the AMBYX allows us to test devices for functionality without removing them from the burn-in oven, we effectively eliminate failures resulting from handling, thereby minimizing "noise" from the test results. During the test phase, output produced by the devices under test is compared to the pattern expected. If a discrepancy occurs, the AMBYX records the failure and provides the bit address, device address, board address, temperature, Vcc voltage, test pattern, and time set.

During the burn-in cycle itself, devices are functionally tested in four intervals. The first test begins at room temperature. Then, we ramp up the oven to 85°C for more functional testing. This enables us to detect thermal intermittent failures, another unique feature of intelligent burn-in. We conduct the next test at 125°C — any device that does not pass this sequence is eliminated. As the burn-in process continues, the devices are dynamically stressed at high temperature and voltage for a given number of hours. At the end of this period, we functionally test all devices again, followed by another burn-in cycle and further tests. This sequence is repeated four times on every device in every production lot.

These test results allow us to identify individual failures after each burn-in cycle. Figure 2 illustrates how the four burn-in and test cycles flow. The typical test results shown make up the first portion of the bathtub curve of component reliability.

There are two important reasons that Micron conducts the last two burn-in and test periods (or "quarters") at lower Vcc than the first two portions. First, we want the several million device hours that we accumulate weekly on production lots to be conducted at stress conditions identical to the conditions for the extended high-temperature-operating-life (HTOL) test. All semiconductor manufacturers use this test to calculate the random field failure rates. Second, we want to be sure we are not introducing new failure modes (failures unrelated to normal wearout) by testing them at extremely elevated conditions. In this way, Micron ensures that we've effectively screened our products for infant mortalities.

Control charts, such as the one shown in Figure 3, alert us to trends in the failure rates of some lots. When we detect an increase in a certain failure rate, we pinpoint the lots that need additional burn-in cycles to identify all variables that might influence the failure rates of those lots. Such variables could include fabrication and assembly equipment, manufacturing shifts and time frames when the lots were processed through specific steps.

The overall benefits of intelligent burn-in are wide ranging. It allows us to identify early-life failures and failure mechanisms as they would actually occur in customer applications. It also allows us to identify problem lots that, if undetected, could contribute substantially to infant mortalities.

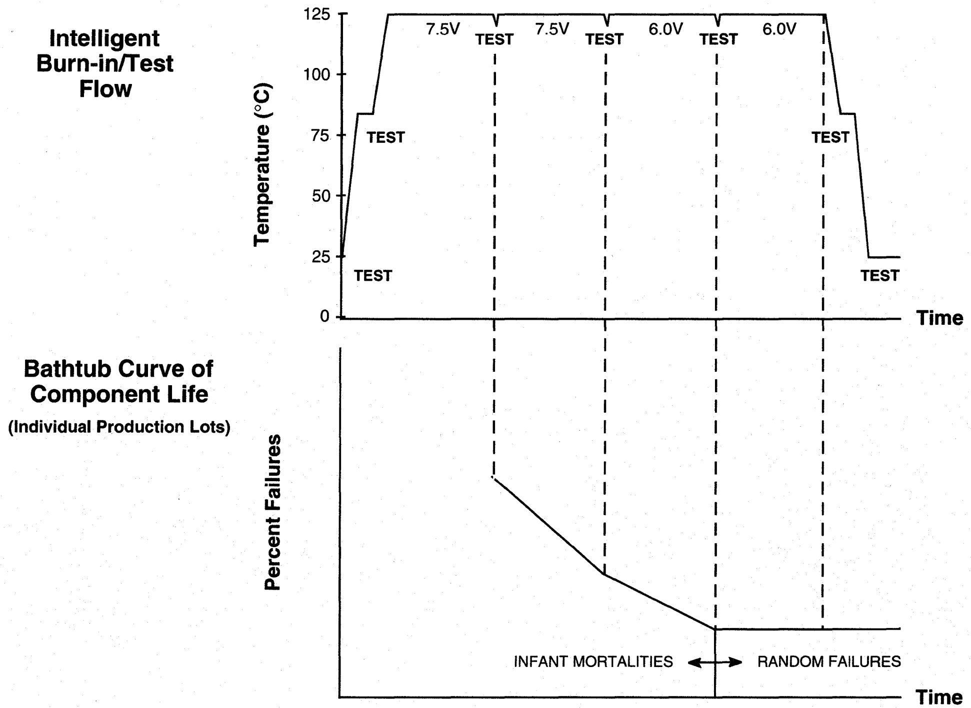


Figure 2
AMBYX™ BURN-IN/TEST FLOW AND TEST RESULTS

ENVIRONMENTAL PROCESS MONITOR PROGRAM

Micron's environmental process monitor (EPM) program is designed to ensure the reliability of our standard products. Under this program, we subject weekly samples of our various product and package types to a battery of environmental stress tests.

As discussed in the previous pages, we test our devices for many hours under conditions designed to simulate years of normal field use. We then apply equations derived from intricate engineering models to the data collected from the accelerated tests. From these calculations, we are able to predict failure rates under *normal use.* Figure 3 shows the conditions for these tests, known as "accelerated environmental stress" tests. The EPM program described in Figure 3 is for our 1 Meg SRAM.

TEST NAME AND DESCRIPTION	TEST DURATION	BIWEEKLY SAMPLE SIZE
HIGH TEMPERATURE OPERATING LIFE (125°C, 6.0V, Checkerboard/Checkerboard Complement Pattern)	1,008 Hours	100 Devices
TEMPERATURE AND HUMIDITY (85°C, 85% R.H., 5.5V, Alternating Bias)	1,008 Hours	50 Devices
AUTOCLAVE (121°C, 100% R.H., 15 PSI, No Bias)	288 Hours	25 Devices
LOW TEMPERATURE LIFE (-25°C, 7.0V, Checkerboard/Checkerboard Complement Pattern)	1,008 Hours	5 Devices
TEMPERATURE CYCLE (-65°C TO +150°C, Air to Air)	1,000 Cycles	50 Devices
THERMAL SHOCK (-55°C TO +125°C, Liquid to Liquid)	700 Cycles	10 Devices
HIGH TEMPERATURE STORAGE (150°C, No Bias)	1,008 Hours	50 Devices
ELECTROSTATIC DISCHARGE (+ and -)	MIL-STD-3015.7	40 Devices

NOTE: Samples pulled from five different lots at finished goods.

Figure 3
SAMPLE ENVIRONMENTAL PROCESS MONITOR – 1 MEG SRAM

FAILURE RATE CALCULATION

The failure rate during the useful life of a device is expressed as percent failures per thousand device hours or as FITs (failures in time, per billion device hours), and is calculated as follows:

Failure Rate = Pn ÷ [Device hours × A.F. environment]

A.F. is relative to the typical operating environment.

where: Pn = Poisson Statistic (at a given confidence level). In our example, Pn = 4.175 at at 60% confidence level.

Device hours = sample size multiplied by test time (in hours) In our example, device hours equal 3.04×10^6 in an accelerated environment.

A.F. =acceleration factor between the stress environment and ***typical*** use conditions. For the 1 Meg SRAM, the acceleration factor between 125°C, 6V (HTOL stress conditions) and 50°C, 5V (typical operating conditions) equals 254.9. (Calculation of this acceleration factor is described in the following section).

Thus, the failure rate of the Micron 1 Meg SRAM family is computed as follows:

Failure Rate = $4.175 \div (3.04 \times 10^6)(254.9) = 5.388 \times 10^{-9}$

where: total device hours at test conditions = 3.04×10^6. Equivalent device hours at typical use conditions (50°C, 5V Vcc) using an acceleration factor of $254.9 = 775 \times 10^6$.

To translate this failure rate into percent failures per thousand device hours, we multiply the failure rate obtained from the equation above by 10^5:

Failure Rate = $(5.388^8 \times 10^{-9}) \times 10^9 = 0.0005388\%$ or 0.0005% per 1K device hours

To state the failure rate in FITs, we multiply the failure rate obtained from the equation above by 10^9:

Failure Rate = $(5.388 \times 10^{-9}) \times 10^9 = 5.388$ or 5 FITs

ACCELERATION FACTOR CALCULATION

Again, using the 1 Meg SRAM for our example, the acceleration factor between high temperature operating life stress conditions (125°C, 6V) and typical operating conditions (50°C, 5.5V) is computed using the following models:

ACCELERATION FACTOR DUE TO TEMPERATURE STRESS

The acceleration factor due to temperature stress is computed using the Arrhenius equation, which is stated as follows:

$$A.F._{t1/t2} = e^{\left[\frac{E_a}{kT_1} - \frac{E_a}{kT_2}\right]}$$

where: k = Boltzmann's constant, which is equal to 8.617×10^{-5} eV/K

T_1 and T_2 = typical operating and stress temperatures, respectively, in kelvins

E = activation energy in eV (For oxide defects, which is the most common failure mechanism for the 1 Meg SRAM, used in our example, the activation energy is determined to be 0.3eV).

Using these values, the temperature acceleration factor between 125°C and 50°C is computed to be 7.62.

ACCELERATION FACTOR DUE TO VOLTAGE STRESS

The acceleration factor due to voltage stress is computed using the following model:

$$A.F._{v1/v2} = e^{[\beta (v_1 - v_2)]}$$

where:

v_1 and v_2 = stress voltage and typical operating voltage, respectively, in volts

β = constant, the value of which was derived experimentally by running several sessions of Micron's intelligent burn-in test sequence at different voltages on large numbers of the device. (For the 1 Meg SRAM used in our example, ß equals 3.5).

Thus, the voltage acceleration factor for the 1 Meg SRAM between 6V (stress condition) and 5V (typical operating condition) is computed to be 33.45.

Finally, the overall acceleration factor due to temperature and voltage stress is calculated as the product of the two respective acceleration factors or:

$$\begin{aligned} A.F._{overall} &= A.F._{temperature} \times A.F._{voltage} \\ &= 7.62 \times 33.45 \\ &= 254.9 \end{aligned}$$

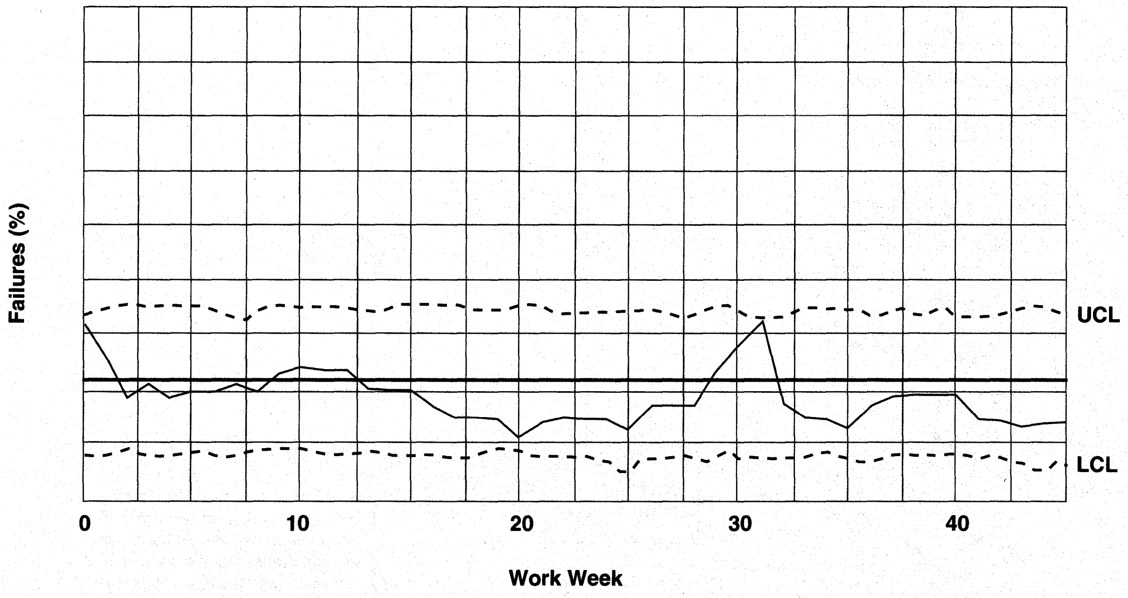


Figure 4
AMBYX™ FOURTH QUARTER FAILURES

OUTGOING PRODUCT QUALITY

Before being sent to our finished goods area, where products are prepared for shipping, a special unit within the quality assurance department takes a one-percent sample from each production lot. These samples are subjected to visual and electrical testing in order to measure the acceptable quality level (AQL) of all outgoing product. Figure 4 shows a flowchart illustrating Micron's AQL test procedure.

Visual or mechanical testing consists of an unaided visual inspection of the sample devices for any physical irregularities which could negatively affect their performance. If a sample device is found to have, for example, a bent lead, a package irregularity or excess solder, the entire lot is returned to our test area for a 100% visual inspection.

Electrical testing of the sample devices is performed using ATE (automatic test equipment) systems. Testing is conducted at room temperature (~25°C) and at 70°C. Should an electrical failure occur, a quality assurance engineer further evaluates the failing device. If after completing this analysis, the quality assurance engineer determines which production monitor/test should have caught the failure and the entire lot is retested at that point in the test flow. These are important steps to preserve the integrity of our test process.

Micron records the percent of devices found to be defective in the total number sampled weekly on a control chart. This chart, containing AQL data for the previous 52 weeks, is presented in weekly management meetings so that the Quality Assurance department can take appropriate action.

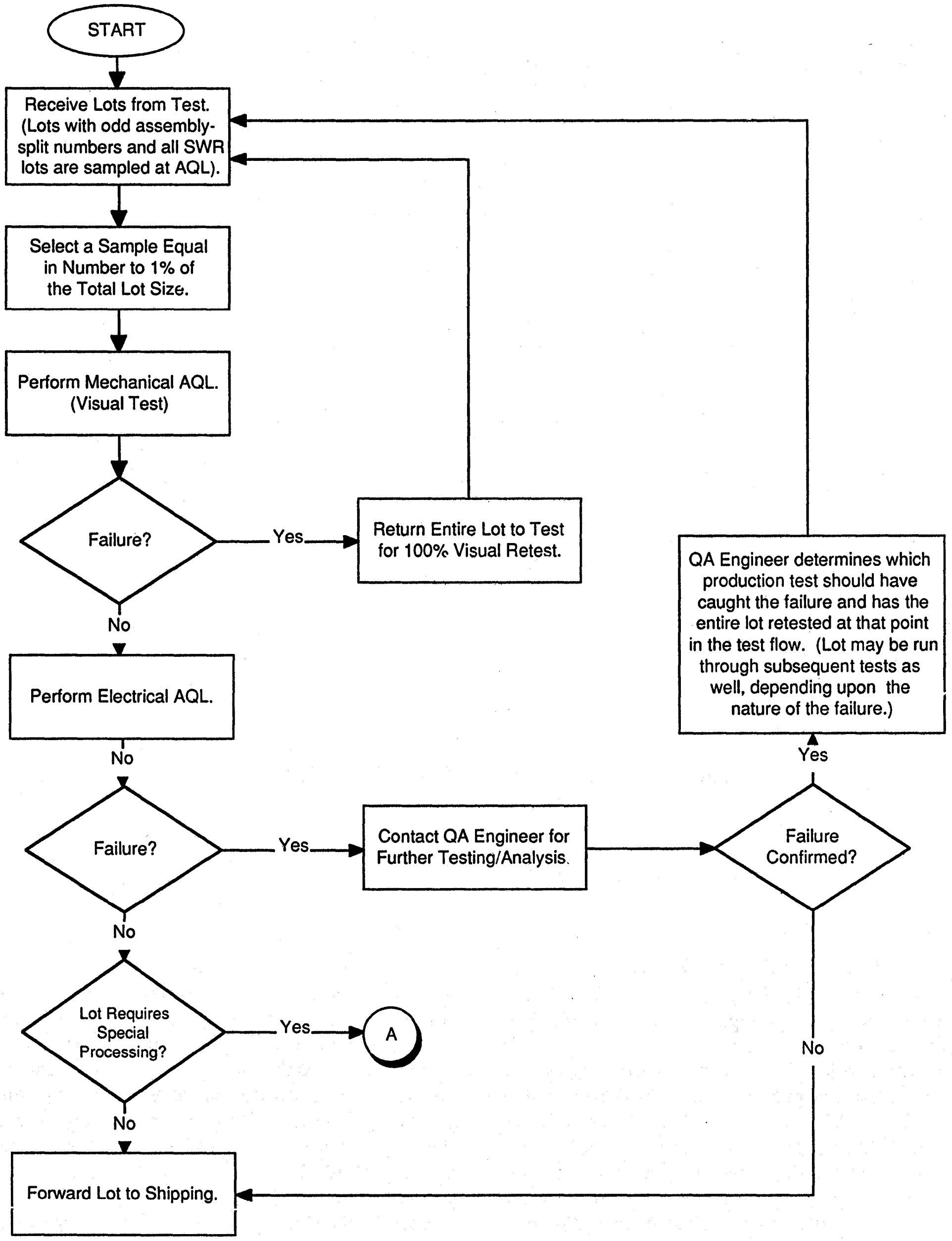


Figure 5
AQL TEST FLOW FOR ALL OUTGOING PRODUCTS

Example of Special Processing:
Lot Mounted on Tape & Reel

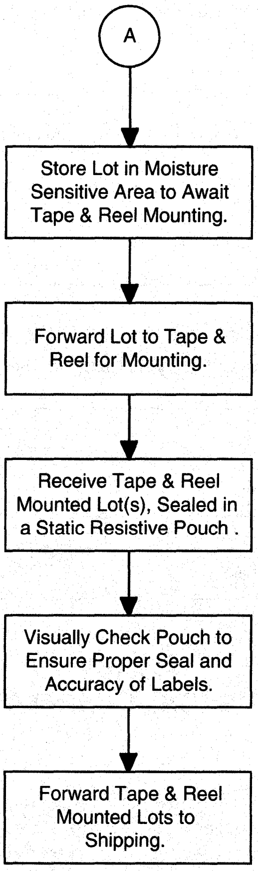


Figure 6
AQL TEST FLOW — SPECIAL PROCESSING

AUTOMATED DATA CAPTURE & ANALYSIS

Micron has developed a sophisticated data capture and analysis system with a computer network tailored to the needs of quality IC manufacturing. Figure 5 shows the various functional areas that provide the input to our VAX data bases.

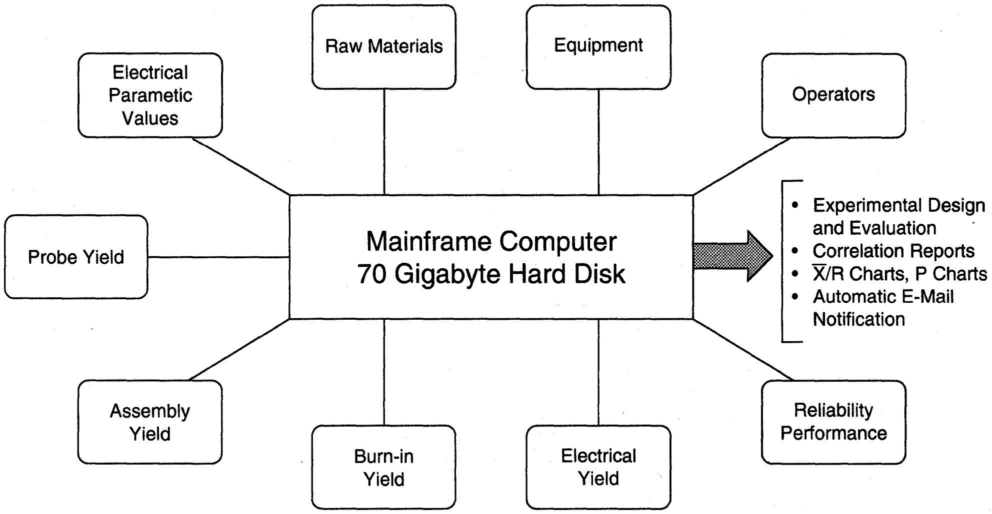


Figure 7
STATISTICAL CORRELATION

DATA CAPTURE

Automated, real-time data capture makes real-time charting ($\overline{X}$ and R charts, etc.) of all critical operations and processes possible and ensures that appropriate personnel know of any unexpected variation on a timely basis. As production lots move through each manufacturing step, detailed information (including step number, lot number, machine number, date/time, and operator number) are entered into the production data base. Automated, highly-programmable measurement systems capture a host of parameters associated with equipment, on-line process material, and environmental variables.

ANALYTICAL TOOLS

By using highly flexible, on-line data extraction programs, system users can tap this vast data base and design their own correlation and trend analyses. Because we can correlate process variables to product performance, we can make on-line projections of the quality of our finished product for a given lot or process run. In addition, we can estimate the impact of process improvements on quality well in advance and can make the impact of process deviations more visible to our engineers. This approach allows us to model yield and quality parameters based on on-line parameters. We then use this model to predict the final product results through the following means.

GROUP SUMMARIES

Summaries, which provide the means and standard deviations of user-defined parametrics, enable system users to compare the parametric values of production lots as well as special engineering lots.

TREND ANALYSIS

Trend charts are routinely generated for critical parameters. System users can plot the means and ranges of any probe or parametric data captured throughout the manufacturing process.

CORRELATION ANALYSIS

Correlation analysis can be performed on any combination of factors; such as equipment, masks or electrical parameters. One report, regularly produced and disseminated to key personnel, takes two groups of lots (one with a high failure rate, the other with a low failure rate) and identifies all the pieces of equipment that are **common** to one or the other group. The report, thus, quickly alerts us to any correlation between a lot with a high failure rate and a particular piece(s) of equipment in the wafer fabrication or assembly areas.

Another regularly produced report analyzes a user-selected set of database parametrics against an index, such as manufacturing yield. Lots are divided into three subgroups (upper yielding, middle yielding and lower yielding). The report then correlates the yields with all electrical parametric values taken on individual lots at wafer sort. It helps us determine which processing step may have caused the yields to vary among the three subgroups.

STATISTICAL PROCESS CONTROL CHARTS

Micron employs SPC control charts throughout the company to monitor and evaluate critical process parameters, such as critical dimensions (CDs), oxide thickness, chemical vapor depositions (CVDs), particle counts, temperature and humidity, and many other critical process and product quality parameters.

OVERLAYS OR WAFER MAPS

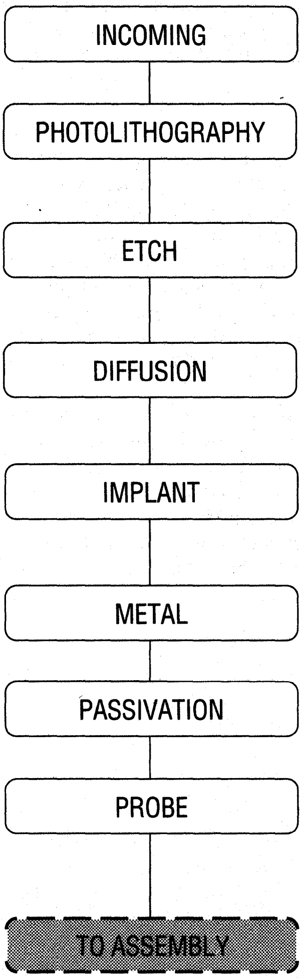
Maps, which are produced for all wafers during probe, show various parameters as a function of position on the wafer and are very useful for problem isolation. Maps may be analyzed individually or in groups. For example, wafers from an entire lot may be analyzed in relation to one particular parameter.

RS/1 DISCOVER/EXPLORE

This analysis software is used for experimental design, and evaluation of results. The statistical approach supported by this software (*t* tests, ANOVA tables, multiregression analysis, etc.) has proven invaluable in reducing time expended for product development and for trouble shooting. It is also used to determine the relationships between process output and probe and parametric data. Using multiregression analysis, for example, we are able to determine the relationship between L effective and CD dimensions to the speed of a device.

The use of automation in data capture, analysis and feedback greatly enhances the flexibility and speed with which we can view all aspects of the manufacturing process. This effective data analysis and feedback system helps to reduce parametric deviations, improve margin to specifications, increase manufacturing yields and provide for more accurate fabrication output planning.

FABRICATION*



Incoming
Verification that the starting material is clean and uniform, and complies with all requirements. Each wafer receives an individual laser scribe for total product traceability.

Photolithography
Wafers are coated with a layer of light-sensitive photoresist. Specified sections of the wafer are exposed by projecting ultraviolet light onto the wafer through a mask. The exposed photoresist hardens and becomes impervious to etchants.

Etch
The areas of the wafer not protected by the exposed photoresist are removed by either plasma (dry etch) or acid (wet etch). The photoresist is then cleaned ("stripped") off of the wafer, leaving a pattern in the exact design of the mask.

Thermal Processing
Wafers are placed in furnaces where they are exposed to various gases while being heated to temperatures over 1,000 degrees celsius.Layers similar to glass are grown on the wafer. These layers help form the building blocks for the circuitry constructed on each wafer.

Implant
Wafers are bombarded with positively or negatively charged dopant ions, which are implanted into the silicon. This process changes electrical characteristics in selective areas of the silicon. This is called "doping," and forms conductive regions on the wafer.

Metal
A thin layer of aluminum or other metal is deposited and patterned, forming interconnections between various regions of the die.

Passivation
The fabrication process is completed by forming a final glass layer on the wafer. This layer protects the circuits from contamination or damage through the testing and packaging process flows.

Probe
When the fabrication process is complete, each wafer consists of many "dice." Each die on the wafer is taken individually through a series of tests. A computer attached to a probe card tests the die and produces a "wafer map" storing data on each functioning (good) die . All data is collected and stored for each die. Wafer maps are used in assembly to ensure that only good dice are packaged.

Assembly (see next page)

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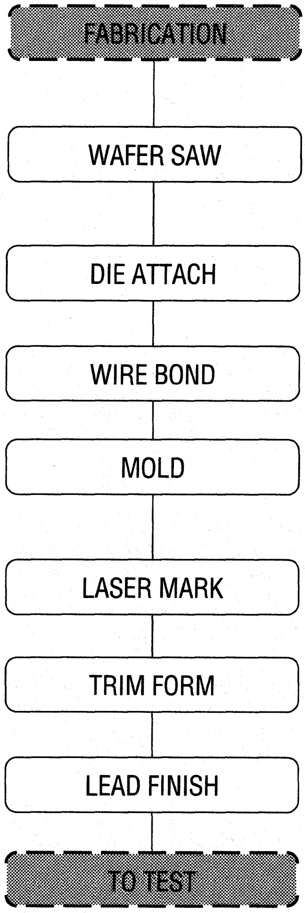
*This flow is general and is based on DRAM products.

ASSEMBLY*



Fabrication

Before assembly, incoming raw silicon wafers are processed through a myriad of fabrication steps. This fabrication process yields fully-fabricated wafers containing complete, functioning circuitry in die form. These wafers go to assembly so each individual die may be separated and packaged prior to final testing.

Wafer Saw

Wafers that have finished Fab processing and probe are automatically mounted on a carrying film. The wafer is then sawed using an automated, high-speed diamond blade and high-pressure water. This separates each individual die from the others on the wafer without disturbing the carrying film.

Die Attach

With automated pick-and-place equipment, the good dice as specified by the probe "wafer map" are removed from the carrier film. Each die is attached to a leadframe with a layer of adhesive.

Wire Bond

With high-speed automated equipment, interconnections are made with gold wire (the diameter of a human hair). These interconnections are between the aluminum circuit on the die and the lead fingers of the leadframe.

Mold

A heated mold with a hydraulic press is used to transfer hot thermosetting plastic into mold cavities where the leadframe is placed. This encapsulation protects the die and the interconnections throughout the useful life of the product.

Laser Mark

A laser mark is scribed on the bottom side of the package. This mark is a code used to identify the assembly manufacturing lot.

Trim/Form

A press with a tool set is used to cut and form leads of the lead frame into specified shapes. Some packages have leads formed for surface mount applications. Other packages have leads for through-hole applications.

Lead Finish

Each package is given a lead finish of tin/lead (solder) to ensure reliable application by the customer.

Test (see next page)

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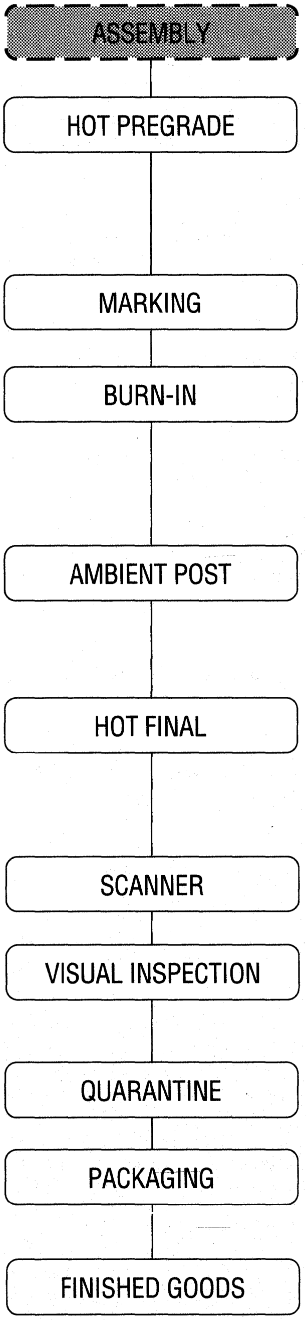
*This flow is general and is based on DRAM products.

TEST*



Assembly

Fully fabricated silicon wafers reach assembly after each die has been probed to screen out failures. Passing chips are then carried through a number of steps to become individual units in leaded packages.

Hot Pregrade

At temperatures ranging from 83°C to 125°C, parts are tested for speed grade and functionality. Parametric tests are performed to detect opens, shorts, input and output leakage, input and output high and low levels and standby current. Functional tests include low and high Vcc margin, vbump, speed sorting, dynamic and static refresh, and a full range of patterns and backgrounds. Patterns performed include row fast, column fast, single and multiple walking columns and diagonals, moving inversions, and fast page or static column. Backgrounds used include solids, checkerboard, row stripes, column stripes and parity. Specific tests and temperatures as applicable to specific products.

Marking

Devices are marked with ink with the following information: year, special process designator, part type, package type and speed grade.

Burn-in

Micron uses its exclusive AMBYX™ intelligent burn-in and test system to screen out infant mortalities. Devices are dynamically burned-in using checkerboard/checkerboard complement patterns in four intervals under the following conditions: 125°C, 7.5V Vcc for the first two intervals and 125°C, 6V Vcc for the final two intervals. Functional testing is performed at 85°C and back to 25°C AMBYX™ tests for thermal intermittent opens. Devices are also functionally tested at burn-in conditions (125°C, 7.5V) at the beginning of the burn-in cycle to verify that the devices under test are being properly exercised.

Ambient Post

At a temperature of 25°C, parametric tests include input and output leakage as well as standby and operating currents. Functional tests include low and high Vcc margin, vbump, speed sorting, dynamic and static refresh, and a full range of patterns and backgrounds. Patterns performed include row fast, column fast, single and multiple walking columns and diagonals, moving inversions and fast page or static column. Backgrounds used include solids, checkerboard, row stripes, column stripes and parity.

Hot Final

At a temperature of 78°C to 100°C, parametric tests include input and output leakage as well as input and output high and low levels. Functional tests include low and high Vcc margin, vbump, speed sorting, dynamic and static refresh, and a full range of patterns and backgrounds. Patterns performed include row fast, column fast, single and multiple walking columns and diagonals, moving inversions and fast page or static column. Backgrounds used include solids, checkerboard, row stripes, column stripes and parity.

Scanner

Devices are optically scanned by an automated scanning machine for bent leads, incorrect splay, coplanarity failures and tweeze failures. Passing and failing parts are then sorted into appropriate bins.

Visual Inspection

All devices, now tested to be functional, are visually inspected for cosmetic defects such as bent leads, poor marks, broken packages and poor solder. Defective products are removed and repaired if possible. Data on the type of defects found is carefuly recorded and used for improving the manufacturing processes in both assembly and test.

Quarantine

All production lots are held at this stage until a quality assurance monitoring program confirms that electrical and environmental specifications are met.

Packaging

Devices are prepared for shipping. They may remain in tubes or they may be mechanically placed in tape-and-reel packages, ready for application in automatic pick-and-place machines. Products will be either dry packed in vacuum sealed bags, or placed in black antistatic bags.

Finished Goods

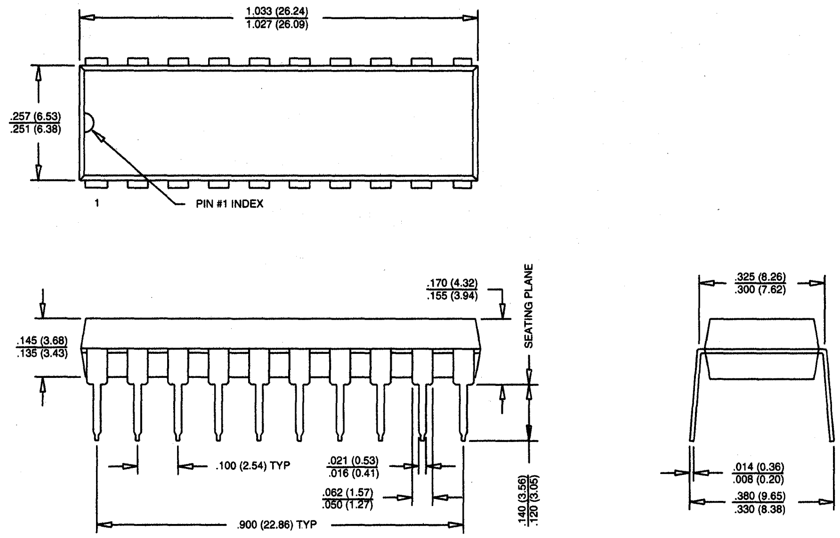
Devices are shipped through a system that maintains lot identity.

*This flow is general and is based on DRAM products.

INDEX

20-PIN PLASTIC DIP

A-4

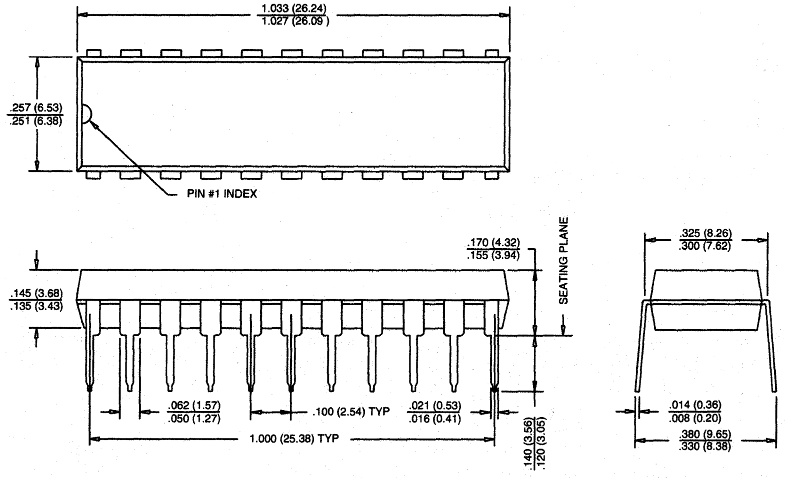


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

22-PIN PLASTIC DIP

A-6

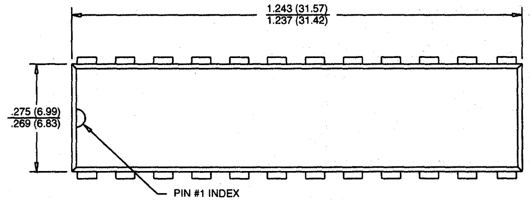


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

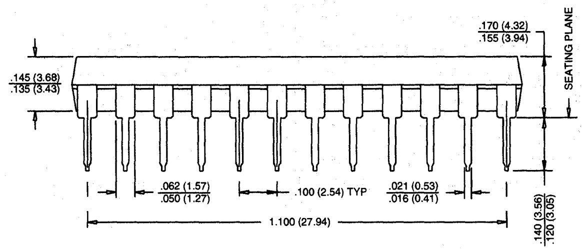
2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

24-PIN PLASTIC DIP

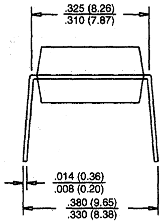
A-7



TOP VIEW



SIDE VIEW



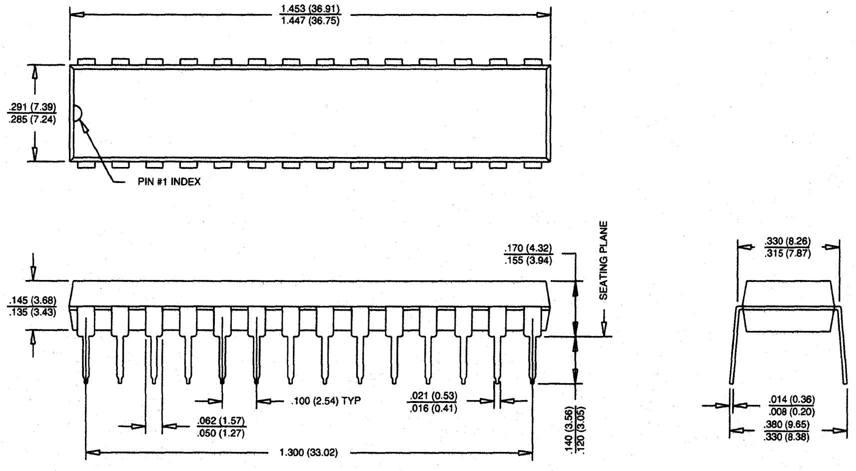
END VIEW

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

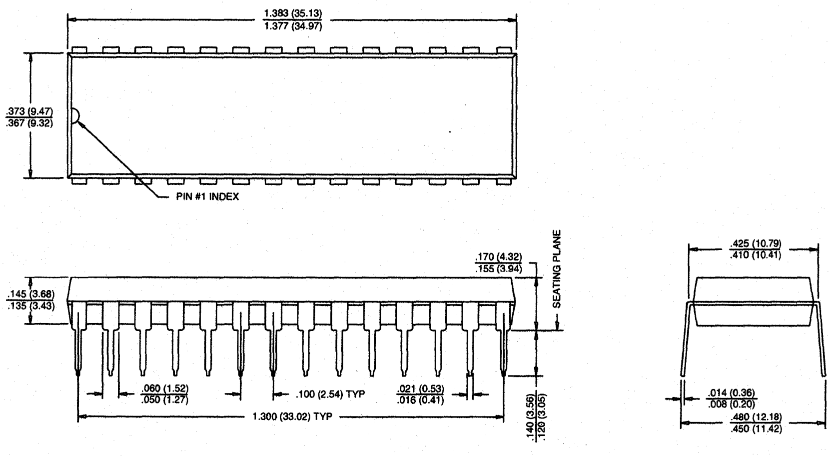
28-PIN PLASTIC DIP

A-9



28-PIN PLASTIC DIP

A-10

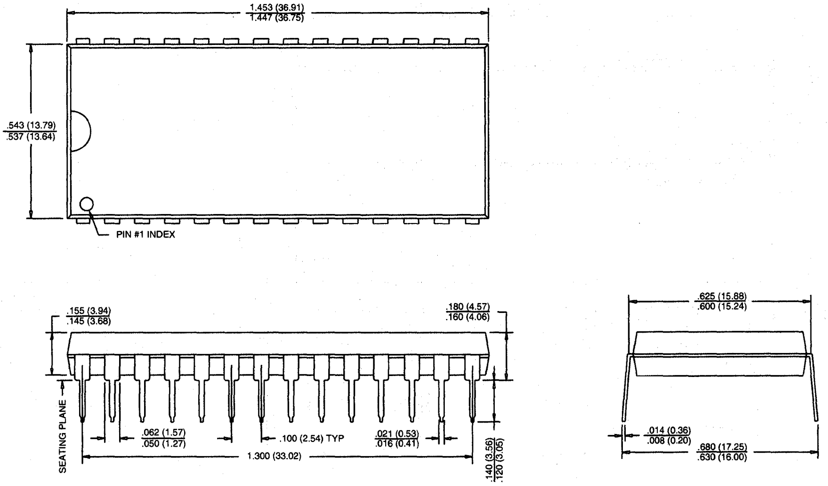


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC DIP

A-11

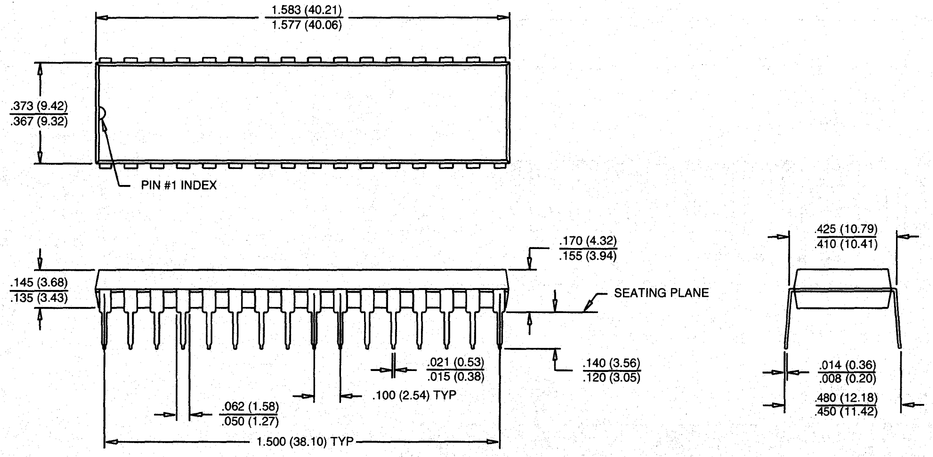


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

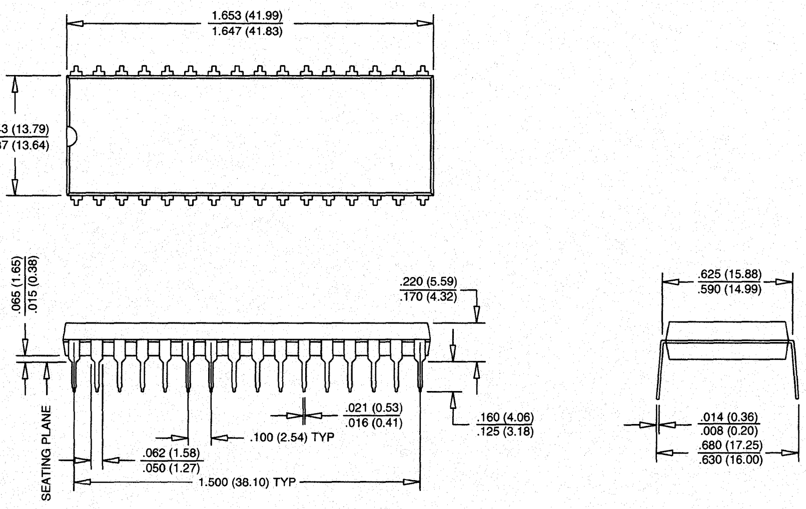
32-PIN PLASTIC DIP

A-12



32-PIN PLASTIC DIP

A-13

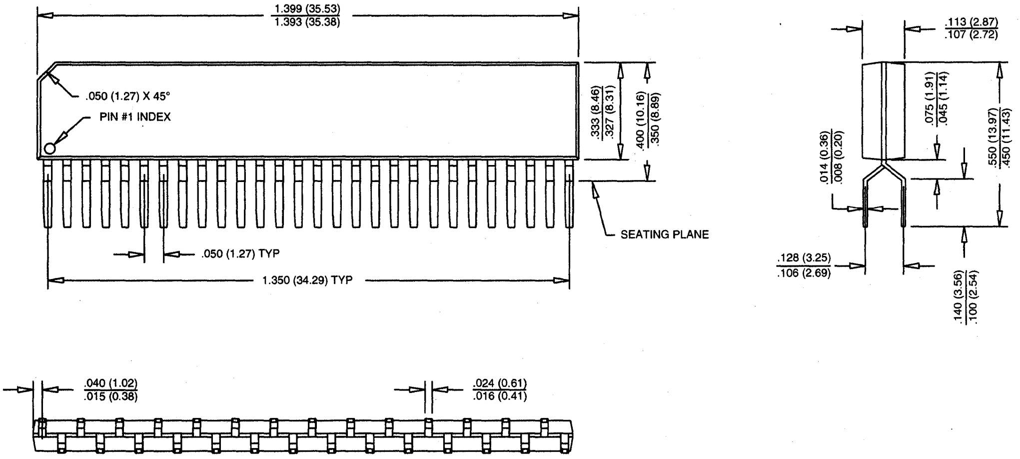


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC ZIP

C-5

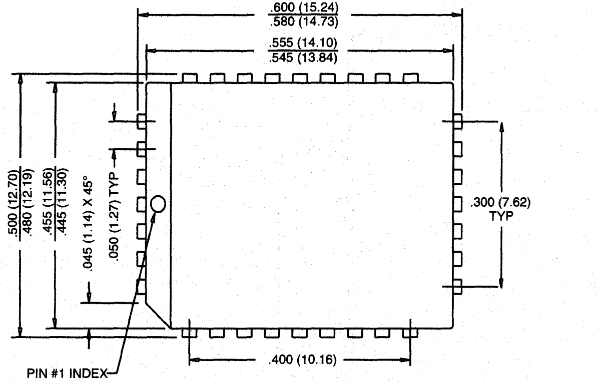


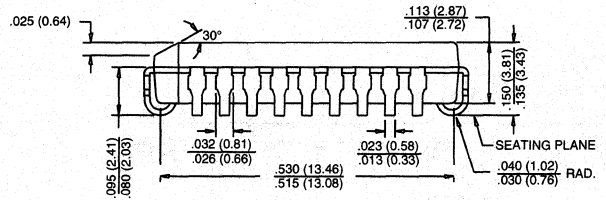
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

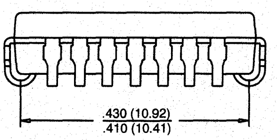
2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLCC

D-2







NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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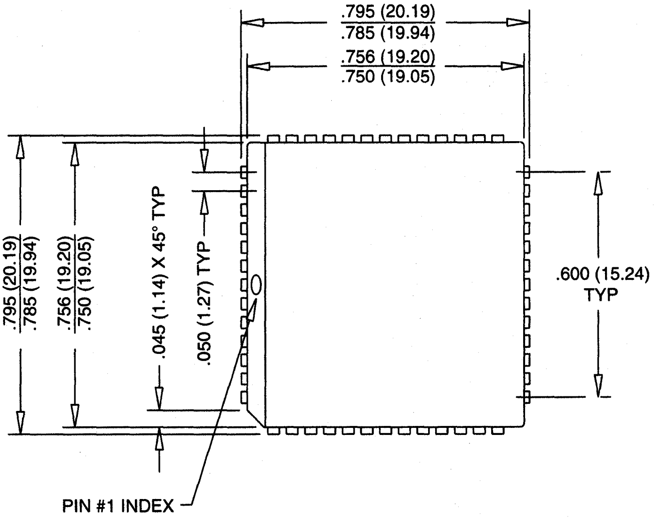
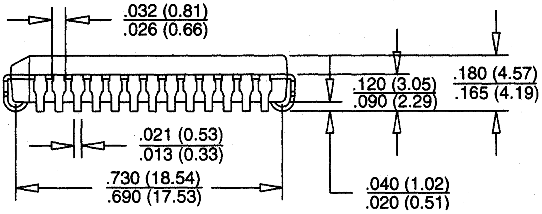
52-PIN PLCC

D-3





NOTE:
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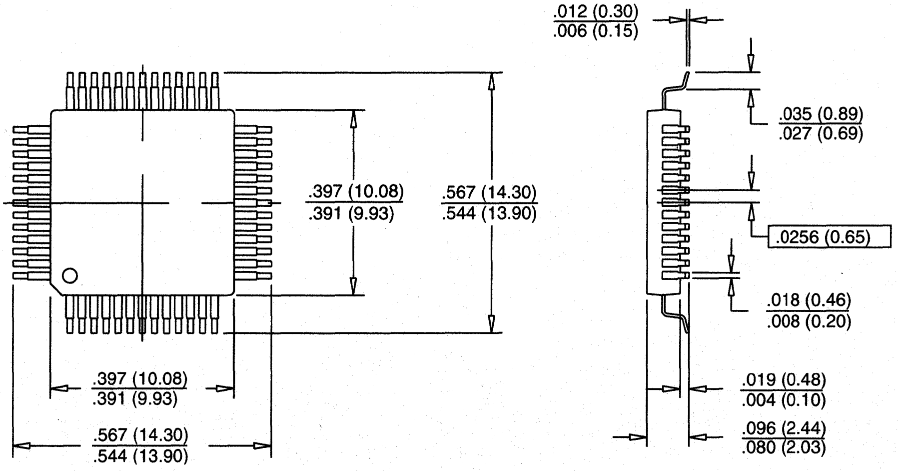
2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

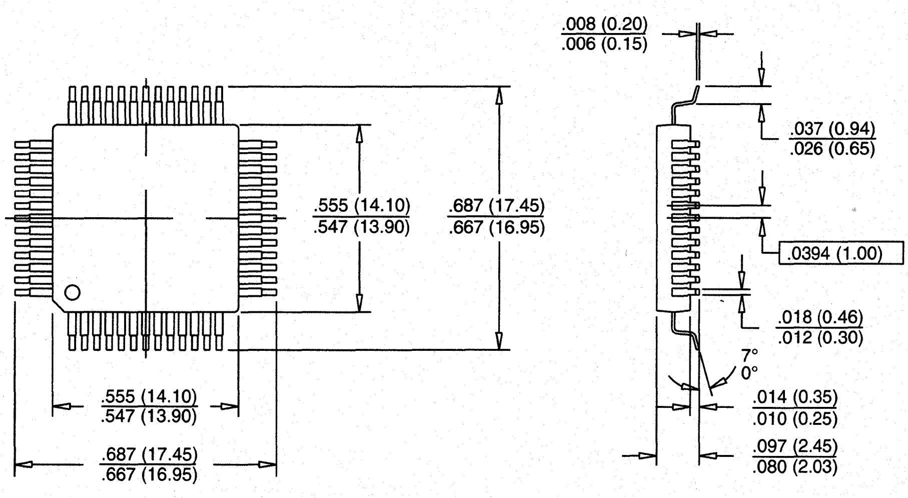
52-PIN PQFP

D-4



52-PIN PQFP

D-5

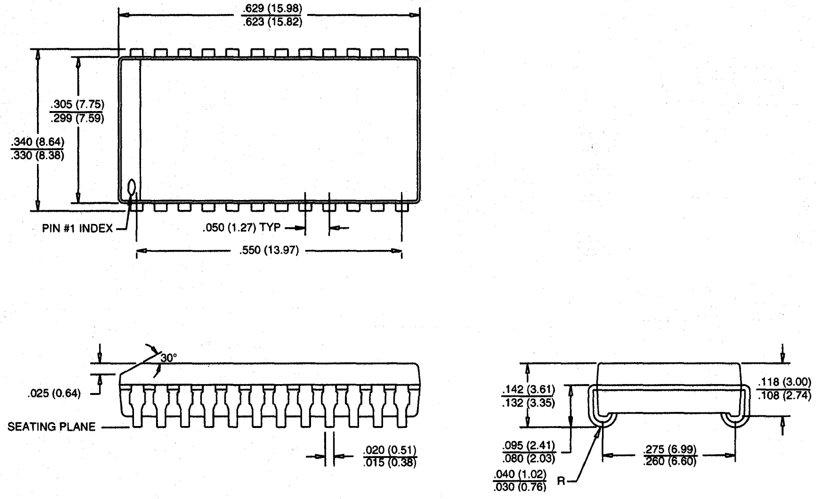


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

24-PIN PLASTIC SOJ

E-4



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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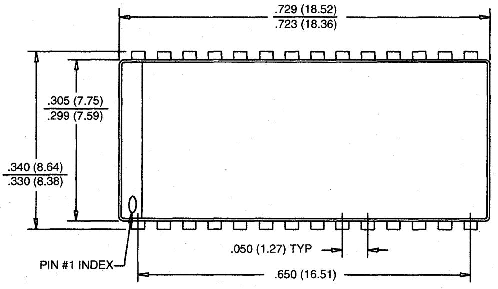
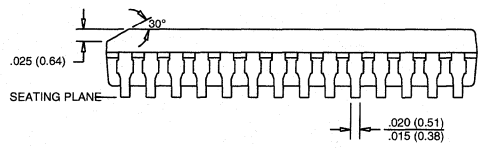
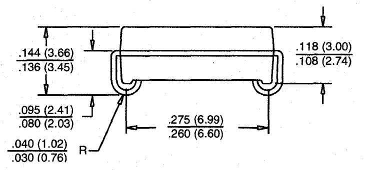
28-PIN PLASTIC SOJ

E-8

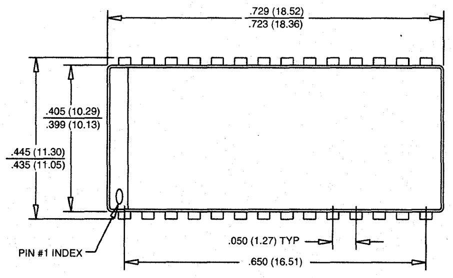


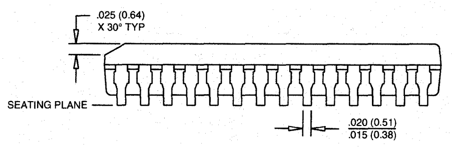


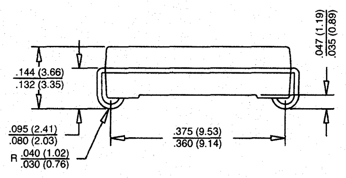


28-PIN PLASTIC SOJ

E-9





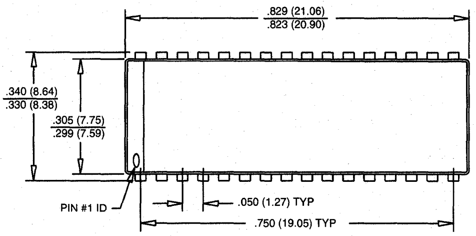


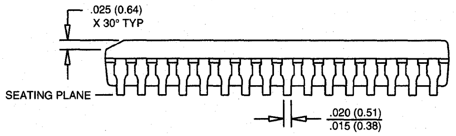
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

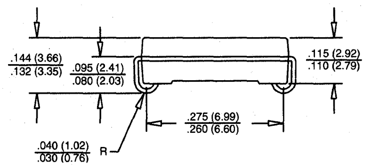
2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC SOJ

E-10

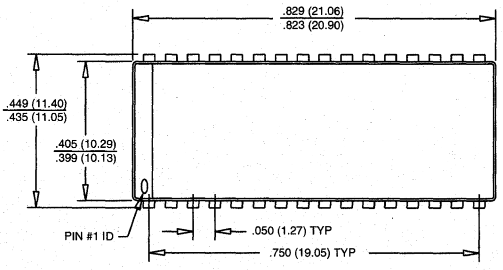


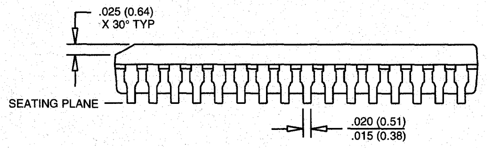


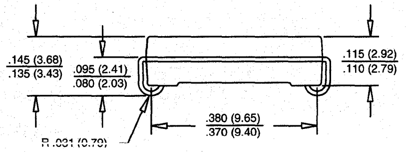


32-PIN PLASTIC SOJ

E-11







NOTE:
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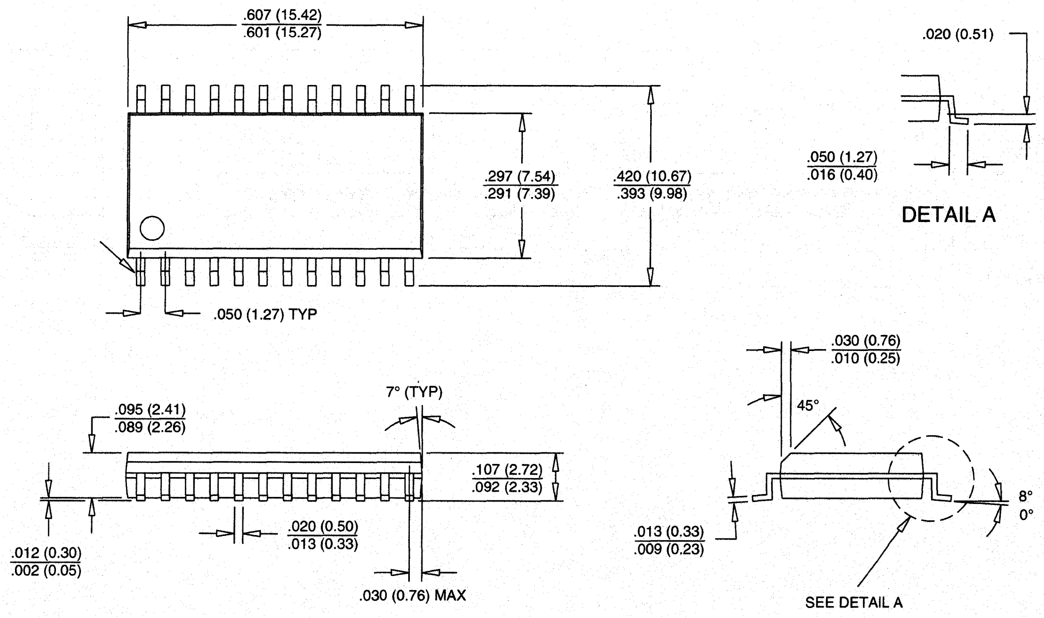
24-PIN PLASTIC SOIC

F-1

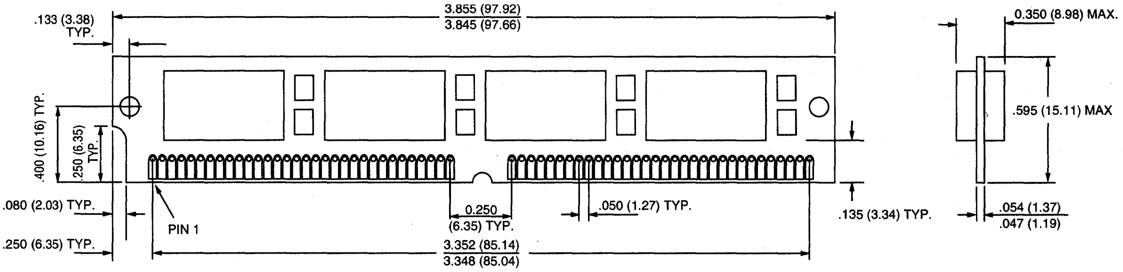


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

64-PIN MODULE SIMM

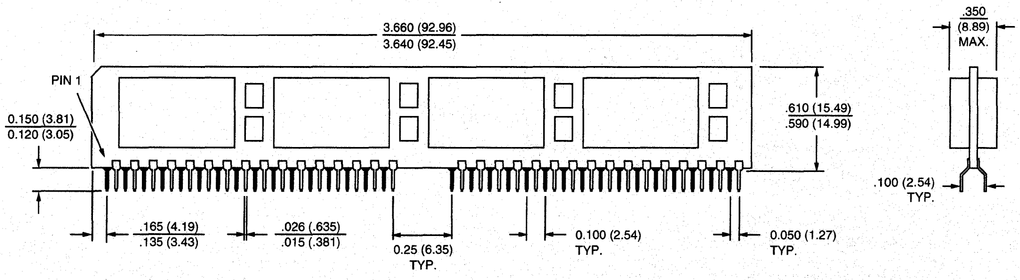
I-11



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

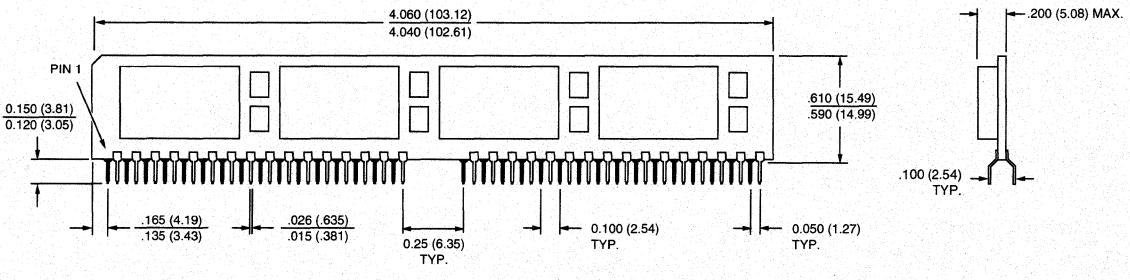
64-PIN MODULE ZIP

J-1



64-PIN MODULE ZIP

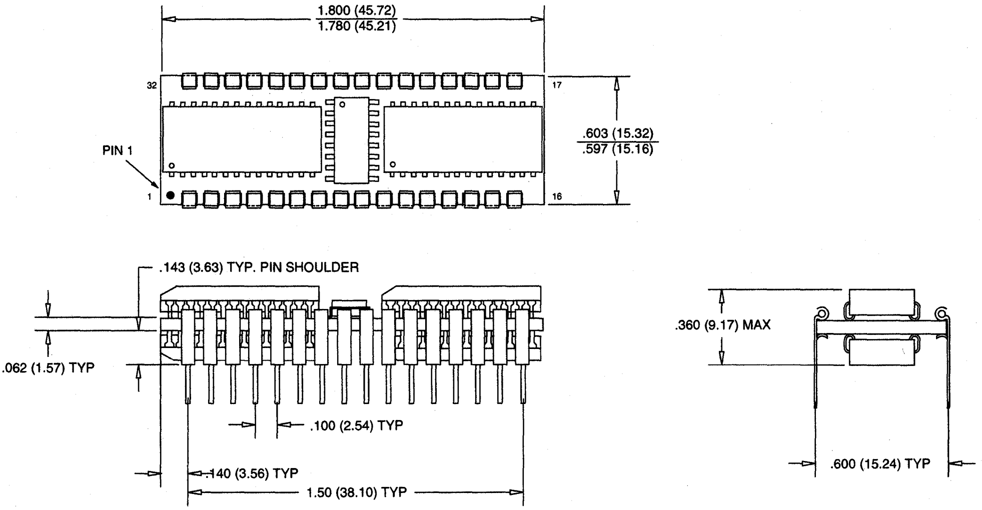
J-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

32-PIN MODULE DIP

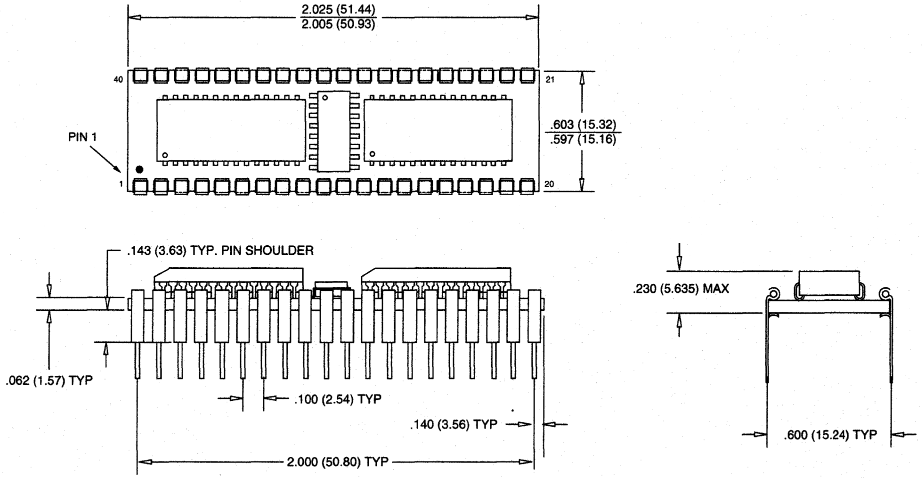
K-1



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

40-PIN MODULE DIP

K-2



40-PIN MODULE DIP

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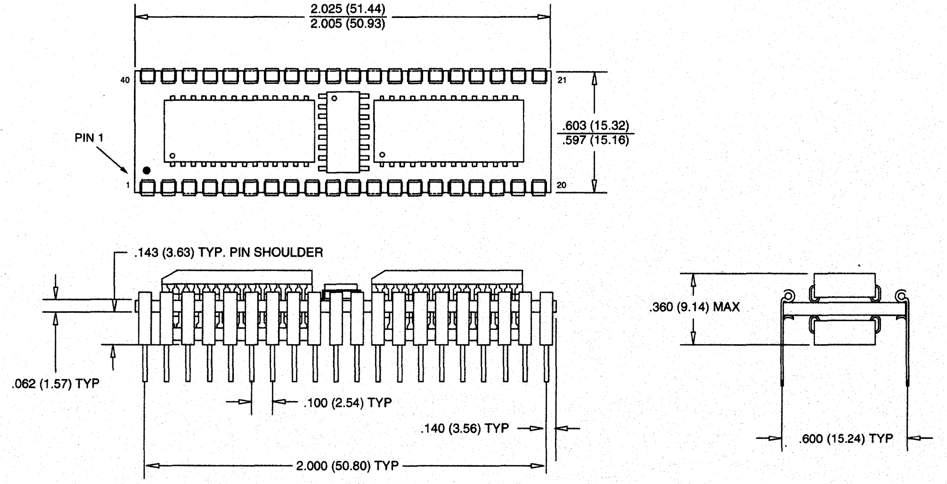


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

MICRON
TECHNOLOGY, INC.

CSN-01

CUSTOMER SERVICE NOTE

STANDARD SHIPPING BAR CODE LABELS

INTRODUCTION

Effective July 1, 1991, Micron Technology, Inc., will implement new standard bar coding labels which will accompany all shipments. These labels conform to EIA Standard 556.

Samples and tape-and-reel boxes will have their own individual bar code labels (see **CSN-02**). The bar code labels will allow customers to scan individual Micron containers for quick order verification. Figure 1 shows an example of the standard bar coding label.

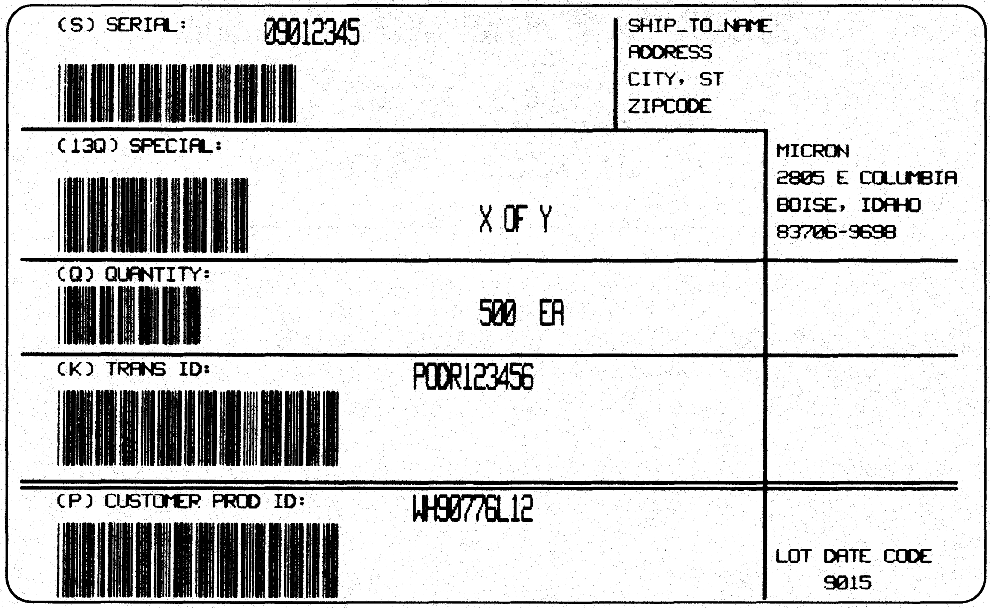
BAR CODE INFORMATION

The information provided on the label is:

(S) — Serial: Individual box serial number
(13Q) — Special: Individual box number and total number of boxes in the shipment (example: 2 of 10)
(Q) — Quantity: Total quantity of parts in the box
(K) — Trans ID: Customer purchase order number
(P) — Customer Product ID: Customer part number. If a customer part number is not designated, the Micron part number will be printed.

ADDITIONAL SALES INFORMATION

Ship-to-Name:	Customer's name and ship-to address
Ship-From-Name:	Micron name and address
Lot Date Code:	Indicates date of oldest lot in the box



(S) SERIAL: 09012345

SHIP_TO_NAME
ADDRESS
CITY, ST
ZIPCODE

(13Q) SPECIAL: X OF Y

MICRON
2805 E COLUMBIA
BOISE, IDAHO
83706-9698

(Q) QUANTITY: 500 EA

(K) TRANS ID: PODR123456

(P) CUSTOMER PROD ID: WH90776L12

LOT DATE CODE
9015

Figure 1
Standard Bar Code Label

MICRON
TECHNOLOGY, INC.

CSN-02

CUSTOMER SERVICE NOTE

TAPE-AND-REEL/SAMPLE BAR CODE LABELS

INTRODUCTION

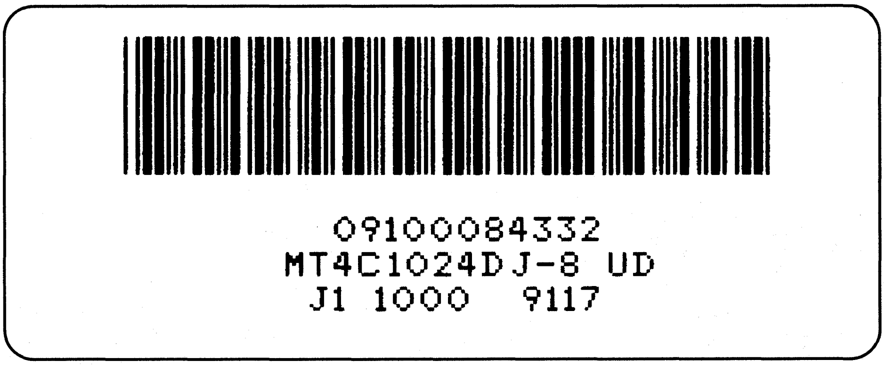
Micron Technology, Inc., provides a standard bar code label on each individual sample and tape-and-reel box. The standard bar code label allows scanning of Micron shipping containers at a receiving dock for quick order verification.

Figure 1 shows an example of the standard bar code label.

BAR CODE INFORMATION

The information provided on the label is:

Label 1: Individual box number (in a multi-box shipment)
Actual box number printed
Micron part number/speed/customer code
Part type/rev/quantity/date code of oldest lot*



09100084332
MT4C1024DJ-8 UD
J1 1000 9117

Figure 1
Label 1

---

*Indicates that more than one date code is contained on the reel.

COMPONENT PRODUCT NUMBERING SYSTEM

Format = AA BB CC DDDD EE FFF-GG HH HH*

PRODUCT FAMILY

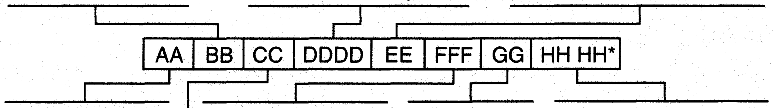
DRAM	= 4
DPDRAM	= 42
TPDRAM	= 43
DRAM FIFO	= 46
SRAM	= 5
FIFO	= 52
CACHE/LATCHED SRAM	= 56
SYNCHRONOUS SRAM	= 58

DEVICE NUMBER
(NUMBER CAN BE MODIFIED TO INDICATE VARIATIONS)

DRAM	= Width, Density
DPDRAM	= Width, Density
TPDRAM	= Width, Density
DRAM FIFO	= Width, Density
SRAM	= Total Bits, Width
LATCHED SRAM	= Total Bits, Width
CACHE SRAM	= Density, Width
FIFO	= Width, Density
SYNCH. SRAM	= Density, Width

OPTIONS
(LISTED IN HIERARCHY IN CASE OF MULTIPLE OPTIONS)

Interim (Errata) Version	= I
Low Power, Extended Refresh DRAM and Low Power SRAM	= L
JEDEC Test Mode (4 Meg DRAM)	= J
3.3V	= V
3.3V, Low Power, Extended Refresh	= H
2K Refresh (16 Meg DRAM)	= R
Self & Extended Refresh, Low Power	= S



PRODUCT LINE IDENTIFIER

Micron Technology Component Product	= MT

PROCESS TECHNOLOGY

CMOS	= C
BICMOS	= B

PACKAGE CODE

PLASTIC	
DIP	= Blank
DIP (Wide Body)	= W
ZIP	= Z
LCC	= EJ
SOIC	= SG
QFP	= LG
TSOP (Type II)	= TG
TSOP (Reversed)	= RG
TSOP (Longer)	= TL
SOJ	= DJ
SOJ (Reversed)	= DR
SOJ (Longer)	= DL
DIE	
Die	= XDC
Wafer	= XWC
Military Die	= XD
Military Wafer	= XW
CERAMIC	
DIP	= C
DIP (Wide Body)	= CW
LCC (Narrow Body)	= ECN
LCC	= EC
LCC (Wide Body)	= ECW
SOIC	= CG
SOJ	= DCJ
PGA	= CA
FLAT PACK	= F

ACCESS TIME

-8	= 8ns or 80ns
-10	= 10ns or 100ns
-12	= 12ns or 120ns
-15	= 15ns or 150ns
-17	= 17ns
-20	= 20ns
-25	= 25ns
-35	= 35ns
-45	= 45ns
-50	= 50ns
-53	= 53ns
-55	= 55ns
-60	= 60ns
-70	= 70ns
-85	= 85ns

PROCESSING* LEVEL/TEMP/SPECIAL

Commercial Process	
0°C to +70°C	= Blank
-40°C to +85°C	= IT
-40°C to +125°C	= AT
-55°C to +125°C	= XT
MIL-STD-883C	
-55°C to +125°C	= 883C
-55°C to +110°C (DRAMs)	= 883C
0°C to +70°C	= M070
Low Volt Data Retention	= L
Tape and Reel	= TR
Bar Code	= BC
EPI Wafer	= E

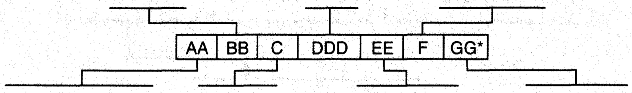
* Multiple processing codes are separated by a space. Listed in hierarchy in case of multiple options.

MODULE PRODUCT NUMBERING SYSTEM

Format = AA BB C DDD EE-FF GG*

PACKAGE CODE

DIP	= D
GOLD PLATE	= G
ZIP	= Z
SIP	= N
SIMM	= M



PRODUCT LINE IDENTIFIER

Micron Technology Component Product	= MT

RAM FAMILY

SRAM	= S
DRAM	= D

ORGANIZATION

Width

SPECIAL DESIGNATOR*

Partial	= P
Low Power	= L

* Multiple processing codes are separated by a space. Listed in hierarchy in case of multiple options.

SALES INFORMATION

ORDER INFORMATION

Each Micron component family is manufactured and quality controlled in the USA at our modern Boise, Idaho, facility employing Micron's low-power, high-performance CMOS silicon-gate process. Micron products are functionally equivalent to other manufacturers' products meeting JEDEC standards. Device functionality is consistently assured over a wider power supply, temperature range and refresh range than specified. Each unit receives continuous system-level testing during many hours of accelerated burn-in prior to final test and shipment. This testing is performed with Micron's exclusive **AMBYX™** intelligent burn-in and test system.

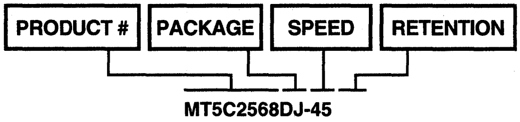
Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's quality assured policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

Telphone: (208) 368-3900
FAX: (208) 368-4431
Customer Comment Line: (800) 932-4992

ORDER EXAMPLES

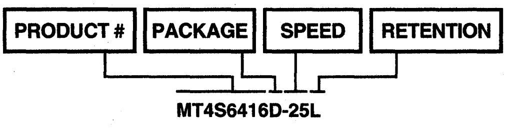
SRAM

32K x 8, 45ns in Plastic SOJ



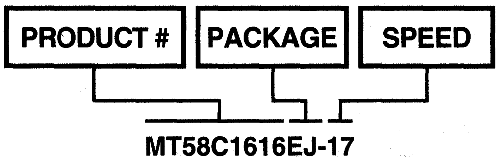
SRAM MODULE

64K x 16, 25ns in DIP Module with 2V Data Retention



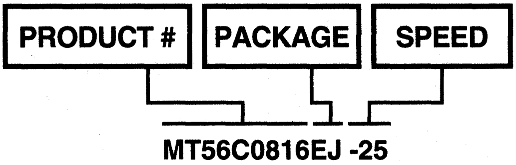
SYNCHRONOUS SRAM

16K x 16, 17ns in Plastic LCC



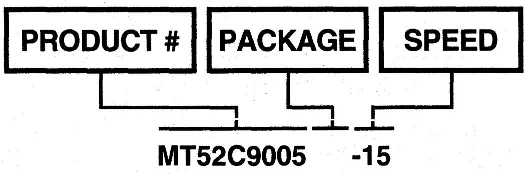
CACHE DATA SRAM

Dual 4K x 16, Single 8K x 16, 25ns in Plastic LCC



FIFO

512 x 9, 15ns DIP



ALABAMA

Representative

Southeast Technical Group
101 Washington, Suite 6
Huntsville, AL 35801
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Fax - 205-534-2384

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Business Center, Suite 1
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FAX - 205-830-2565

Pioneer Technology
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Huntsville, AL 35816
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FAX - 205-837-9358

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FAX - 602-820-7054

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FAX - 602-966-4826

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Phoenix, AZ 85040
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FAX - 602-437-2348

Wyle Laboratories
4141 E. Raymond St., Suite #1
Phoenix, AZ 85040
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FAX - 602-437-2124

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FAX - 408-629-4892

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FAX - 214-343-5988

Pioneer Electronics
13710 Omega Road
Dallas, TX 75234
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FAX - 214-490-6419

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FAX - 214-644-5064

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FAX - 408-452-8139

Hamilton
743 3300

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FAX - 619-453-0034

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FAX - 818-775-1302

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FAX - 714-380-4747

Anthem Electronics Incorporated
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Fax - 916-624-9750

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FAX - 408-432-4044

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FAX - 714-727-6066

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San Jose, CA 95134
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FAX - 408-954-9113

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El Segundo, CA 90245
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FAX - 213-322-1763

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3000 Bowers Ave.
Santa Clara, CA 95051
Phone - 408-727-2500
FAX - 408-727-5896

Wyle Laboratories
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Irvine, CA 92714
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FAX - 714-863-0473

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Rancho Cordova, CA 95742
Phone - 916-638-5282
FAX - 916-638-1491

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9525 Chesapeake Dr.
San Diego, CA 92123
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FAX - 619-565-0512

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FAX - 818-708-7436

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22700 Savi Ranch Pkwy.
Yorba Linda, CA 92686
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FAX - 714-921-2715

Zeus Components, Inc.
5236 Colodny Dr., Suite 102
Agoura Hills, CA 91301
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FAX - 818-889-2464

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5625 Ruffin Road, Suite 200
San Diego, CA 92123
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6276 San Ignacio Ave., Suite E
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20 Regan Road, Unit #14
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FAX - 416-840-6091

Clark-Hurman Associates
66 Colonnade Road, Suite 205
Nepean, Ontario K2E 7K7
Canada
Phone - 613-727-5626
FAX - 613-727-1707

Clark-Hurman Associates
19 Donegani, Suite 5
Pointe Claire, Quebec H9R 2V6
Canada
Phone - 514-426-0453
FAX - 514-426-0455

Davetek Marketing
#37 4429 Kingsway
Burnaby, BC V5H 2A1
Canada
Phone 604-430-3680
FAX - 604-435-5490

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Semad Electronic
85 Spy Court
Markham, Ontario L3R 4Z4
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Phone - 416-475-3922
FAX - 416-475-4158

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Ottawa, Ontario K2C OR3
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FAX - 613-727-9489

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8563 Government Street
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FAX - 604-420-0124

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Pointe Claire, PQ H9R 4Z7
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FAX - 514-694-0965

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6120 3rd St. S.E., Unit 9
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4891 Independence St.
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373 Inverness Dr. South
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12503 E. Euclid Dr., #20
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FAX - 303-790-4991

Wyle Laboratories
451 E. 124th Street
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6925 Canby, Bldg. 109
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FAX - 914-937-2553

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Omega Electronic Sales Incorporated
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FAX - 215-244-4104

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Horsham, PA 19044
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FAX - 215-674-3107

Military Distributor

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Columbia, MD 21045
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FAX - 301-964-9784

DISTRICT OF COLUMBIA

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235 Prince George St.
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FAX - 301-921-3852

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FAX - 407-259-1323

Photon Sales, Inc.
715 Florida St.
Orlando, FL 32806
Phone - 407-896-6064
FAX - 407-896-6197

Photon Sales, Inc.
4321 W. McNab Road, A-20
Pompano Beach, FL 33069
Phone - 305-977-6872
FAX - 305-977-0056

Photon Sales, Inc.
115 112th Ave. N. #301
St. Petersburg, FL 33716
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FAX - 813-578-0104

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FAX - 813-796-4880

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Orlando, FL 32810-2696
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FAX - 407-290-0164

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Largo, FL 34646
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FAX - 813-544-4394

Hall-Mark Electronics Corporation
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Pompano Beach, FL 33069-4806
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FAX - 305-971-9339

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489 E. Semoran Blvd., #145
Casselberry, FL 32707
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FAX - 407-767-5002

Pioneer Technologies
337 South-North Lake #1000
Altamonte Springs, FL 32701
Phone - 407-834-9090
FAX - 407-834-0865

Pioneer Technologies
5500 Rio Vista Dr.
Clearwater, FL 34620
Phone - 813-531-5037
FAX - 918-492-0546

Pioneer Technologies
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Deerfield Beach, FL 33442
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FAX - 305-481-2950

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FAX - 407-365-2356

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FAX - 404-979-2055

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3425 Corporate Way, Suite A
Ouluth, GA 30136
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FAX - 404-476-8806

Pioneer Technologies
3100F Northwoods Place
Norcross, GA 30071
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FAX - 408-452-2281

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Phone - 408-432-4000
FAX - 408-432-4044

Wyle Laboratories
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Santa Clara, CA 95051
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IDAHO

Representative

Contact Micron
Component Sales
Phone - 208-368-3900
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Customer Comment Line - 800-932-4992

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FAX - 408-629-4892

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13755 St. Charles Rock Road
Bridgeton, MO 63044
Phone - 314-291-5003
FAX - 314-291-7958

Industrial Representatives, Inc.
8430 Gross Point Road
Skokie, IL 60077
Phone - 708-967-8430
FAX - 708-967-5903

Distributors

Anthem Electronics Incorporated
1300 Remington, Suite A
Schaumburg, IL 60173
Phone - 708-884-0200
FAX - 708-884-0480

Hall-Mark Electronics Corporation
210 Mittel Dr.
Wooddale, IL 60191
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FAX - 708-860-0239

Pioneer Standard
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Addison, IL 60101
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FAX - 708-495-9831

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Zeus Components, Inc.
100 Midland Ave.
Port Chester, NY 10573
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Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

INDIANA

Representatives

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7321 Shadeland Station, Suite 256
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Phone - 317-841-0010
Fax - 317-841-0107

Scott Electronics, Inc.
Lima Valley Office Village
8109 Lima Road
Fort Wayne, IN 46818
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Fax - 219-489-1842

Distributors

Hall-Mark Electronics Corporation
4275 W. 96th Street
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Pioneer Standard
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Indianapolis, IN 46240
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FAX - 317-573-0979

Military Distributors

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FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

IOWA

Representative

Advanced Technical Sales
375 Collins Road N.E.
Cedar Rapids, IA 52402
Phone - 319-393-8280
FAX - 319-393-7258

Distributors

Anthem Electronics Incorporated
7646 Golden Triangle Dr.
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3045

Hall-Mark Electronics Corporation
210 Mittel Dr.
Wooddale, IL 60191
Phone - 708-860-3800
FAX - 708-860-0239

Pioneer Standard
7625 Golden Triangle Dr.
Eden Prarie, MN 55344
Phone - 612-944-3355
FAX - 612-944-3794

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

KANSAS

Representative

Advanced Technical Sales
601 N. Mur-Len, Suite 8
Olathe, KS 66062
Phone - 913-782-8702
FAX - 913-782-8641

Distributors

Hall-Mark Electronics Corporation
10809 Lakeview Dr.
Lenexa, KS 66215
Phone - 913-888-4747
FAX - 913-888-0523

Pioneer Electronics
2029 Woodland Pkwy., Suite #101
St. Louis, MO 63146
Phone - 314-432-4350
FAX - 314-432-4854

Military Distributor

Zeus Components, Inc.
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Richardson, TX 75081
Phone - 214-783-7010
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KENTUCKY

Representatives

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7321 Shadeland Station, Suite 256
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Fax - 317-841-0107

Scott Electronics, Inc.
Lima Valley Office Village
8109 Lima Road
Fort Wayne, IN 46818
Phone - 819-489-5690
Fax - 819-489-1842

Scott Electronics, Inc.
10901 Reed-Hartman Hwy., Suite 301
Cincinnati, OH 45242-2821
Phone - 513-791-2513
FAX - 513-791-8059

Distributors

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FAX - 614-888-0767

Hall-Mark Electronics Corporation (W. Ky)
4275 W. 96th Street
Indianapolis, IN 46268
Phone - 317-872-8875
FAX - 317-876-7165

Pioneer Standard (W. Ky)
9350 N. Priority Way, W. Dr.
Indianapolis, IN 46240
Phone - 317-573-0880
FAX - 317-573-0979

Pioneer Standard (E. Ky)
4433 Interpoint Blvd.
Dayton, OH 45424
Phone - 513-236-9900
FAX - 513-236-8133

LOUISIANA

Representative

Nova Marketing Incorporated
8350 Meadow Road, Suite 174
Dallas, TX 75231
Phone - 214-750-6082
FAX - 214-750-6068

Distributors

Hall-Mark Electronics Corporation
11333 Pagemill Road
Dallas, TX 75243
Phone - 214-343-5000
FAX - 214-343-5851
Pioneer Electronics
13710 Omega Road
Dallas, TX 75234
Phone - 214-386-7300
FAX - 214-490-6419

Wyle Laboratories
1810 N. Greenville Ave.
Richardson, TX 75081
Phone - 214-235-9953
FAX - 214-644-5064

Military Distributors

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

Zeus Components, Inc.
1800 N. Glenville, Suite 120
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MAINE

Representative

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348 Park Street, Suite 102
North Reading, MA 01864
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FAX - 508-664-5503

Distributors

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
FAX - 508-657-6008

Gerber Electronics
128 Carnegie Row
Norwood, MA 02062
Phone - 617-769-6000
Fax - 617-762-8931

Micron Technology, Inc., reserves the right to change products or specifications without notice.

Hall-Mark Electronics Corporation
Pinehurst Park, 6 Cook Street
Billerica, MA 01821
Phone - 617-935-9777
FAX - 617-667-4129

Pioneer Standard
44 Hartwell Ave.
Lexington, MA 02173
Phone - 617-861-9200
FAX - 617-863-1547

Wyle Laboratories
15 3rd Ave.
Burlington, MA 01803
Phone - 617-272-7300
FAX - 617-272-6809

Military Distributors

JAN Devices
44 Cochrane St.
Melrose, MA 02176
Phone - 617-662-3901
Fax - 617-662-0837

Zeus Components, Inc.
11 Lakeside Office Park
607 North Ave.
Wakefield, MA 01880
Phone - 617-246-8200
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MARYLAND

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Electronic Engineering & Sales, Inc.
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Annapolis, MD 21401
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9020A Mendenhall Court
Columbia, MD 21045
Phone - 301-995-6640
FAX - 301-381-4379

Hall-Mark Electronics Corporation
10240 Old Columbia Road
Columbia, MD 21046
Phone - 301-988-9800
FAX - 301-381-2036

Pioneer Technologies
15810 Gaither Dr.
Gaithersburg, MD 20877
Phone - 301-921-0660
FAX - 301-921-3852

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FAX - 617-272-6809

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44 Cochrane St.
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Phone - 617-662-3901
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MICHIGAN

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Farmington Hills, MI 48331-3263
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38027 Schoolcraft Road
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FAX - 313-462-1830

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100 Midland Ave.
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FAX - 914-937-2553

Zeus Components, Inc.
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MINNESOTA

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Distributors

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Phone - 612-944-5454
FAX - 612-944-3045

Hall-Mark Electronics Corporation
10300 Valley View Road, Suite 101
Eden Prairie, MN 55343
Phone - 612-941-2600
FAX - 612-941-5778

Pioneer Standard
7625 Golden Triangle Dr.
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FAX - 205-830-2565

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FAX - 314-291-0362

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FAX - 408-452-8139

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FAX - 916-624-9750

Hall-Mark Electronics Corporation
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Phone - 916-624-9781
FAX - 916-961-0922

Wyle Laboratories
2951 Sunrise Blvd., Suite 175
Rancho Cordova, CA 95742
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FAX - 916-638-1491

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FAX - 617-662-0837

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FAX - 508-657-6008

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FAX - 617-667-4129

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FAX - 617-863-1547

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FAX - 617-246-8293

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Trevose, PA 19047
Phone - 215-244-4000
FAX - 215-244-4104

Distributors

Anthem Electronics
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Pine Brook, NJ 07058
Phone - 201-227-7960
FAX - 201-227-9246

Hall-Mark Electronics Corporation
Moorestown West Corporate Center
225 Executive Dr., Flex XI
Moorestown, NJ 08057
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FAX - 609-235-3381

Hall-Mark Electronics Corporation
200 Lanidex Plaza
Parsippany, NJ 07054
Phone - 201-515-3000
FAX - 201-515-4475

Pioneer Standard
14A Madison Road
Fairfield, NJ 07006
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FAX - 201-575-3454

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Port Chester, NY 10573
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FAX - 914-937-2553

Zeus Components, Inc.
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Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

NEW MEXICO

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Quatra Associates Incorporated
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Albuquerque, NM 87123
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FAX - 505-292-2092

Distributors

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1555 W. 10th Pl., Suite #101
Tempe, AZ 85281
Phone - 602-966-6600
FAX - 602-966-4826

Hall-Mark Electronics Corporation
4637 S. 36th Place
Phoenix, AZ 85040
Phone - 602-437-1200
FAX - 602-437-2348

Wyle Laboratories
4141 E. Raymond St., Suite #1
Phoenix, AZ 85040
Phone - 602-437-2088
FAX - 602-437-2124

Military Distributors

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

NEW YORK

Representatives

Electra Sales Corporation
3000 Winston Road S., Bldg. E
Rochester, NY 14623
Phone - 716-427-7860
FAX - 716-427-0614

Electra Sales Corporation
1 Alder Dr.
East Syracuse, NY 13057
Phone - 315-463-1248
FAX - 315-463-1717

Parallax, Inc.
734 Walt Whitman Road
Melville, NY 11747
Phone - 516-351-1000
FAX - 516-351-1606

Distributors

Anthem Electronics-Military
47 Mall Dr.
Commack, NY 11725-5703
Phone - 516-864-6600
FAX - 516-493-2244

Hall-Mark Electronics Corporation
6605 Pittsford - Palmyra Road, Suite E8
Fairport, NY 14450
Phone - 716-425-3300
FAX - 716-425-7195

Hall-Mark Electronics Corporation
101 Comac St.
Ronkonkoma, NY 11779
Phone - 516-737-0600
FAX - 516-737-0838

MAST Distributors, Inc.
710-2 Union Pkwy.
Ronkonkoma, NY 11779
Phone - 516-471-4422
FAX - 516-471-2040

Pioneer Standard
68 Corporate Dr.
Binghamton, NY 13904
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FAX - 607-722-9562

Pioneer Standard
840 Fairport Park
Fairport, NY 14450
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FAX - 716-381-5955

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Zeus Components, Inc.
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FAX - 919-544-5885

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Hall-Mark Electronics Corporation
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FAX - 612-941-5778

Pioneer Standard
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FAX - 918-254-6207

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FAX - 503-626-7928

Wyle Laboratories
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Beaverton, OR 97005
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FAX - 503-646-5466

Military Distributors

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Reseda, CA 91335
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FAX - 818-708-7436

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FAX - 203-272-1704

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